95160

Features

- Transmission Frequency 70MHz to 120MHz
- 40dB Channel Separation
- 15% Pilot Modulation
- Supply Voltage 4~6Volts
- Supply Current 28mA
- Stabilized PLL
- TSSOP-B24 Package

Applications

- Streaming Audio
- MP3 Player Audio Broadcasting
- FM Audio Transmissions
- Surround Sound

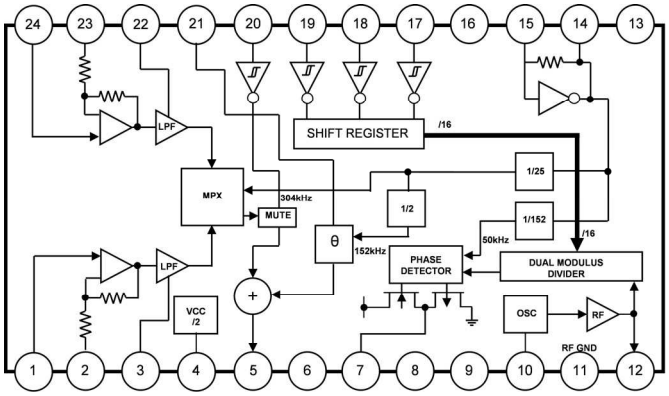
Functions

The PA1418 FV new stereo FM Chip is capable of broadcasting good quality signals over a range of about 60 feet. It's ideal for broadcasting music from a CD player or from any other source so that it can be picked up in another location.

For example, if you don't have a MP3/CD player in your car, you can use the PA1418 FV to broadcast signals from the portable MP3/CD player to your car's radio. Alternatively, you might want to use the PA1418 FV to broadcast signals from your lounge-room DVD/CD player to an FM receiver located in another part of the house or by the pool. It can be used for transmitting surround sound.

It broadcasts on the FM band (i.e., 88-108MHz) so that its signal can be received on any standard FM tuner or portable radio.

Functional Diagram



Pin Out

Pin	Designation
1	Right Ch INPUT
2	Pre-emphasis Time Constant
3	LPF Time Constant
4	Filter
5	Composite Signal Output
6	Ground
7	Phase Frequency Detector Output
8	Vcc
9	N.C.
10	RF Oscillator
11	RF Ground
12	RF Output
13	PLL Vcc
14	X'TAL Oscillator
15	X'TAL Oscillator
16	N.C.
17	Chip Enable
18	Clock
19	DATA
20	Audio Muting
21	Pilot Signal Adjust
22	LPF Time Constant
23	Pre-emphasis Time Constant
24	Left Ch INPUT

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified Ta = 25^{O}C, Vcc=3.3V Signal Source fin = 400Hz)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Quiescent Current	Iq	13	18.5	28	mA	
Channel Separation	Sep	25	40		dB	VIN=-20dBV,L-R, R-L
Total Harmonic Distortion	THD		0.1	0.3	%	VIN=-20dBV,L+R
Channel Balance	C.B	-2	0	+2	dB	VIN=-20dBV,L+R
Input Output Gain	Gv	-2	0	+2	dB	VIN=-20dBV,L+R
Pilot Modulation Rate	Mp	12	15	18	%	VIN=-20dBV,L+R, Pin 5
Sub Carrier Rejection Rate	SCR	-	-30	-20	dB	VIN=-20dBV,L+R
Pre-emphasis time constant	T_{PRE}	40	50	60	µS	VIN=-20dBV,L+R
Limiter Input Level	$V_{IN\ (LIM)}$	-16	-13	-10	dBV	OP Level @ 1dB Gain Compression
LPF Cut Frequency	$F_{c\ (LPF)}$	12	15	18	kHz	Vo = -3dB Pin 2,23 Open
Mute Attenuation Volume	$V_{(MUTE)}$	-	-48	-42	dB	Vin = -20dBV, L+R
Transmission Output Level	V_{TX}	96	99	102	dBµV	FTX = 100MHz
“H” Level Input Current	I_{IH}	-	-	1.0	µA	Pin 17,18,19,20 Vin 3.3V
“L” Level Input Current	I_{IL}	-1.0	-	-	µA	Pin 17,18,19,20 Vout 0V
“H” Level Output Voltage	V_{OH}	V_{CC}-1.0	V_{CC}-0.15		V	Pin 7 IOUT = -1.0mA
“L” Level Output Voltage	V_{OL}		0.15	1.0	V	Pin 7 IOUT = 1.0mA
“Off” Level Peak Current 1	I_{OFF1}			100	nA	Pin 7 VOUT = 3.3V
“Off” Level Peak Current 2	I_{OFF2}	-100			nA	Pin 7 VOUT = GND

OPERATING RANGE

(Ta = 25°C,)

Parameter	Symbol	Limits	Unit	Conditions
Operating Supply Voltage	V_{CC}	2.7 to 4.0	V	Pin 8, 13.
Operating Temperature	T_{OPR}	-40 to +85	ºC	
Audio Input level	V IN-A	Up to 10	dBV	Pin 1, 24
Audio Input Frequency Band	fIN-A	20 to 15k	Hz	Pin 1, 24
Pre-emphasis time constant set up range	t_{PRE}	to 155	µS	Pin 2, 23
Transmission Frequency	fTX	70 to 120	MHz	Pin 10, 12
Control Terminal “H” level input voltage	VIH	0.8Vcc to Vcc	V	Pin 17, 18, 19, 20.
Control Terminal “H” level input voltage	VIL	GND to 0.2Vcc	V	Pin 17, 18, 19, 20.

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, In test circuit)

Parameter	Symbol	Limits	Unit	Conditions
Supply Voltage	V_{CC}	+7.0	V	Pin 8, 13.
Data Input voltage	V IN-D	- 0.3 to Vcc + 0.3	V	Pin 17,18,19,20.
Phase comparator output voltage	VOUT-P	- 0.3 to Vcc + 0.3	V	Pin 7.
Power dissipation	P D	630	mW	(*Note 1*)
Storage Temperature	Tstg	-55 to +125	ºC	

(*Note 1*) when operation temperature exceeds Ta= to 25ºC power is derated at 6.3mW per 1ºC

PA1418 FV FM Stereo Transmitter

The PA1418 FV, FM stereo transmitter IC made by ProTek Analog. Includes all the processing circuitry required for stereo FM transmission and also the crystal control section, which provides precise frequency locking
As shown, the PA1418 FV includes two separate audio processing sections, for the left and right channels. The left-channel audio signal is applied to pin 24 of the chip, while the right channel signal is applied to pin 1. These audio signals are then applied to a pre-emphasis circuit, which boosts those frequencies above a 50ms time constant (i.e., those frequencies above 3.183 kHz) prior to transmission
Pre-emphasis is used to improve the signal-to-noise ratio of the received FM signal. It works by using a complementary de-emphasis circuit in the receiver to attenuate the boosted treble frequencies after demodulation, so that the frequency response is restored to normal. At the same time, this also significantly reduces the hiss that would otherwise be evident in the signal

The amount of pre-emphasis is set by the value of the capacitors connected to pins 2 & 23Signal limiting is also provided within the pre-emphasis section. This involves attenuating signals above a certain threshold, to prevent overloading the following stages. That in turn prevents over-modulation and reduces distortion.The pre-emphasized signals for the left and right channels are then processed through two low-pass filter (LPF) stages, which roll off the response above 15kHz. This roll-off is necessary to restrict the bandwidth of the FM signal and is the same frequency limit used by commercial broadcast FM transmitters.

The outputs from the left and right LPFs are in turn applied to a multiplex (MPX) block. This is used to effectively produce sum (left plus right) and difference (left - right) signals which are then modulated onto a 38kHz carrier. The carrier is then suppressed (or removed) to provide a double-sideband suppressed carrier signal. It is then mixed in a summing (+) block with a 19kHz pilot tone to give a composite signal output (with full stereo encoding) at pin 5.

The phase and level of the 19kHz pilot tone are set using a capacitor at pin 21.The 38kHz multiplex signal and 19kHz pilot tone are derived by dividing down the 7.6MHz crystal oscillator located at pins 14 & 15. The frequency is first divided by four to obtain 1.9MHz and then divided by 50 to obtain 38kHz. This is then divided by two to derive the 19kHz pilot tone.

In addition, the 1.9MHz signal is divided by 19 to give a 100kHz signal. This signal is then applied to the phase detector, which also monitors the program counter output. This program counter is actually a programmable divider, which outputs a divided down value of the RF signal.

The division ratio of this counter is set by the voltage levels at inputs D0-D3 (pins 17-20). For example, when D0-D3 are all low, the programmable counter divides by 877. Thus, if the RF oscillator is running at 87.7MHz, the divided output from the counter will be 100kHz and this matches the frequency divided down from the 7.6MHz crystal oscillator (i.e., 7.6MHz divided by 4 divided by 19).

The phase detector output at pin 7 produces an error signal to control the voltage applied to a Varicap diode. And forms part of the RF oscillator at pin 10. Its frequency of oscillation is determined by the value of the inductance and the total parallel capacitance.

Since the varicap diode forms part of this capacitance, we can alter the RF oscillator frequency by varying its value. In operation, the varicap diode's capacitance varies in proportion to the DC voltage applied to it by the output of the PLL phase detector.

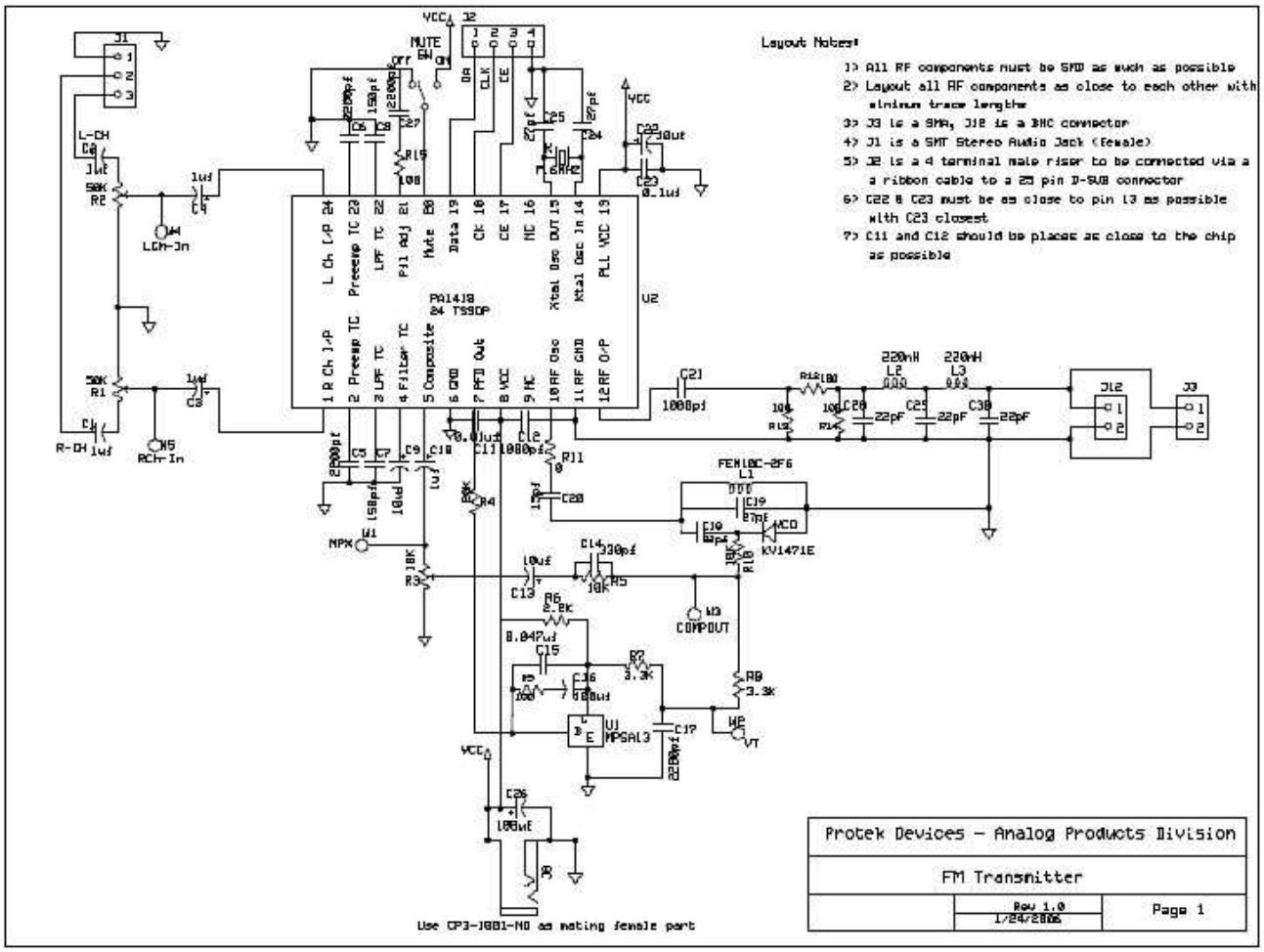
The phase detector adjusts the varicap voltage so that the divided RF oscillator frequency is 100 kHz at the program counter output. If the RF frequency drifts high, the frequency output from the programmable divider rises and the phase detector will "see" an error between this and the 100kHz provided by the crystal division.As a result, the phase detector reduces the DC voltage applied to the varicap diode, thereby increasing its capacitance. And this in turn decreases the oscillator frequency to bring it back into "lock".

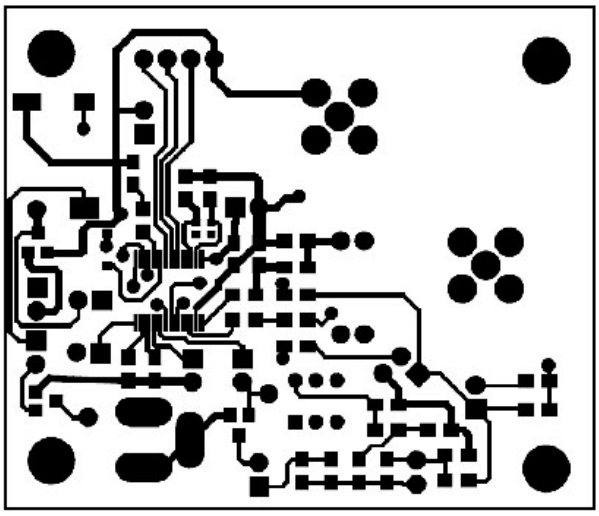
Conversely, if the RF frequency drifts low, the programmable divider output will be lower than 100kHz. This means that the phase detector now increases the applied DC voltage to the varicap to decrease its capacitance and raise the RF frequency. As a result, this PLL feedback arrangement ensures that the programmable divider output remains fixed at 100kHz and thus ensures stability of the RF oscillator.

By changing the programmable divider we can change the RF frequency. So, for example, if we set the divider to 1079, the RF oscillator must operate at 107.9MHz for the programmable divider output to remain at 100kHz.

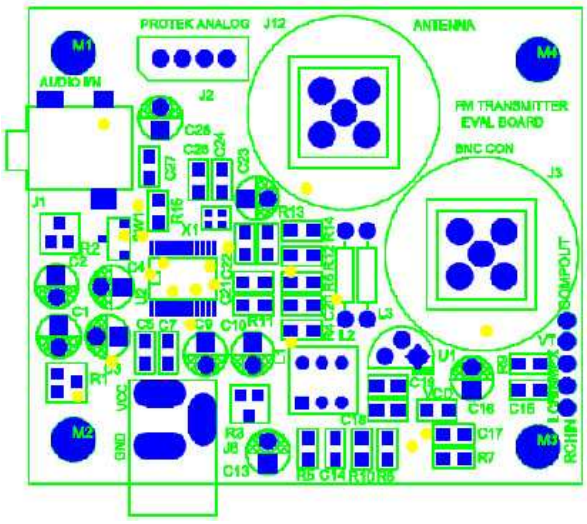
To frequency modulate the RF oscillator. We do that by modulating the voltage applied to the varicap diode using the composite signal output at pin 5.The average frequency of the RF oscillator remains fixed, as set by the programmable divider. As a result, the transmitted FM signal varies either side of the carrier frequency according to the composite signal level - i.e., it is frequency modulated.

Typical Application



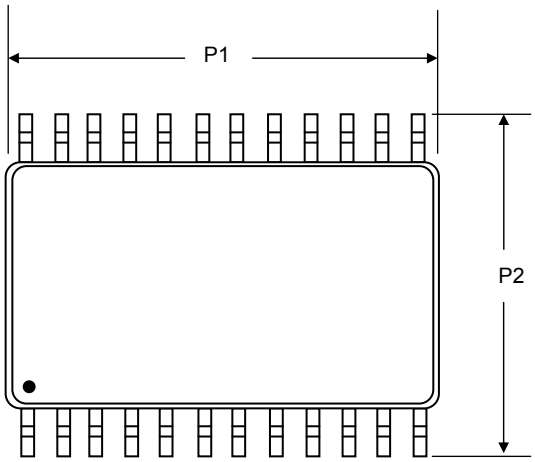


PCB Layout Back Side

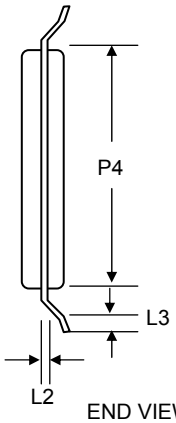


PCB Layout Component Side

Package Layout and Dimensions TSSOP-B24

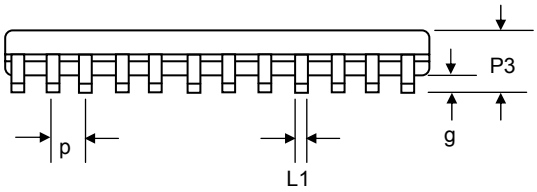


TOP VIEW

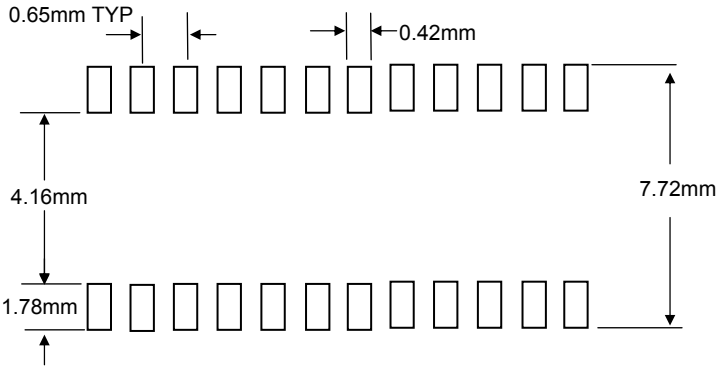


END VIEW

Dim	MILLIMETERS		
	MIN	TYP	MIN
P1	7.70	7.80	7.90
P2	6.40	6.40	6.40
P3	1.18	1.19	1.20
P4	4.30	4.40	4.50
L1	0.19	0.25	0.30
L2	0.10	0.11	0.12
L3	0.50	0.60	0.70
p	0.65	0.65	0.65
g	0.06	0.10	0.15



SIDE VIEW



Recommended Pattern Layout