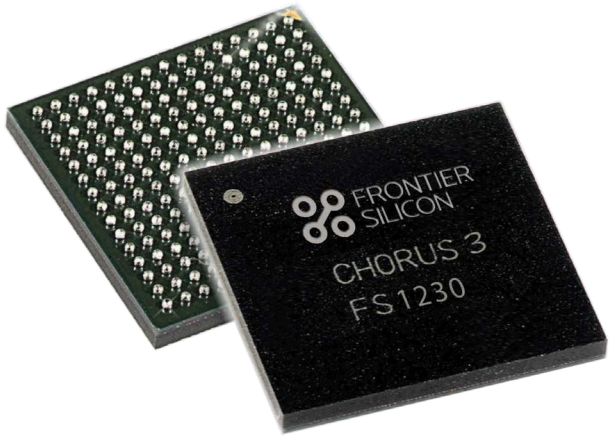
CHORUS 3 FS1230

Advanced digital radio and audio baseband network processor



CHORUS 3 CHIP

APPLICATIONS

- **WorldDMB Profile 1 and Profile 2 digital radio receivers**
- **Internet radio**
- **Media player with multiple codecs**
- **Connected digital audio**
- **DAB/DAB+**
- **DMB-Audio**
- **FM-RDS**

OVERVIEW

The Chorus 3 baseband processor is the latest generation of integrated system-on-chip, providing an optimised solution for WorldDMB Profile 1 and Profile 2 DAB/DAB+/DMB-A and FM-RDS broadcast receivers and Internet radio products.

Chorus 3 is an advanced programmable baseband receiver capable of receiving DAB/DAB+ and DMB-A broadcasts as well as being able to receive and decode internet radio streaming audio. It incorporates a number of mixed signal system components as well as advanced peripherals previously only available as discrete additional components, providing significant space, cost and power savings.

The CPU provides the processing power to receive digital radio, decode internet media and operate the user interface in the system. It is powerful enough to be the master processor in any digital radio system.

Coupled to the CPU are a host of interfaces that allow interfacing to displays, external memory storage and PCs, allowing Chorus 3-based receivers to connect to other devices with minimal additional components.

ADVANCED POWER MANAGEMENT

Chorus 3 uses dynamic and static power management techniques including fully-static design, clock-gating and inactive period state minimisation for low power usage without compromising performance. The processor clock is generated by a PLL which can be reprogrammed dynamically, enabling power consumption to be minimised for specific applications.

EVALUATION

Chorus 3 will be available on a range of DAB and Internet Radio modules from Frontier Silicon. Full software, reference design and evaluation platforms are also available.

225 ball BGA 13 x13 x 1.2 mm, 0.8 mm pitch

FEATURES

- CPU 166 MHz META122 RISC/DSP multithreaded
- Memory configurable between system and TCM (Tightly Coupled Memory)
- 64K ROM located in TCM space for boot and library functions
- Analogue interface to DAB RF for zero and low IF
- SDIO/SD device Interface
- USB 2.0 Full-speed/high-speed host/device
- 10/100 Ethernet MAC
- 18-bit RGB TFT interface
- Monochrome LCD interface
- EMI (External Memory Interface) for connection to external SDRAM
- NAND flash interface
- 4 PDM DAC outputs
- Standard 16550 UART
- SCB 2-wire bus (I^2C-compatible)
- I^2S and S/PDIF audio output
- SDRAM/SRAM/ROM/Flash memory interface
- 10-bit ADC
- Temperature range
  - Operating -40 to +65 °C at 90% humidity
  - Storage -40 to +125 °C
- Full RoHS compliance

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Chorus 3 FS1230 Product Brief FSM 0000 1025 Rev 4

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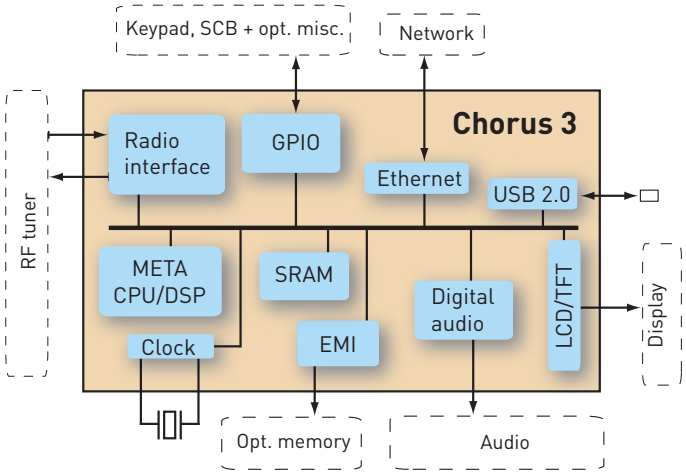
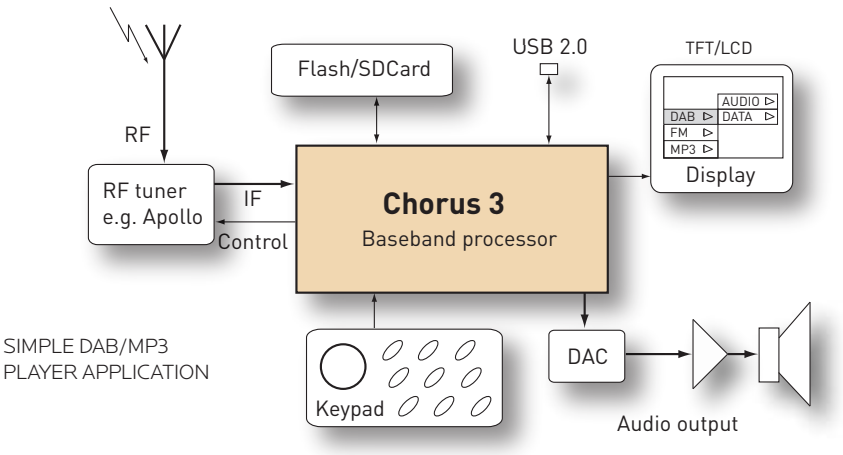
EXTENSIVE INTERFACES

- **10/100 Ethernet** MAC interface to external PHY
- **USB 2.0** interface with support for full-speed (12 Mbps) and high-speed (480 Mbps) operation
- Integrated support for **TFT** and **LCD** displays
- **SD** interface for optional mass storage applications
- Extensive and flexible **GPIO**
- **S/PDIF** audio output
- Up to 8-channel I^2S output of decoded audio data (both master and slave modes)
- Support for 5 **SPI slave** devices (including DMB TS data output, SD card profile and optional local SPI Flash)
- SPI slave port available for MSC/TS data output and control to/from host
- 3 SCB (I^2C-compatible) ports for control of RF device and optional control from host
- 4 PDM DAC outputs for interface to RF tuners and other applications
- 16 550-compliant **UART** with optional flow control
- **JTAG** interface for test and emulator support
- Support for expansion RAM (SRAM, Cellular SRAM, SDRAM or mobile SDRAM) for the most demanding applications.





ARCHITECTURE

The META multithreaded core is a high-performance low-power modular device enabling extensive customisation. It is designed for use in applications such as audio signal processing and next-generation digital wireless.

Processor architecture	Multithreaded 3-operand register based
Data types and registers	16/32-bit integer ALU with multiple 32-bit register files
System architecture	Independent 64-bit instruction and data interfaces
Exceptions and interrupts	Memory, instruction, and interrupt handling on each thread
Instruction set	RISC 32-bit with 64-bit extensions
Pipeline	3-stage

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