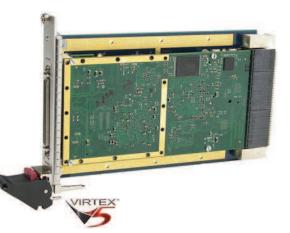
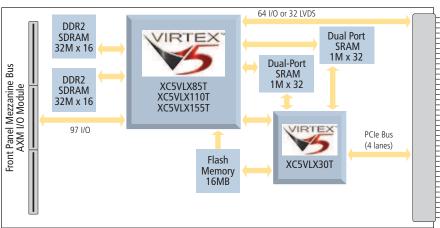
VPX-VLX VPX Board with User-Configurable Virtex-5 FPGA









VPX 3U card with PCIe interface ◆ Logic-optimized Virtex-5 FPGA ◆ Air and conduction-cooled models

Description

VPX-VLX85: 85k logic cells VPX-VLX110: 110k logic cells VPX-VLX155: 155k logic cells

Acromag's VPX-VLX 3U VPX boards feature a configurable Xilinx® Virtex®-5 FPGA enhanced with multiple high-speed memory buffers and a high-throughput PCIe interface. The result is a powerful and flexible logic processor module that is capable of executing your custom instruction sets and algorithms.

Three models provide a choice of logic-optimized FPGAs to match your performance requirements. Although there is no limit to the uses for these boards, several applications are ideal. Typical uses include hardware simulation, military servers, communications, in-circuit diagnostics, signal intelligence, and image processing.

Large, high-speed memory banks provide efficient data handling. Generous DDR2 SDRAM buffers store captured data prior to FPGA processing. Afterward, data is moved to dualport SRAM for high-speed DMA transfer to/from the rest of the system. A high-bandwidth PCIe interface ensures fast data throughput.

64 I/O lines are accessible through the rear (P2) connector. Additional I/O processing is supported on a separate mezzanine card that plugs into the FPGA base board. A variety of these external AXM I/O cards are available to interface your analog and digital I/O signals.

Take advantage of the conduction-cooled version for use in hostile environments. Conduction efficiently dissipates heat if there is inadequate cooling air flow.

Acromag's Engineering Design Kit provides software utilities and example VHDL code to simplify your program development and get you running quickly. A JTAG interface enables on-board VHDL debugging.



Conduction-cooled version



Plug in an AXM analog or digital I/O module for additional I/O signal processing capabilities.

Key Features & Benefits

- Reconfigurable Xilinx Virtex-5 FPGA
- PCIe bus 4-lane Gen 1 interface
- Supports both front and rear I/O connections
- 64 I/O or 32 LVDS lines direct to FPGA via rear (P2) connector
- Plug-in I/O extension modules are available for the front mezzanine
- FPGA code loads from the PCIe bus or from on-board flash memory
- 1M x 64-bit dual-ported SRAM provides direct links from the PCle bus and to the FPGA
- 32M x 32-bit DDR2 SDRAM is directly accessed through the FPGA
- Supports dual DMA channel data transfer to/from the rest of the system
- Support for Xilinx ChipScope™ Pro interface
- Designed for conduction-cooled host card or -40 to 85°C operation in air-cooled systems



Tel 248-295-0310 ■ Fax 248-624-9234 ■ solutions@acromag.com ■ www.acromag.com ■ 30765 Wixom Rd, Wixom, MI 48393 USA

VPX-VLX VPX Board with User-Configurable Virtex-5 FPGA

Performance Specifications

General

Form Factor

3U VPX bus 6.299" (160mm) x 3.937" (100.0mm).

Pitch

VPX-VLXxxx (air-cooled): 0.80" pitch. VPX-VLXxxx-CC (conduction-cooled): 0.85" pitch.

Chassis Compatibility

Compatible VITA 65 module / slot profiles: MOD3-PER-2F-16.3.1-3 / SLT3-PER-2F-14.3.1 MOD3-PER-1F-16.3.2-2 / SLT3-PER-1F-14.3.2 MOD3-PAY-1D-16.2.6-11 / SLT3-PAY-1D-14.2.6 MOD3-PAY-2F-16.2.7-11 / SLT3-PAY-2F-14.2.7 Note 1: Board is compatible with payload profiles but has no hosting capabilities.

FRU EEPROM with temperature monitor.

PCI Express Interface

VITA 46.4 fat pipe (x4) PCIe Gen 1 interface.

FPGA

VPX Model	Virtex-5 FPGA Device	Logic Cells	DSP48E Slices
VPX-VLX85	XC5VLX85T	82,944	48
VPX-VLX110	XC5VLX110T	110,592	64
VPX-VLX155	XC5VLX155T	155,648	128

FPGA configuration

Download via PCIe bus or flash memory.

Example FPGA program

VHDL provided for bus interface, front & rear I/O control, SRAM read/write interface logic, and SDRAM memory interface controller. See EDK kit.

I/O Processing

Acromag AXM I/O modules:

AXM modules plug into the FPGA board's front mezzanine for additional I/O lines. Analog and digital I/O AXM modules are sold separately.

Rear I/O

64 I/O (32 LVDS) lines supported with a direct connection between the FPGA and the rear I/O connector (P2).

Engineering Design Kit

Provides user with basic information required to develop a custom FPGA program. Kit must be ordered with the first purchase of a VPX-VLX module (see www.acromag.com for more information).

Environmental

Air-Cooled Operating Temperature

0 to 70°C (air flow requirement as measured to be greater than 200 LFM).

Conduction-Cooled Operating Temperature Range -40 to 85°C (board must operate in a fully-installed conduction-cooled rack).

Storage Temperature Range

-55 to 100°C.

Relative Humidity

5 to 95% non-condensing.

Vibration

0.05g RMS (20 - 2000Hz) random, operating 6g RMS per Hz spectrum.

Shock

30g each axis, 11ms.

MTBF

Consult factory.

Power Requirements **Carrier-Only Power Requirements**

- +3.3V DC: 0.9A typical plus any additional power consumed by PMC/XMC (4A max).
- +5V DC: 0.9A typical plus any additional power consumed by PMC/XMC (4A max).
- +12V DC and -12V DC provided to PMC site from VPX backplane.

Ordering Information

NOTE: XMC-VLX-EDK is required to configure FPGA.

■ VPX Boards

VPX-VLX85

3U VPX, Virtex-5 FPGA, 85k logic cells, air-cooled

VPX-VLX85-CC

Same as VPX-VLX85 except conduction-cooled

3U VPX, Virtex-5 FPGA, 110k logic cells, air-cooled

VPX-VLX110-CC

Same as VPX-VLX110 except conduction-cooled

VPX-VLX155

3U VPX, Virtex-5 FPGA, 155k logic cells, air-cooled

VPX-VLX155-CC

Same as VPX-VLX155 except conduction-cooled

■ AXM Plug-In I/O Extension Modules

For more information, see www.acromag.com.

AXM-A30

2 analog input 100MHz 16-bit A/D channels

AXM-D02

30 RS485 differential I/O channels

AXM-D03

16 CMOS and 22 RS485 differential I/O channels

AXM-D04

30 LVDS I/O channels

Custom I/O configurations available, call factory.

Software

For more information, see www.acromag.com.

XMC-VLX-EDK

Engineering Design Kit (one kit required)

PMCSW-API-VXW

VxWorks® software support package

PCISW-API-WIN

Windows® DLL software support package

PCISW-LINUX

Linux™ support (website download only)

VIRTEX-5 FPGA JTAG / CHIPSCOPE FRONT PANE LOGIC CONTROL LINES VIRTEX-5 DIGITAL CLOCK MANAGER DUAL-PORT SRAM TERFACE / INTERRU CONTROL & LOGIC 64 I/O USER LOCAL BUS INTERFACE LOGIC LOCAL CRYSTAL 125MHZ ■ SRAM 2 CLOCK IRTEX-5 LX30T PCIe INTERFACE CONFIGURATION CONTROL LOGIC LOCAL BUS CLOCK MULTIPLEXER CONTROL LOGIC LOW SKEW CLOCK DRIVERS DMA CH 0 AND 1 INTERRUPT LOGIC



