

Audio Modulated Matrix LED Driver

Description

SN3730 is a LED matrix driver which features an audio modulation display mode and a general LED dot matrix display mode. The default configuration of SN3730 is to drive a single 8×8 LED matrix. However, SN3730 may be configured to drive either one or two 8×8, 7×9, 6×10, or 5×11 dot matrix display(s). The intensity of any matrix picture can be modulated by an audio signal.

In matrix display mode, the rows and columns of the matrix are internally scanned, requiring only one time programming of the individual LED on or off state, thus eliminating the need for real time system resource utilization to perform the row and column scanning function.

In the general purpose mode, the ON or OFF condition of each individual LED in the display matrix is programmed via an I2C interface.

SN3730 is available in QFN-24 (4mm×4mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

Features

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Internal reset register
- Programmable single or dual 8×8, 7×9, 6×10, or 5×11 LED matrix display mode
- One-time programming, internal scan
- Audio modulated display intensity with digitally programmable input gain
- Internal registers to digitally adjust display intensity
- Modulate LED brightness with 128 different items in PWM
- One address pin with 4 logic levels to allow four I2C slave addresses
- Over-temperature protection
- QFN-24 (4mm × 4mm) package

Applications

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

Typical Application Circuit

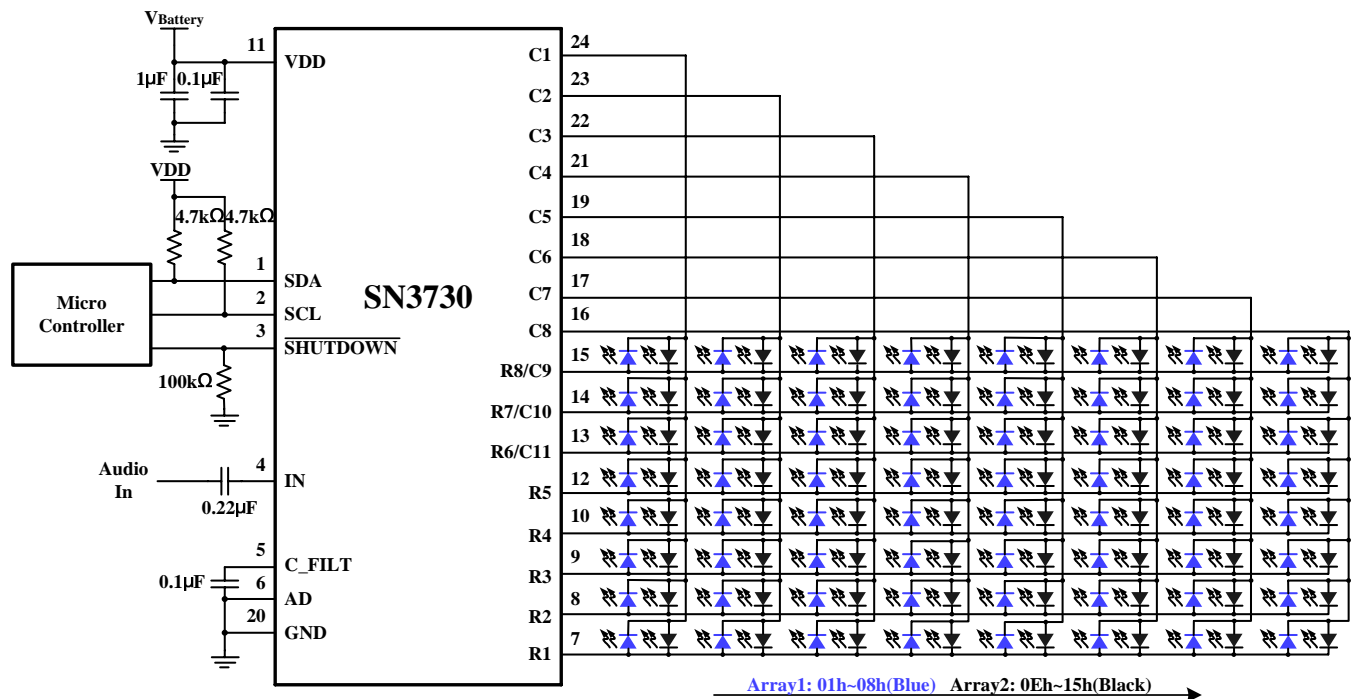


Figure 1 Typical application circuit dual 8×8

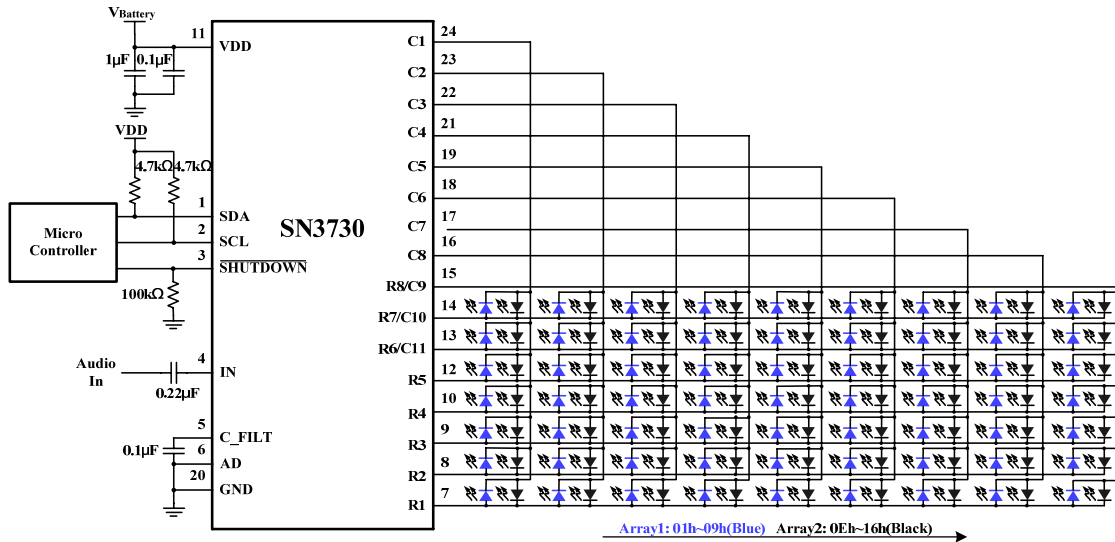


Figure 2 Typical application circuit dual 7×9

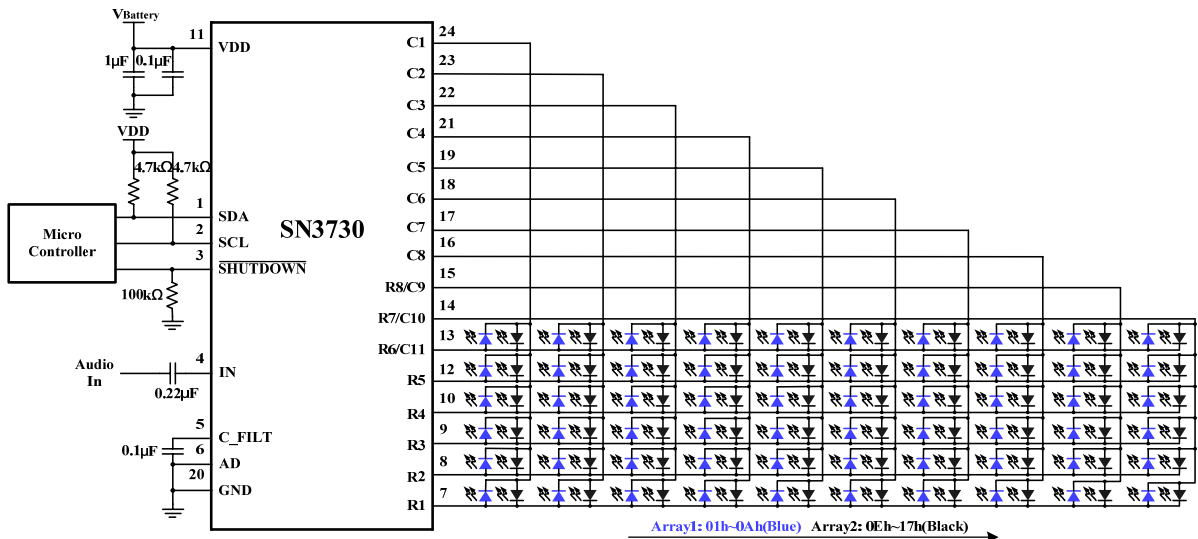


Figure 3 Typical application circuit dual 6×10

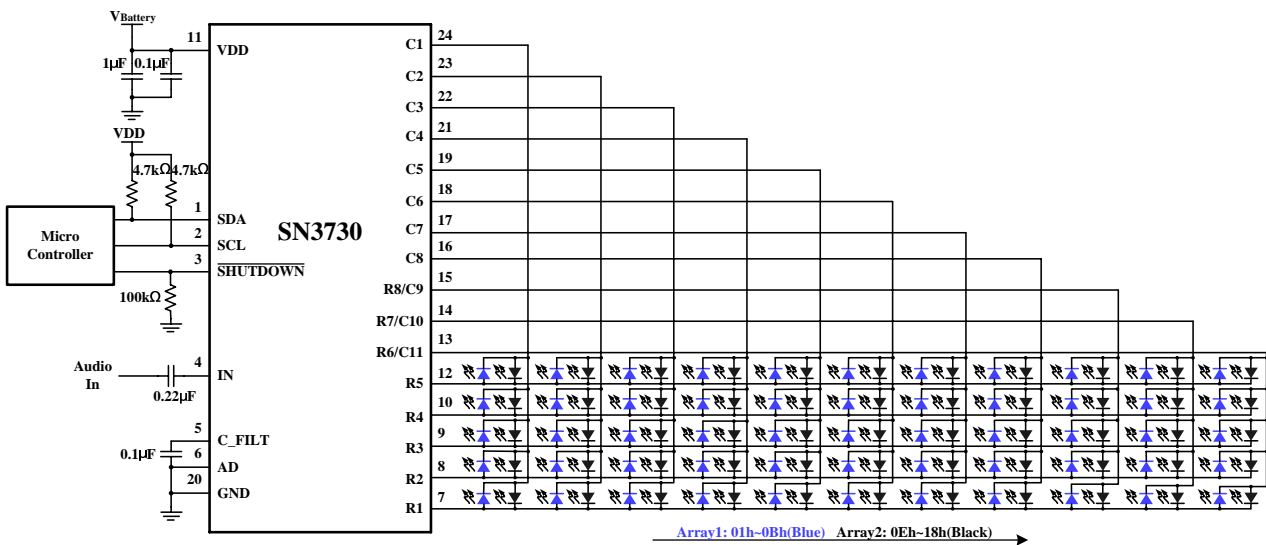
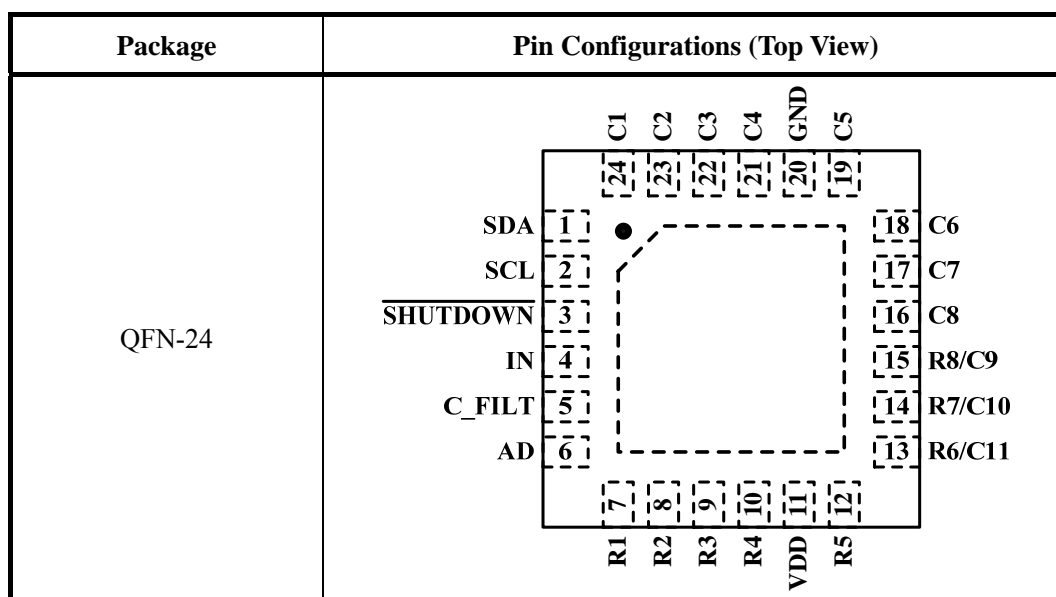


Figure 4 Typical application circuit dual 5×11

Pin Configurations



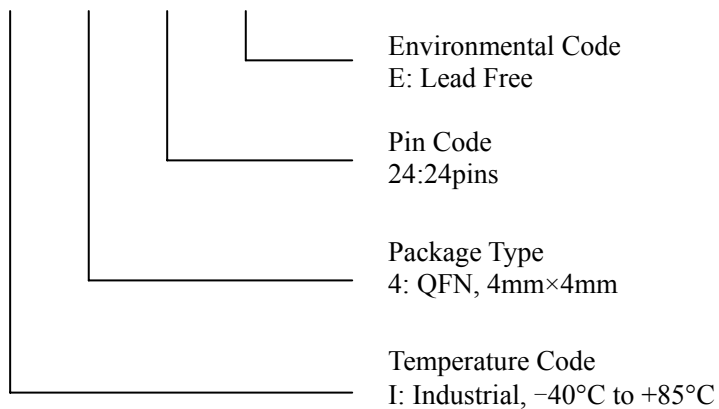
Pin Description

No.	Pin	I/O	Description
1	SDA	I/O	I2C serial data
2	SCL	I	I2C serial clock
3	SHUTDOWN	I	Shutdown the chip when pull to low
4	IN	I	Audio input
5	C_FILT	-	Filter cap for audio control
6	AD	I	I2C address setting
7~10, 12	R1~R5	-	Row control
11	VDD	I	Power supply
13~15	R6/C11, R7/C10, R8/C9	-	Row/column control
16~19, 21~24	C8~C5, C4~C1	-	Column control
20	GND	I	Ground
Thermal Pad	Thermal Pad		Connect to GND

Ordering Information

Order Number	Package Type	QTY/Reel	Operating Temperature Range
SN3730I424E	QFN-24	2500	-40°C to +85°C

SN3730 □ □ □ □



Absolute Maximum Ratings

Supply Voltage, V_{DD} -----	-0.3V to 6.0V
Voltage at Any Input Pin -----	-0.3V to $V_{DD} + 0.3V$
Junction Temperature, T_{JMAX} -----	150°C
Thermal Resistance θ_{JA} (QFN-24) -----	30°C/W

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD}=2.7V$ to $5.5V$, unless otherwise noted. Typical value are $T_A=25^\circ\text{C}$, $V_{DD}=3.6V$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7		5.5	V
I_{DD}	Quiescent power supply current	$V(IN)=0V$, without audio input, all LEDs off		7.0		mA
I_{SD}	Shutdown current	$\overline{SHUTDOWN} = 0V$		0.2	1.0	μA
		$\overline{SHUTDOWN} = V_{DD}$, software shutdown		1.7	3.0	
I_{OUT}	Output current of R1~R8, C1~C8	Matrix display mode without audio modulation Lighting Effect Register(0Dh) = 0xxx 0000		40 <i>(Note 1)</i>		mA
		Matrix display mode with audio modulation $V(IN)=2.5V_{P-P}$, 1kHz square wave, audio gain=0dB		40 <i>(Note 1)</i>		
V_{HR}	Current sink headroom voltage R1~R8, C1~C8	$I_{sink}=320mA$ <i>(Note 2)</i>		300		mV
	Current source headroom voltage R1~R8, C1~C8	$I_{source}=40mA$		200		
T_{SCAN}	Period of row and column scanning <i>(Figure 10)</i>			32		μs
T_{SCANOL}	Non-overlap blanking time during row and column scan <i>(Figure 10)</i>			1		μs

Logic Electrical Characteristics (SDA, SCL, AD)

V_{IL}	Logic “0” input voltage	$V_{DD} = 2.7V$			0.4	V
V_{IH}	Logic “1” input voltage	$V_{DD} = 5.5V$	1.4			V
I_{IL}	Logic “0” input current	$V(IN)=0V$		5 <i>(Note 3)</i>		nA
I_{IH}	Logic “1” input current	$V(IN)=V_{DD}$		5 <i>(Note 3)</i>		nA

Digital Input Switching Characteristics (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μ s
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μ s
$t_{SU, STA}$	Repeated START condition setup time		0.6			μ s
$t_{SU, STO}$	STOP condition setup time		0.6			μ s
$t_{HD, DAT}$	Data hold time				0.9	μ s
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μ s
t_{HIGH}	SCL clock high period		0.7			μ s
t_R	Rise time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns

Note 1: Due to the row and column scanning sequence, the average current of an individual LED in the display is $I_{OUT}/8$ when configured to drive a single matrix. When configured to drive two matrices, the average current of an individual LED in the display is $I_{OUT}/16$.

Note 2: All row drivers are ON.

Note 3: Guaranteed by design.

Note 4: Cb = total capacitance of one bus line in pF. $I_{SINK} \leq 6mA$. t_R and t_F measured between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

Detailed Description

I2C Interface

The SN3730 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The SN3730 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Since SN3730 only supports write operations, A0 must always be 0. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table1 Slave Address (Write only):

Bit	A7:A3	A2:A1	A0
Value	11000	AD	0

- AD connected to GND, AD=00;
- AD connected to VDD, AD=11;
- AD connected to SCL, AD=01;
- AD connected to SDA, AD=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the SN3730.

The timing diagram for the I2C is shown in Figure 5. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the SN3730's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the SN3730 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of SN3730, the register address byte is sent, most significant bit first. SN3730 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the SN3730 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

Address Auto Increment

To write multiple bytes of data into SN3730, load the address of the data register that the first data byte is intended for. During the SN3730 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to SN3730 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to SN3730. This feature is useful for loading the LED on/off condition for each of the display matrices as a burst of data. Pay careful attention when loading data for dual LED matrix displays since the register addressing is not continuous.

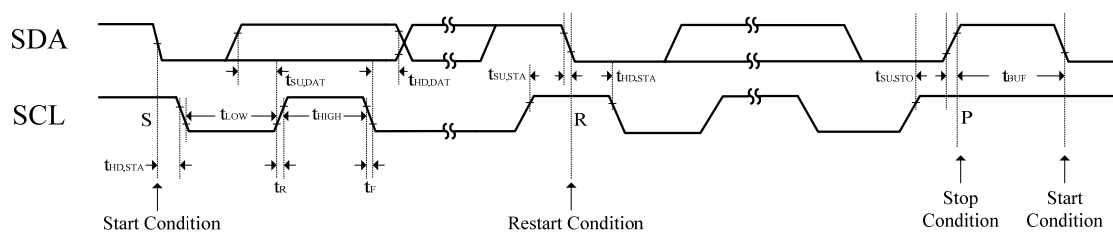


Figure 5 Interface timing

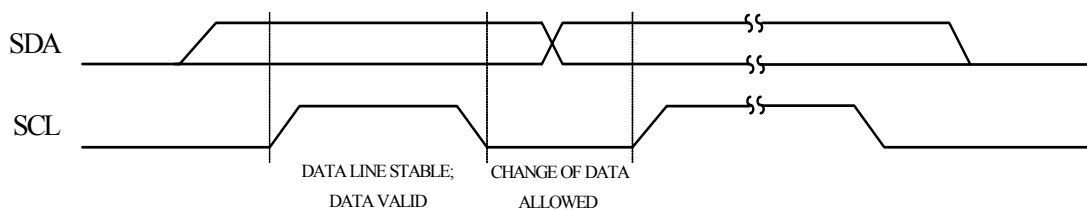


Figure 6 Bit transfer

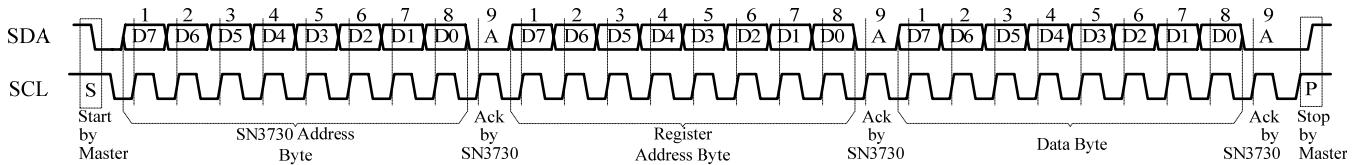


Figure 7 Writing to SN3730(Typical)

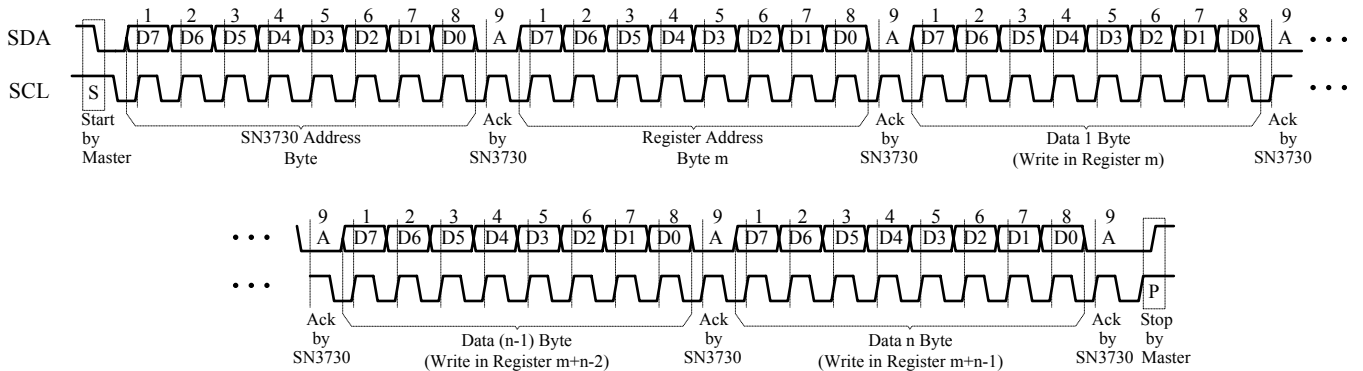


Figure 8 Writing to SN3730(Automatic address increment)

Registers Definitions

Table2 Register Function

Address	Name	Function	Table	Default
00h	Configuration Register	Set operation mode of SN3730	3	0000 0000
01h~0Bh	Matrix1 Data Register	Store the on or off state of each LED	4	0000 0000
0Eh~18h	Matrix2 Data Register	Store the on or off state of each LED	5	
0Ch	Update Column Register	Make the Data Register update the data	-	xxxx xxxx
0Dh	Lighting Effect Register	Store the intensity control settings	6	0000 0000
19h	PWM Register	Modulate LED light with 128 different items	7	1000 0000
FFh	Reset Register	Reset all registers to default value	-	xxxx xxxx

Table3 00h Configuration Register

Bit	D7	D6:D5	D4:D3	D2	D1	D0
Name	SSD	Reserved	DM	A_EN	ADM	
Default	0	00	00	0	0	0

The Configuration Register sets operation mode of SN3730.

SSD Software Shutdown Enable

0 Normal operation

1 Software shutdown mode

DM Display Mode

00 Matrix1 only

01 Matrix2 only

11 Matrix1 and Matrix2

A_EN Audio Input Enable

0 Matrix intensity is controlled by the current setting in the Lighting Effect Register (0Dh)

1 Enable audio signal to modulate the intensity of the matrix

ADM Matrix Mode Selection

00 8×8 dot matrix display mode

01 7×9 dot matrix display mode

10 6×10 dot matrix display mode

11 5×11 dot matrix display mode

Table4 01h~0Bh Matrix1 Data Register(C1~C11)

Bit	D7:D0
Name	R8:R1
Default	00000000

Table5 0Eh~18h Matrix2 Data Register(C1~C11)

Bit	D7:D0
Name	R8:R1
Default	00000000

The Data Registers(Matrix1/Matrix2) store the on or off state of each LED in the Matrix.

Rx LED State

0 LED off

1 LED on

11×2 registers are assigned to C1~C11 columns respectively; the LED at a particular (row, column) location will be turned on when the respective data is set to “1”. When configured for more than 8 column operation, only the required numbers of LSBs are used in each data register. For example, in 5×11 dot matrix mode, only bits R1 thru R5 are used, and bits R6 thru R8 are ignored.

0Ch Update Column Register

The data sent to the Data Registers will be stored in temporary registers. A write operation of any 8-bit value to the Update Column Register is required to update the Data Registers (01h~0Bh, 0Eh~18h).

Table6 0Dh Lighting Effect Register

Bit	D7	D6:D4	D3:D0
Name	Reserved	AGS	CS
Default	0	000	0000

The Lighting Effect Register stores the intensity control settings for all of the LEDs in the Matrix

AGS Audio Input Gain Selection

000: Gain= 0dB

001: Gain= +3dB

010: Gain= +6dB

011: Gain= +9dB

100: Gain= +12dB

101: Gain= +15dB

110: Gain= +18dB

111: Gain= -6dB

CS Full Current Setting for Each Row Output

0000: 40mA

0001: 45mA

... ..

0111: 75mA

1000: 5mA

1001: 10mA

... ..

1110: 35mA

Table7 19h PWM Register

Bit	D7	D6:D0
Default	1	0000000

The PWM Register can modulate LED light with 128 different items.

When the D7 set to “1”, the PWM is the 128 item.

When the D7 set to “0”, D6:D0 set the PWM from the 0 item to the 127 item.

For example, if the data in PWM Register is 0000 0100, then the PWM is the 4 item.

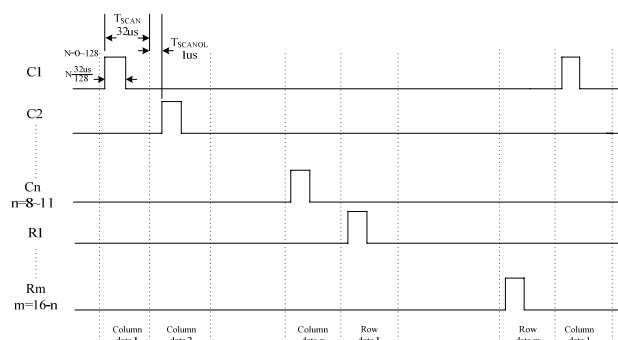


Figure 9 PWM timing diagram

FFh Reset Register

Once user writes any 8-bit data to the Reset Register, SN3730 will reset all registers to default value. On initial power-up, the SN3730 registers are reset to their default values for a blank display.

Typical Application

General Purpose Dot Matrix Display Mode

The general purpose dot matrix display timing diagram is shown in Figure 10. SN3730 may be configured to drive displays of different dimensions from 8×8 to 5×11. Furthermore, SN3730 may be configured to drive one or two LED matrices of the same dimension. Therefore, the overall row and column scan time can vary based on the final LED matrix configuration.

In any LED matrix configuration, a single line (column or row) of LEDs is illuminated for 32 μ s before SN3730 moves on to the next line of LEDs (Figure 10).

Example 1: When the SN3730 is configured in the general purpose dual 8×8 dot matrix display mode, column controls C8:C1 scans the eight columns of Matrix1 then row controls R8:R1 scans the eight rows of Matrix2 at a rate of 1.89kHz, or 528 μ s per frame. Each line is active for 32 μ s. The non-overlap interval between adjacent lines is 1 μ s.

Example 2: When configured to drive a single 7×9 dot matrix display (Matrix1), the column controls C9:C1 scan the nine columns every 297 μ s. Also note that in this case, the Data Registers' MSB will be ignored.

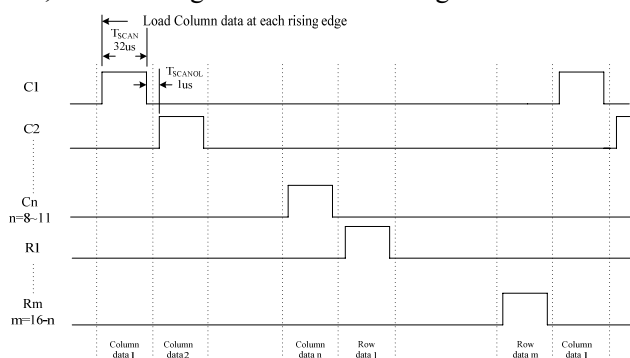


Figure 10 Dot matrix display timing diagram

Dual 8×8 Dot Matrix Display Mode

The application example in Figure 1 shows the SN3730 in the dual 8×8 LED dot matrix display mode.

The Matrix1 LED columns have common cathodes and are connected to the C1:C8 outputs. The rows are connected to the row drivers. The Matrix2 LED rows have common cathodes and connected to the R1:R8. The columns are connected to the C1:C8. Each of the 128 LEDs can be addressed separately.

Dual 5×11 Dot Matrix Display Mode

By setting the ADM bits of the Configuration Register(00h) to “11” and the DM bits to “11”, the SN3730 will operate in the dual 5×11 LED dot matrix display mode.

The Matrix1 LED columns have common cathodes and are connected to the C1:C11 outputs. The rows are connected to the row drivers. The Matrix2 LED rows have common cathodes and are connected to the R1:R5 outputs. The columns are connected to the column drivers. Each of the 110 LEDs can be addressed separately. The three MSBs (D7:D5) of each Data Register (01h~0Bh, 0Eh~18h) are ignored.

Dot Matrix Display Mode with Audio Modulation

When the SN3730 operates in any of the dot matrix modes, if the bit A_EN in Configuration Register (00h) is set to “1”, the brightness of LED image can be modulated by audio signal not controlled by the CS bit in Lighting Effect Register (0Dh).

An external capacitor, C_FILT is required to control the rate at which the display intensity will change. The rate of change is computed using the formula: $\Delta T = C \times 500k\Omega$. A value of 0.1 μ F provides a good effect by allowing the display to fade from full intensity to off in approximately 50ms. Smaller capacitance will cause the intensity to change more quickly, and, conversely, a larger capacitance will cause the display intensity to change at a slower rate.

Shutdown Mode

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

Software Shutdown

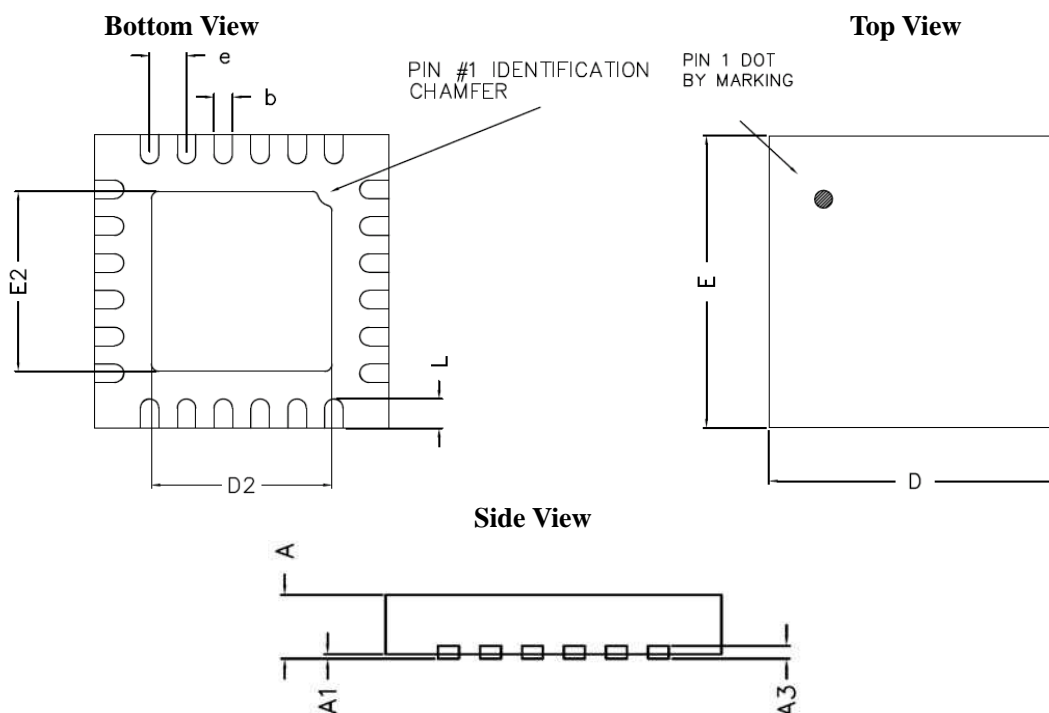
By setting SSD bit of the Configuration Register (00h) to “1”, the SN3730 will operate in software shutdown mode, wherein they consume only 1.7 μ A (typ.) current. When the SN3730 is in software shutdown mode, all current sources and digital drivers are switched off, so that the matrix is blanked.

Hardware Shutdown

The chip enters hardware shutdown mode when the SHUTDOWN pin is pulled low.

Package Information

QFN-24



Symbol	Dimension (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	—	0.20.REF	—
D	3.90	4.00	4.10
E	3.90	4.00	4.10
b	0.18	0.25	0.30
L	0.30	0.40	0.50
D2	2.30	2.45	2.80
E2	2.30	2.45	2.80
e	0.50 BSC		

IMPORTANT NOTICE

SI-EN Technology cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a SI-EN Technology product. SI-EN Technology reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its specifications, products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.