Six-Channel RGB LED Driver

Description

The SN3103 is a constant current LED driver featuring One Shot Programming mode and Interface Intensity Control mode for RGB lighting effects.

Each output of the SN3103 is a constant current sink pulse width modulated in 256 steps. The output current is user selectable to be one of 5 levels, 17.5mA, 28.5mA, 38.9mA, 46.5mA or 69.5mA (Typ.). At 38.9mA the SN3103 outputs require only 0.4V of headroom voltage.

In One Shot Programming mode, the timing characteristics for output current - Gamma corrected current ramping up, holding, Gamma corrected ramping down and off time, can be adjusted individually so that each output can independently maintain a pre-established pattern without requiring any additional interface activity, thus saving valuable system resources.

In Interface Intensity Control mode, the PWM duty cycle of each output can be independently programmed and controlled in 256 steps to simplify color mixing.

Features

- 6 independently controlled outputs of 256 steps PWM RGB LED drivers
- Changing Intensity of Color LEDs with two modes:
  - −One Shot Programming Mode with Gamma correction
  - −Interface Intensity Control Mode
- Programmable output current level settings
- For anode-common LEDs
- SPI interface
- Supply voltage range: 3.0V to 5.5V
- Operating temperature range T_A = −40°C ~ +85°C
- Package: QFN-20, 4mm × 4mm

Application

- Cellular phones
- MP3/MP4/CD/minidiskplayers
- Digital Picture Frame/Toy

Typical Application Circuit

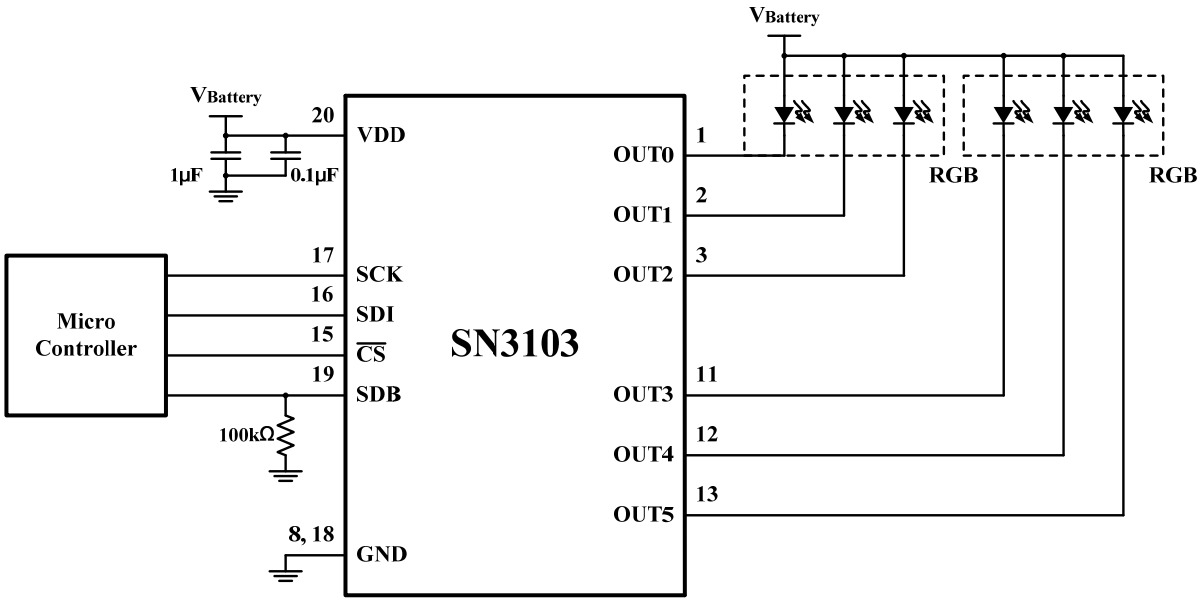
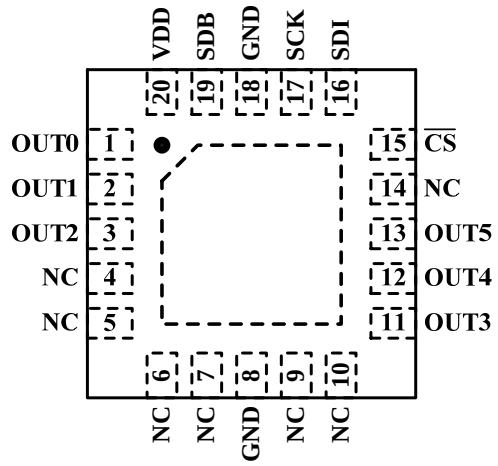


Figure 1 Typical Application Circuit

Pin Configuration

Package	Pin Configuration (Top View)
QFN-20	

Pin Description

No.	Pin	I/O	Description
1~3, 11~13	OUT0 ~ OUT5	O	LED outputs.
4~7,9,10	NC	–	No connection.
15	$\overline{CS}$	I	Active low chip select for serial communications.
16	SDI	I/O	Input serial data for data shift resister.
17	SCK	I	Input Clock for data shift on rising edge.
8, 18	GND	–	Ground.
19	SDB	I	Shutdown, pull to GND in the shutdown mode.
20	VDD	–	Power supply.
	Thermal Pad	–	Connect to GND.

Ordering Information

Order Number	Package Type	QTY/Reel	Operating Temperature Range
SN3103I420E	QFN-20	2500	−40°C ~ +85°C

SN3103 □ □ □ □

Lead Free Code
E: Lead Free

Pin Code
20: 20 Pins

Package Type
4: QFN, 4mm × 4mm

Operating Temperature Range
I: Industrial, −40°C ~ +85°C

Absolute Maximum Ratings

Supply voltage, V_{DD} ---------- −0.3V ~ +6.0V
Storage temperature range ---------- −65°C ~ +150°C
Input voltage ---------- −0.3V ~ V_{DD}+0.3V
Junction temperature ---------- 150°C
Solder Information −Vapor phase (60s) ---------- 215°C
−Infrared (15s) ---------- 220°C
Operating temperature ratings ---------- −40°C ~ +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A = 25°C. *(Note 1)*

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0		5.5	V
I_{DD}	Quiescent power supply current	$V_{SDB} = V_{DD}$		1.4	2.0	mA
I_{SD}	Shutdown current	V_{SDB} = GND		0.4	1.1	μA
	Software shutdown	$V_{SDB} = V_{DD}$		1.7	3.0	μA
I_{OUT}	Average output current	Interface Intensity Control Mode PWM Bytes = 0xFF, V_{DS} = 0.6V OUT0~ OUT5		38.9		mA
V_{HR}	Current sink headroom voltage	I_{LED} = 38.9mA		400.0		mV
SCK, SDI, $\overline{CS}$, SDB Logic Electrical Characteristics						
$V_{IN(0)}$	Logic "0" input voltage	V_{DD} = 3V ~ 5.5V			0.4	V
$V_{IN(1)}$	Logic "1" input voltage	V_{DD} = 3V ~ 5.5V	1.4			V
$I_{IN(0)}$	Logic "0" input current	*(Note 2)*		5.0		nA
$I_{IN(1)}$	Logic "1" input current	*(Note 2)*		5.0		nA

Digital Input Switching Characteristics *(Note 2)*

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{CK}	SCK frequency				1.0	MHz
t_{CH}	SCK high time		200			ns
t_{CL}	SCK low time		200			ns
t_{DH}	SDI setup time		50			ns
t_{DS}	SDI high time		50			ns
t_{CSS}	$\overline{CS}$ to SCK rise setup time		250			ns
t_{CSCP}	$\overline{CS}$ rising edge to SCK rising edge		200			ns
t_{CSH}	$\overline{CS}$ pulse high time		300			ns

Note1: Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

Note2: Guaranteed by design.

Application Information

SPI Interface

The SN3103 contains a 16bit SPI interface to access the internal data and control registers of the device (see Registers Definitions). This module is used to receive the commands transmitted by MCU. The 16-bit serial interface uses three pins, SDI and SCK to enter data. Data read is not available and data entered must be 16 bits. The description of three pins is shown in table 1.

Table 1 Serial Pins

Signal Name	Attribute	Direction	Description
SCK	Edge Triggered	MCU-> SN3103	Serial bus clock
SDI	Level	MCU -> SN3103	Serial data
$\overline{CS}$	Active Low	MCU -> SN3103	SPI bus selection

Table 2 shows the structure of the 16-bit command word and Figure 2 shows the timing diagram of this serial interface. When the SPI block is idle, the MCU must maintain HIGH. For the MCU to transmit data to the SN3103, must be pulled LOW and remain LOW for the duration of the transmission. The first 8 bits are address bits and the remaining 8 bits are data bits.

Initial Power-Up

On initial power-up, the SN3103 registers are reset to their default values, OUT0~OUT5 need to be turned on thru **SDRGB1** bit and **SDRGB2** bit in Configuration Register (00h).

Shutdown Mode

The SN3103 device features a shutdown mode. Shutdown mode is entered via a write to the Configuration Register (see Table 4). In shutdown mode all of the output current sources are switched off. Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode).

Note: During shutdown mode the Digit-Registers maintain their data.

Table 2 16-Bit Serial Data Format

A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB			Register Address (see Table 3)				LSB	MSB			Data				LSB

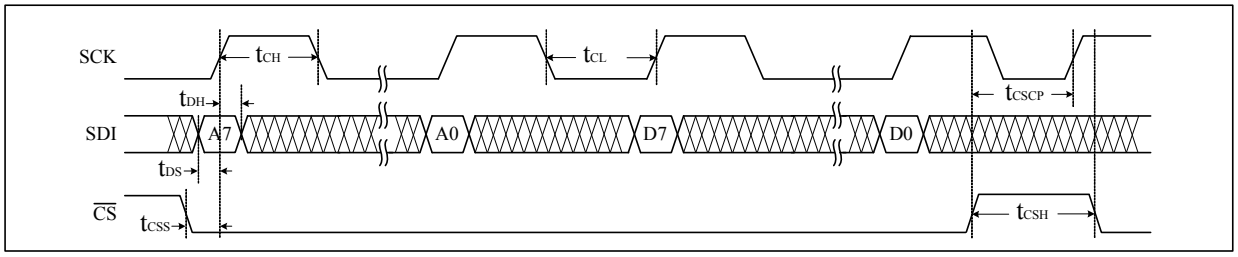


Figure 2 Interface Timing

Registers

The SN3103 device contains 31 Registers, which are listed in Table 3. Communication to the SN3103 via the serial interface consists of an 8-bit address word followed by an 8-bit data word.

Table 3 Register Function Map

Address	Name	Function	Table	Default
00h	Configuration	Configure the operation mode	4	0000 0001
02h	RGB mode	Set RGB mode	5	0000 0000
03h	RGB current	Set RGB current	6	
04h	OUT0_PWM	Set OUT0 PWM duty cycle	7	0000 0000 *(Note 1)*
05h	OUT1_PWM	Set OUT1 PWM duty cycle	7	
06h	OUT2_PWM	Set OUT2 PWM duty cycle	7	
07h	OUT3_PWM	Set OUT3 PWM duty cycle	7	
08h	OUT4_PWM	Set OUT4 PWM duty cycle	7	
09h	OUT5_PWM	Set OUT5 PWM duty cycle	7	
0Ah	OUT0_T0	OUT0 holdoff time	8	0000 0000 *(Note 2)*
0Bh	OUT1_T0	OUT1 holdoff time	8	
0Ch	OUT2_T0	OUT2 holdoff time	8	
0Dh	OUT3_T0	OUT3 holdoff time	8	
0Eh	OUT4_T0	OUT4 holdoff time	8	
0Fh	OUT5_T0	OUT5 holdoff time	8	
10h	OUT0_T1&T2	OUT0 ramping up time and hold time	9	
11h	OUT1_ T1&T2	OUT1 ramping up time and hold time	9	
12h	OUT2_ T1&T2	OUT2 ramping up time and hold time	9	
13h	OUT3_ T1&T2	OUT3 ramping up time and hold time	9	
14h	OUT4_ T1&T2	OUT4 ramping up time and hold time	9	
15h	OUT5_ T1&T2	OUT5 ramping up time and hold time	9	
16h	OUT0_T3&T4	OUT0 ramping down time and off time	10	
17h	OUT1_T3&T4	OUT1 ramping down time and off time	10	
18h	OUT2_T3&T4	OUT2 ramping down time and off time	10	
19h	OUT3_T3&T4	OUT3 ramping down time and off time	10	
1Ah	OUT4_T3&T4	OUT4 ramping down time and off time	10	
1Bh	OUT5_T3&T4	OUT5 ramping down time and off time	10	
1Ch	Update	Update data of register 0Ah~1Bh		xxxx xxxx *(Note 3)*
1Dh	OUT3-0_EN	Enable OUT3~0	11	1xxx x111 *(Note 4)*
1Eh	OUT5-4_EN	Enable OUT5~4	12	11xx xxxx *(Note 4)*
20h	RGB Gain2	Set RGB current	13	00000000

Note:

1. In Interface Intensity Control mode, the PWM duty cycle is defined by input data set in register 04h-09h.

2. In One Shot Programming mode, the PWM duty cycle is defined by T0-T4. T0 is holdoff time.T1 is Gamma-Corrected ramping up time.T2 is hold time.T3 is Gamma-Corrected ramping down time.T4 is off time. (See in figure 3)

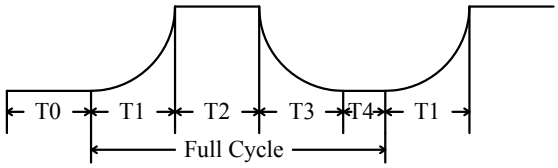


Figure 3 Timing Parameters

3. Write any 8 bit data to the update register after set the value of T0~T4 to update the value of them.

4. In OUT3-0_EN register, OUT3 is controlled by the MSB, OUT0 is controlled by the LSB, D6 thru D3 are reserved. For example, we send 011 1110 1 to OUT3-0_EN register to disable OUT3 and OUT1， but other output channel are enable. In OUT5-4_EN register, D7 controls the OUT5, D6 controls the OUT4.

Table 4 00h Configuration Register

Bit	D7:D6	D5	D4	D3:D1	D0
Name	-	SDRGB1	SDRGB2	-	SSD
Default	00	0	0	000	1

The Configuration Register controls SN3103 two groups RGB outputs and shutdown mode. Notice **SDRGB1** bit and **SDRGB2** bit should be set to 1 to ensure that the outputs are turned on.

SDRGB1 RGB1 (OUT0~OUT2) Enable
0 Disable
1 Enable

SDRGB2 RGB2 (OUT3~OUT5) Enable
0 Disable
1 Enable

SSD Software Shutdown Mode Enable
0 Chip Enable
1 Chip Shutdown

Table 5 02h RGB Mode Register

Bit	D7:D6	D5	D4	D3:D0
Name	-	M_RGB1	M_RGB2	-
Default	00	0	0	0000

The RGB Mode Register selects the operation mode.

M_RGB1 RGB1(OUT0~OUT2) Mode selection
0 Interface Intensity Control Mode
1 One Shot Programming Mode

M_RGB2 RGB2(OUT3~OUT5) Mode Selection
0 Interface Intensity Control Mode
1 One Shot Programming Mode

Table 6. 03h RGB Current Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	RGB1_MAX		RGB2_MAX	
Default	0000	0	0	0	0

Default the outputs each with 38.9mA current capability, they are adjustable. The RGB current register allows the maximum output current to be scaled as indicated in Table above. The SN3103 provides for a maximum current range from as low as 17.5mA to as high as 69.5mA, notice that the 17.5mA is set by register 20h, as shown in Table 13. Care must be taken so as not to exceed the maximum allowable power dissipation for the device.

RGB1_MAX Maximum Current For RGB1 (Typ.)
00 38.9mA
01 46.5mA
10 69.5mA
11 28.5mA

RGB2_MAX Maximum Current For RGB2 (Typ.)
00 38.9mA
01 46.5mA
10 69.5mA
11 28.5mA

Table 7 04h~09h OUTx_PWM Register

Bit	D7:D0
Name	PWM REGISTER
Default	0000 0000

In Interface Intensity Control mode, the PWM duty cycle is defined by input data set in register 04h-09h.

OUT0_PWM register acts when D5 of RGB mode register is set to 0, the value of OUT0_PWM register decides the average output current of OUT0, the average output current may be computed using the formula,

$$I_{OUT} = \frac{38.9mA}{256} * \sum_{n=0}^{7} 2^n$$

Where n stands for the set bit sequence number, for D4, n=4. An example:

D7~D0=10110101,

I_{OUT} =38.9mA×(2^0+2^2+2^4+2^5+2^7)/256

=27.4mA.

See Table 13 in Application Information for more.

OUT1 ~OUT5 PWM register are the same as OUT0 PWM register.

Time Registers

In One Shot Programming mode, the PWM duty cycle is defined by T0-T4.

By programming different values of T0~T4 for the different outputs, OUT0~OUT5, many different combinations LED effects can be created.

The complete waveform period consists of the summation of all times T1~T4.

Table 8 0Ah~0Fh OUTx_T0 Register

Bit	D7:D4	D3:D0
Name	T0	–
Default	0000	0000

T0 is the hold off delay before the waveform (described by the values of T1~T4) begins as shown in Figure 3. The hold off delay occurs only after 1) any 8-bit value is written to the update register (0Ch), or 2) turn on the One Shot Programming mode by programming the RGB Mode Register (02h)

All output T0 registers (0Ah~0Fh) are programmed in the same manner.

T0	Time Delay of Output Current		
0000	0s	0001	0.13s
0010	0.26s	0011	0.52s
0100	1.04s	0101	2.08s
0110	4.16s	0111	8.32s
1000	16.64s	1001	33.28s
1010	66.56s		

Table 9 10h~15h OUTx_T1&T2 Register

Bit	D7:D5	D4:D1	D0
Name	T1	T2	–
Default	000	0000	0

T1: T1 is the time that the output current ramps up to its final value. It is Gamma-Corrected and consists of 32 steps and the PWM duty cycle is increasing at each step as shown in Table 14.

T2: T2 is the time the output holds its maximum current.

All output T1, T2 registers (10h~15h) are programmed in the same manner.

T1	Ramping Up Time		
000	0.13s	001	0.26s
010	0.52s	011	1.04s
100	2.08s	101	4.16s
110	8.32s	111	16.64s

T2	Holding Full Current Time		
0000	0s	0001	0.13s
0010	0.26s	0011	0.52s
0100	1.04s	0101	2.08s
0110	4.16s	0111	8.32s
1000	16.64s		

Table 10. 16h~1Bh OUTn_T1&T2 Register

Bit	D7:D5	D4:D1	D0
Name	T3	T4	–
Default	000	0000	0

T3: T3 is the time that the output current ramps down from the maximum value to zero. It is Gamma-Corrected and consists of 32 steps and the PWM duty cycle is reducing at each step as shown in Table 15.

T4: T4 is the time delay before repeating the next cycle.

All output T3, T4 registers (16h~1Bh) are programmed in the same manner.

T3	Ramping Down Time		
000	0.13s	001	0.26s
010	0.52s	011	1.04s
100	2.08s	101	4.16s
110	8.32s	111	16.64s

T4	Holding Off Time		
0000	0s	0001	0.13s
0010	0.26s	0011	0.52s
0100	1.04s	0101	2.08s
0110	4.16s	0111	8.32s
1000	16.64s	1001	33.28s
1010	66.56s		

1Ch Update Register

Once configured, the timing parameters, T0 thru T4, may only be changed by modifying the values stored in the timing registers (0Ah~1Bh), followed by writing any 8-bit value to the update register. The new timing parameters will take effect following the write to the update register.

Table 11 1Dh O3-0_EN Registers

Bit	D7	D6:D3	D2	D1	D0
Name	O3_EN	–	O2_EN	O1_EN	O0_EN
Default	1	0000	1	1	1

Table 12 1Eh OUT5-4_EN Registers

Bit	D7	D6	D5: D0
Name	O5_EN	O4_EN	–
Default	1	1	000000

Ox_EN Registers control the on or off state of each output.

Ox_EN	Output States
0	Output Off
1	Output On

Table 13 20h RGB Gain2 Register

Bit	D7:D2	D1	D0
Name	–	RGB1_C	RGB2_C
Default	000000	0	0

RGB Gain2 Register makes RGB current on the fifth setting at 17.5mA.

D1 RGB1 Current Setting
1 RGB1 Current is Set To 17.5mA
0 RGB1 Current is Set By REG 03h

D0 RGB2 Current Setting
1 RGB2 Current is Set To 17.5mA
0 RGB2 Current is Set By REG 03h

Constant Current

The maximum current of OUT0 ~ OUT5 are internally set to one of 5 constant current levels (17.5mA, 28.5mA, 38.9mA, 46.5mA or 69.5mA (typical)). The constant current sinks maintain the output current at the programmed level when sinking current.

When set to sink 38.9mA, if the voltage at the output pin falls below 0.4V, because of a large LED forward voltage (V_F) or falling supply voltage, then the output current will begin to fall off as shown in Figure 3. The selection for the constant current level is made by programming the RGB current register as shown in Table 6.

Interface Intensity Control Mode

When configuration register (00h) D5 and D4 are set high, the maximum current of output is selected via RGB current register (03h) bits D3~D0. Outputs operate in Interface Intensity Control mode when you clear the RGB mode register bits D5&D4. In this control mode, you must send data if you want to change the PWM intensity of the RGB LEDs.

The SN3103's PWM LED outputs can be used to drive individual color LEDs or RGB LED modules. When driving an RGB LED module, the intensity of each LED in the module is programmable allowing the RGB LED module to be set to many different colors, based on the value of the PWM byte.

When Interface Intensity Control mode is enabled, the average output current of OUT0~OUT5 is dependent upon the PWM duty cycle. LEDs driven with a higher duty cycle results in a higher luminous intensity. For example, if the maximum output current is 38.9mA, the table below gives some average I_{OUT} values controlled by PWM bytes. The average output current can be adjusted in 256 steps of PWM control.

Table 14 256 Steps Output Current

PMW Byte	I_{OUT} (mA)
0x00	0
0x01	0.15
0x02	0.30
0x03	0.46
… …	… …
0xff	38.90

One Shot Programming Mode

Outputs work in One Shot Programming mode when you set RGB mode register bit D5 to '1'. When the SN3103 is operating in One Shot Programming mode, the output waveform is user configurable by the selection of T0~T4. New values written to T0~T4 will take effect after writing any 8 bits of data to the Update register.

In One Shot Programming mode, the PWM duty cycle is defined by T0-T4.

T0: T0 is the hold off delay before the waveform (described by the values of T1~T4) begins as shown in Figure 3. The hold off delay occurs only after 1) any 8-bit value is written to the update register, or 2) turn on the One Shot Programming mode by programming the RGB Mode Register (02h).

T1: T1 is the time that the output current ramps up to its final value. It is Gamma-Corrected and consists of 32 steps and the PWM duty cycle is increasing at each step as shown in Table 14.

T2: T2 is the time the output holds its maximum current.

T3: T3 is the time that the output current ramps down from the maximum value to zero. It is Gamma-Corrected and consists of 32 steps and the PWM duty cycle is reducing at each step as shown in Table 14.

The ramping up and down time (T1, T3) consists of 32 steps and the PWM duty cycle is increasing or reducing at each step as shown below in Table 14.

T4: T4 is the time delay before repeating the next cycle.

By programming different values of T0~T4 for the different outputs, OUT0~OUT2, many different combinations LED effects can be created.

The complete waveform period consists of the summation of all times T1~T4.

Table 15 Gamma-Corrected PWM Duty Cycle (Gamma = 1.8)

Gray Scale Data	Duty Cycle (1/256)	Gray Scale Data	Duty Cycle (1/256)
0	0	16	85
1	1	17	95
2	3	18	105
3	5	19	115
4	8	20	125
5	12	21	136
6	16	22	148
7	21	23	160
8	26	24	172
9	32	25	185
10	38	26	198
11	45	27	211
12	52	28	225
13	60	29	239
14	68	30	254
15	76	31	256

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

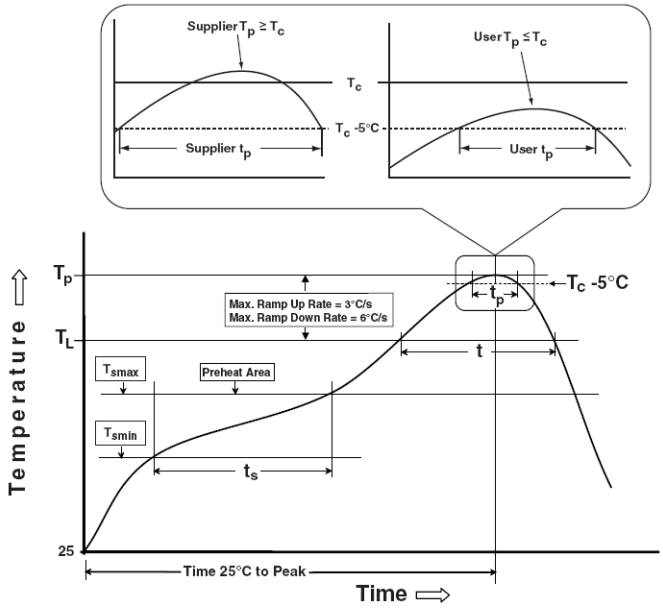
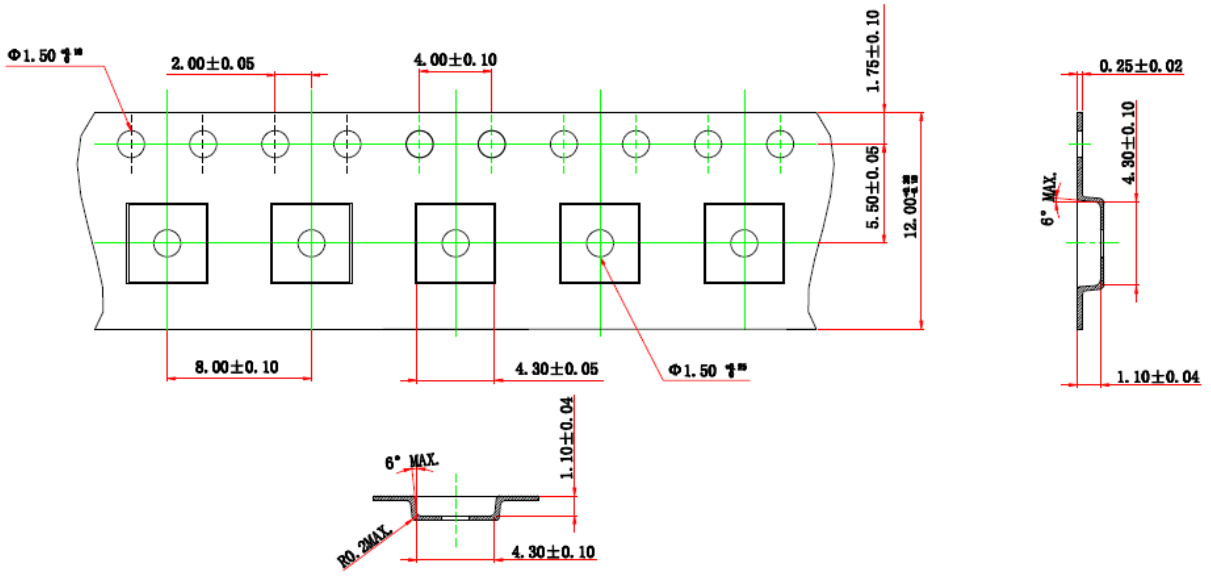


Figure 4 Classification Profile

Tape and Reel Information

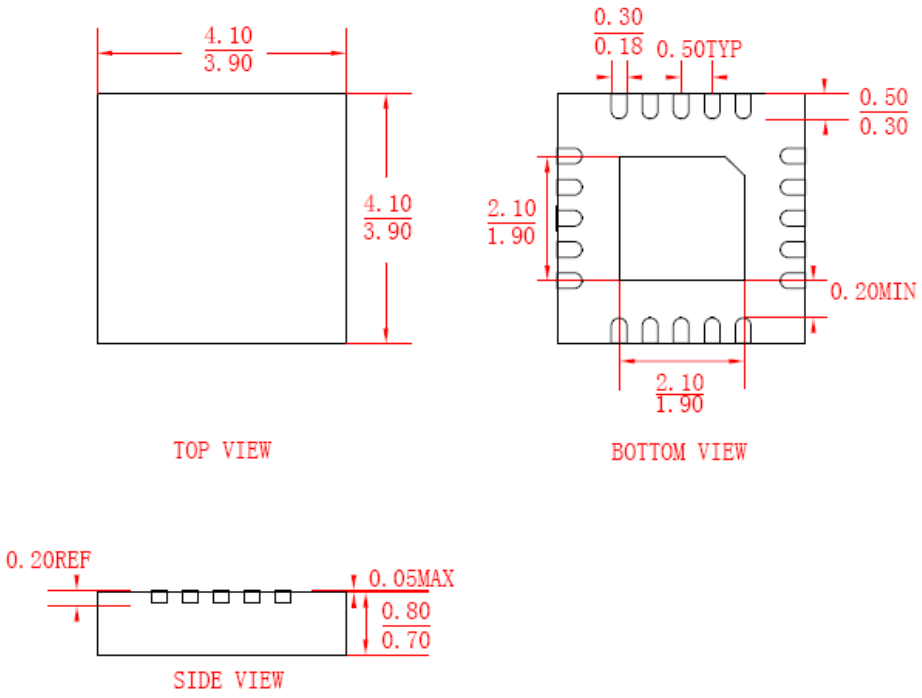


NOTES:[技术要求]:

1.CARRIER TAPE COLOR: BLACK[载带颜色为黑色]
2.COVER TAPE WIDTH:9.50±0.10 [配套9.5±0.10宽盖带]
3.COVER TAPE COLOR:TRANSPARENT[盖带颜色无色透明]
4. ANTISTATIC COATED 10^{8}~ 10^{11}OHMS/SQ.[单位面积表面阻抗为$10^{8}\Omega$/□~$10^{11}\Omega$/□]
5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
[10个传送定位孔间距累积公差0.20MAX.]
6.SUPPLIER:3M[供应商3M]
7.MOLD# W8P8P(4×4×0.75/0.85)[载带规格W8P8P(4×4×0.75/0.85)]
8.ALL DIMS IN mm.[所有单位为mm]
9.SAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.
[禁止使用长电科技规定的一级环境管理物质]
10.THE DERECTION OF VIEW: ⊣◎。[视图方向:⊣◎]
11.SPECIAL FOR CUSTOMER SI-EN [矽恩客户专用]

Package Information

QFN-20



Note: All dimensions in millimeters unless otherwise stated.