±1°C Accurate, Remote Diode and Local Digital Temperature Sensor with Two-Wire Interface and Beta Compensation

Description

The SN1086 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) serial interface. The SN1086 accurately measures its own temperature as well as the temperature of an external device, such as processor thermal diode or diode connected transistor such as the MMBT3904. The temperature of any ASIC can be accurately determined using the SN1086 as long as a dedicated diode (semiconductor junction) is available on the target die. The SN1086 has an offset register to allow measuring other diodes without requiring continuous software management.

Activation of the $\overline{\text{ALERT}}$ output occurs when any temperature goes outside a preprogrammed window set by the HIGH and LOW temperature limit registers or exceeds the T_CRIT temperature limit. Activation of the $\overline{\text{T\_CRIT\_A}}$ occurs when any temperature exceeds the T_CRIT programmed limit.

Key Specifications

- Supply voltage ------------------------- 3.0V ~ 3.6V
- Supply current ------------------------ 450μA (Typ.)
- Local temp accuracy (includes quantization error)
  T_A = 25°C ~ 125°C ------------------- ±3.0°C (Max.)
  T_A = −40°C ~ 25°C ------------------- ±5.0°C (Max.)
- Remote diode temp accuracy (includes quantization error)
  T_A = 30°C ~ 50°C, T_D = 60°C ~ 100°C ------- ±1.0°C (max)
  T_A = 0°C ~ 85°C, T_D = 25°C ~ 125°C -------- ±3.0°C (max)
  T_A = −40°C ~ 0°C, T_D = −55°C ~ 0°C -------- ±5.0°C (max)

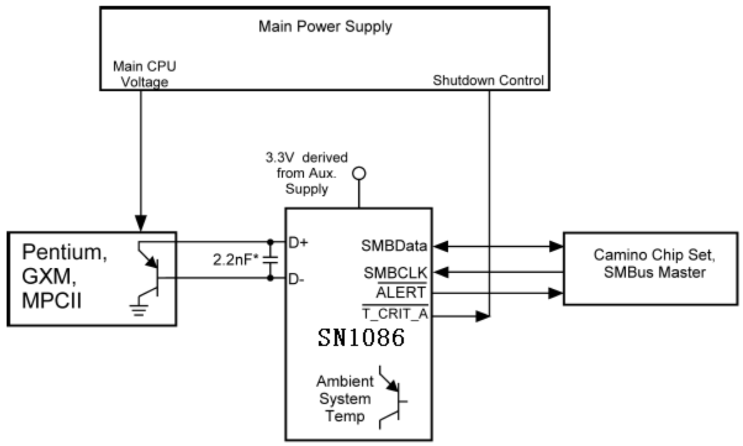
Features

- Support for diodes requiring the BJT/transistor model——supports 45nm, 65nm, and 90nm CPU thermal diodes.
- Accurately senses die temperature of remote ICs or diode junctions
- Offset register allows sensing a variety of thermal diodes accurately
- On-board local temperature sensing
- 10 bits plus sign remote diode temperature data format, 0.125°C resolution
- $\overline{\text{T\_CRIT\_A}}$ output useful for system shutdown
- $\overline{\text{ALERT}}$ output supports SMBus 2.0 protocol
- SMBus 2.0 compatible interface, supports TIMEOUT
- MSOP-8 packages

Applications

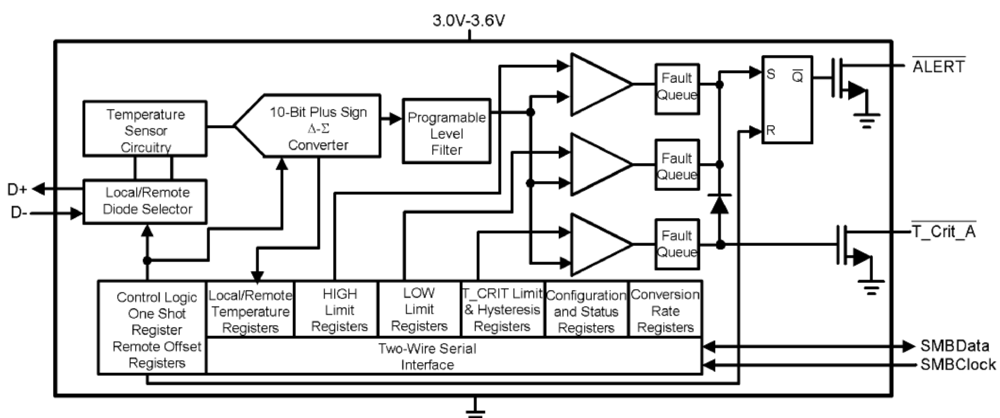
- System thermal management
- Computers
- Electronic test equipment
- Office electronics
- HVAC

Typical Application

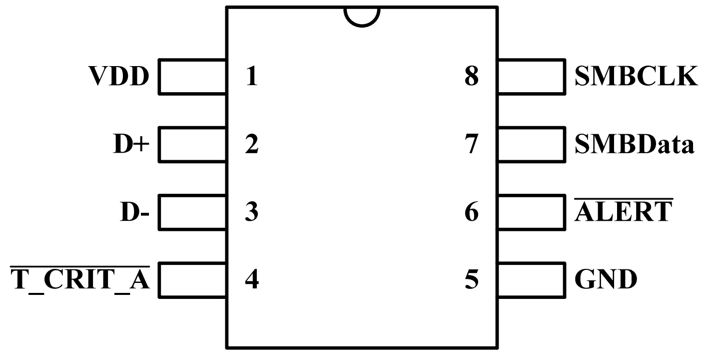


*Note:2.2nF Capacitor must be placed as close as possible to D+ and D- pins of the SN1086.

Simplified Block Diagram



Pin Configuration

Package	Pin Configuration (Top View)
MSOP-8	

Ordering Information

Order Number	Package Type	Operating Temp. Range	Measure Temp. Range
SN1086MIR1	MSOP-8	−40°C ~+125°C	−55°C ~+125°C

Pin Description

No.	Pin	Description	Typical Connection
1	V_{DD}	Positive supply voltage input	DC voltage from 3.0V to 3.6V.
2	D+	Diode current source	To diode anode. Connected to remote discrete diode connected transistor junction or to the diode connected transistor junction on a remote IC whose die temperature is being sensed.
3	D−	Diode return current sink	To diode cathode.
4	$\overline{\text{T\_CRIT\_A}}$	T_CRIT alarm output, open-drain, active-low	Pull-up resistor, controller interrupt or power supply shutdown control.
5	GND	Power supply ground	Ground.
6	$\overline{\text{ALERT}}$	Interrupt output, open-drain, active-low	Pull-up resistor, controller interrupt or alert line.
7	SMBData	SMBus bi-directional data line, open-drain output	From and to controller, pull-up resistor.
8	SMBCLK	SMBus input	From controller, pull-up resistor.

Absolute Maximum Ratings *(Note 1)*

Supply voltage, V_{DD} ---------- −0.3V ~ +6.0V
Voltage at SMBData, SMBCLK, $\overline{\text{ALERT}}$, $\overline{\text{T\_CRIT\_A}}$ ---------- −0.5V ~ +6.0V
Voltage at other pins ---------- .−0.3V ~ V_{DD} + 0.3V
D− input current ---------- ±1mA
Input current at all other pins *(Note2)* ---------- ±5mA
Package input current *(Note 2)* ---------- 30mA
SMBData, $\overline{\text{ALERT}}$, $\overline{\text{T\_CRIT\_A}}$ output sink current ---------- 10mA
Storage temperature range ---------- −65°C ~ +150°C
Soldering information, lead temperature, Vapor Phase (60s) ---------- 215°C
Infrared (15s) ---------- 220°C
ESD susceptibility *(Note 3)*, Human Body Model ---------- 2kV
Machine Model ---------- 200V
Operating temperature range ---------- −40°C ~ +125°C

Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 3.0V ~ 3.6V.
Boldface limits apply for $T_A = T_J = T_{MIN} \le T_A \le T_{MAX}$. All other limits $T_A = T_J$ = +25°C, unless otherwise noted.

Parameter	Condition	Typ. *(Note 5)*	Limit	Unit
Temperature error using local diode	T_A = +25°C ~ +125°C *(Note 6)*	±1	±3	°C (Max.)
	T_A = −40°C ~ +25°C *(Note 6)*		±5	
Temperature error using remote diode of mobile Pentium iii with typical non-ideality of 1.008. (T_D is the remote diode junction temperature)	T_A = +30°C ~ +50°C T_D = +60°C~ +100°C		±1	°C (Max.)
	T_A = +0°C ~ +85°C T_D = +25°C ~ +125°C		±3	°C (Max.)
	T_A = −40°C ~ 0°C T_D = −55°C ~ 0°C		±5	°C (Max.)
Remote diode measurement resolution		11		Bits
		0.125		°C
Local diode measurement resolution		8		Bits
		1		°C
Conversion time of all temperatures at the fastest setting	*(Note 8)*	125	156	ms (Max.)
Quiescent current *(Note 7)*	SMBus Inactive, 16Hz conversion rate	0.45	1	mA (Max.)
	Shutdown	1.5		μA
D− source voltage		0.7		V
Diode source current	(D+ − D−) = +0.65V; high level	100	120	μA (Max.)
			80	μA (Min.)
	Low level	10	12	μA (Max.)
			8	μA (Min.)

Temperature-to-Digital Converter Characteristics (Continued)

Unless otherwise noted, these specifications apply for V_{DD} = 3.0V ~ 3.6V.
Boldface limits apply for $T_A = T_J = T_{MIN} \leq T_A \leq T_{MAX}$. All other limits $T_A = T_J$ = +25°C, unless otherwise noted.

Parameter	Condition	Typ. *(Note 5)*	Limit	Unit
$\overline{\text{ALERT}}$ and $\overline{\text{T\_CRIT\_A}}$ output saturation voltage	I_{OUT} = 6.0mA		0.4	V (max)
Power-on reset threshold	Measure on V_{DD} input, falling edge		2.4 1.8	V (max) V (min)
Local and remote high default temperature settings	(Note 9)	+70		°C
Local and remote low default temperature settings	(Note 9)	0		°C
Local and remote T_CRIT default temperature setting	(Note 9)	85		°C

Logic Electrical Characteristics

Digital DC Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 3.0V ~ 3.6V.
Boldface limits apply for $T_A = T_J = T_{MIN} \leq T_A \leq T_{MAX}$. All other limits $T_A = T_J$ = +25°C, unless otherwise noted.

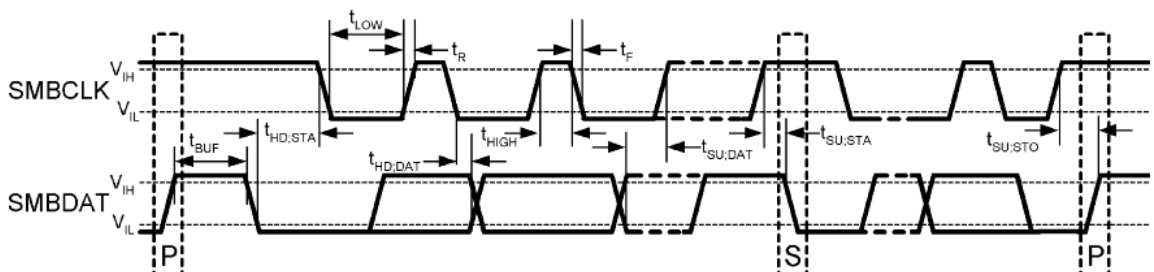
Symbol	Parameter	Condition	Typ. *(Note 5)*	Limit	Unit
SMBData, SMBCLK Inputs					
$V_{IN(1)}$	Logical "1" input voltage			2.1	V (min)
$V_{IN(0)}$	Logical "0"input voltage			0.4	V (max)
$V_{IN(HYST)}$	SMBData and SMBCLK digital input hysteresis		400		mV
$I_{IN(1)}$	Logical "1" input current	$V_{IN} = V_{DD}$	0.005	±10	µA (max)
$I_{IN(0)}$	Logical "0" input current	V_{IN} = 0 V	−0.005	±10	µA (max)
C_{IN}	Input capacitance		5		pF
All Digital Outputs					
I_{OH}	High level output current	$V_{OH} = V_{DD}$		10	µA (max)
V_{OL}	SMBus low level output voltage	I_{OL} = 4mA I_{OL} = 6mA		0.4 0.6	V (max)

SMBus Digital Switching Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 3.0V ~ 3.6V.
Boldface limits apply for $T_A = T_J = T_{MIN} \leq T_A \leq T_{MAX}$. All other limits $T_A = T_J$ = +25°C, unless otherwise noted.
The switching characteristics of the SN1086 fully meet or exceed the published specifications of the SMBus version 2.0.
The following parameters are the timing relationships between SMBCLK and SMBData signals related to the SN1086.
They adhere to but are not necessarily the SMBus bus specifications.

Symbol	Parameter	Condition	Typ. (Note 5)	Limit	Unit
f_{SMB}	SMBus clock frequency			100 10	kHz(max) kHz (min)
t_{LOW}	SMBus clock low time	from $V_{IN(0)}$ max to $V_{IN(0)}$ max		4.7 25	µs (min) ms(max)
t_{HIGH}	SMBus Clock High Time	from $V_{IN(1)}$min to $V_{IN(1)}$ min		4.0	µs (min)
$t_{R,SMB}$	SMBus Rise Time	(Note 10)	1		µs(max)
$t_{F,SMB}$	SMBus Fall Time	(Note 11)	0.3		µs(max)
t_{OF}	Output Fall Time	C_L = 400pF, I_O = 3mA (Note 11)		250	ns (max)
$t_{TIMEOUT}$	SMBData and SMBCLK Time Low for Reset of Serial Interface (Note 12)			25 35	ms (min) ms(max)
$t_{SU;STA}$	Data In Setup Time to SMBCLK High			250	ns (min)
$t_{HD;DAT}$	Data Out Stable after SMBCLK Low			300 900	ns (min) ns (max)
$t_{HD;STA}$	Start Condition SMBData Low to SMBCLK Low (Start condition hold before the first clock falling edge)			100	ns (min)
$t_{SU;STO}$	Stop Condition SMBCLK High to SMBData Low (Stop Condition Setup)			100	ns (min)
$t_{SU;STA}$	SMBus Repeated Start-Condition Setup Time, SMBCLK High to SMBData Low			0.6	µs (min)
t_{BUF}	SMBus Free Time Between Stop and Start Conditions			1.3	µs (min)

SMBus Communication



Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: When the input voltage (V_I) at any pin exceeds the power supplies (V_I< GND or $V_I > V_{DD}$), the current at that pin should be limited to 5 mA.

Parasitic components and or ESD protection circuitry are shown in the figure below for the SN1086's pins. The nominal breakdown voltage of D3 is 6.5 V. Care should be taken not to forward bias the parasitic diode, D1, present on pins: D+, D-. Doing so by more than 50 mV may corrupt a temperature measurement.

Pin Name	PIN #	D1	D2	D3	D4	D5	D6	D7	R1	SNP	ESD CLAMP
V_{DD}	1										x
D+	2	x	x				x	x	x		x
D−	3	x	x			x	x	x			x
$\overline{\text{T\_CRIT\_A}}$	4							x	x	x	
$\overline{\text{ALERT}}$	6							x	x	x	
SMBData	7							x	x	x	
SMBCLK	8									x	

Note: An "x" indicates that the diode exists.

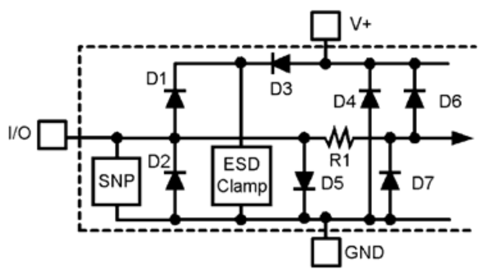


Figure 1 ESD Protection Input Structure

Note 3: Human body model, 100pF discharged through a 1.5k resistor. Machine model, 200pF discharged directly into each pin.

Note 4: Thermal resistance junction-to-ambient when attached to a printed circuit board with 2 oz. foil:

– MSOP-8 = 210°C/W

Note 5: Typically are at T_A= 25°C and represent most likely parametric norm.

Note 6: Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the SN1086 and the thermal resistance. See (Note 4) for the thermal resistance to be used in the self-heating calculation.

Note 7: Quiescent current will not increase substantially with an SMBus.

Note 8: This specification is provided only to indicate how often temperature data is updated. The SN1086 can be read at any time without regard to conversion state (and will yield last conversion result).

Note 9: Default values set at power up.

Note 10: The output rise time is measured from ($V_{IN(0)}$max + 0.15V) to ($V_{IN(1)}$min − 0.15V).

Note 11: The output fall time is measured from ($V_{IN(1)}$min -0.15V) to ($V_{IN(1)}$min + 0.15V).

Note 12: Holding the SMBData and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the SN1086's SMBus state machine, therefore setting SMBData and SMBCLK pins to a high impedance state.

1.0 Functional Description

The SN1086 temperature sensor incorporates a delta V_{BE} based temperature sensor using a Local or Remote diode and a 10-bit plus sign ADC (Delta-Sigma Analog-to-Digital Converter). The SN1086 is compatible with the serial SMBus version 2.0 two-wire interface. Digital comparators compare the measured Local Temperature (LT) to the Local High (LHS), Local Low (LLS) and Local T_CRIT (LCS) user-programmable temperature limit registers. The measured Remote Temperature (RT) is digitally compared to the Remote High (RHS), Remote Low (RLS) and Remote T_CRIT (RCS) user-programmable temperature limit registers. Activation of the $\overline{\text{ALERT}}$ output indicates that a comparison is greater than the limit preset in a T_CRIT or HIGH limit register or less than the limit preset in a LOW limit register. The $\overline{\text{T\_CRIT\_A}}$ output responds as a true comparator with built in hysteresis. The hysteresis is set by the value placed in the Hysteresis register (TH). Activation of $\overline{\text{T\_CRIT\_A}}$ occurs when the temperature is above the T_CRIT setpoint. $\overline{\text{T\_CRIT\_A}}$ remains activated until the temperature goes below the setpoint calculated by T_CRIT - TH. The hysteresis register impacts both the remote temperature and local temperature readings.

The SN1086 may be placed in a low power consumption (Shutdown) mode by setting the $\overline{\text{RUN}}$/STOP bit found in the Configuration register. In the Shutdown mode, the SN1086's SMBus interface remains while all circuitry not required is turned off.

The Local temperature reading and setpoint data registers are 8-bits wide. The format of the 11-bit remote temperature data is a 16-bit left justified word. Two 8-bit registers, high and low bytes, are provided for each setpoint as well as the temperature reading. Two offset registers (RTOLB and RTOHB) can be used to compensate for non_ideality error, discussed further in Section 3.1 DIODE NON-IDEALITY. The remote temperature reading reported is adjusted by subtracting from or adding to the actual temperature reading the value placed in the offset registers.

1.1 Conversion Sequence

The SN1086 takes approximately 125 ms to convert the Local Temperature (LT), Remote Temperature (RT), and to update all of its registers. Only during the conversion process the busy bit (D7) in the Status register (02h) is high. These conversions are addressed in a round robin sequence. The conversion rate may be modified by the Conversion Rate Register (04h). When the conversion rate is modified a delay is inserted between conversions, the actual conversion time remains at 125ms. Different conversion rates will cause the SN1086 to draw different amounts of supply current as shown in Figure 2

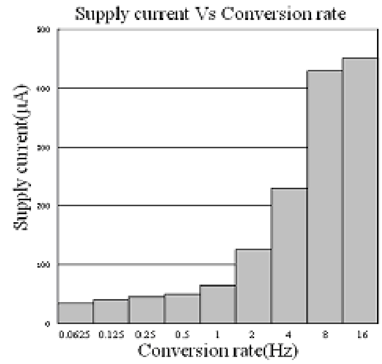


Figure 2 Conversion Rate Effect On Power Supply Current

1.2 The $\overline{\text{ALERT}}$ Output

The SN1086's $\overline{\text{ALERT}}$ pin is an active-low open-drain output that is triggered by a temperature conversion that is outside the limits defined by the temperature setpoint registers. Reset of the $\overline{\text{ALERT}}$ output is dependent upon the selected method of use. The SN1086's $\overline{\text{ALERT}}$ pin is versatile and will accommodate three different methods of use to best serve the system designer: as a temperature comparator, as a temperature based interrupt flag, and as part of an SMBus ALERT system. The three methods of use are further described below. The ALERT and interrupt methods are different only in how the user interacts with the SN1086.

Each temperature reading (LT and RT) is associated with a T_CRIT setpoint register (LCS, RCS), a HIGH setpoint register (LHS and RHS) and a LOW setpoint register (LLS and RLS). At the end of every temperature reading, a digital comparison determines whether that reading is above its HIGH or T_CRIT setpoint or below its LOW setpoint. If so, the corresponding bit in the STATUS REGISTER is set. If the ALERT mask bit is not high, any bit set in the STATUS REGISTER, with the exception of Busy (D7) and OPEN (D2), will cause the $\overline{\text{ALERT}}$ output to be pulled low. Any temperature conversion that is out of the limits defined by the temperature setpoint registers will trigger an ALERT. Additionally, the ALERT mask bit in the Configuration register must be cleared to trigger an ALERT in all modes.

1.2.1 $\overline{\text{ALERT}}$ Output as a Temperature Comparator

When the SN1086 is implemented in a system in which it is not serviced by an interrupt routine, the $\overline{\text{ALERT}}$ output could be used as a temperature comparator. Under this method of use, once the condition that triggered the $\overline{\text{ALERT}}$ to go low is no longer present, the $\overline{\text{ALERT}}$ is de-asserted (Figure 3). For example, if the $\overline{\text{ALERT}}$ output was activated by the comparison of LT > LHS, when this condition is no longer true the $\overline{\text{ALERT}}$ will return HIGH. This mode allows operation without software intervention, once all registers are configured during set-up. In order for the $\overline{\text{ALERT}}$ to be used as a temperature comparator, bit D0 (the $\overline{\text{ALERT}}$ configure bit) in the FILTER and ALERT CONFIGURE REGISTER (xBF) must be set high. This is not the power on default default state.

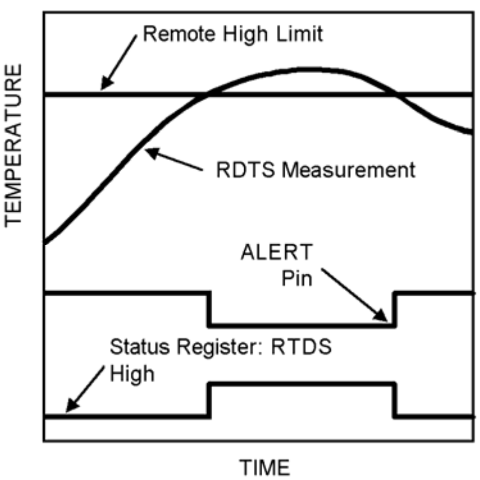


Figure 3 $\overline{\text{ALERT}}$ Comparator Temperature Response Diagram

1.2.2 $\overline{\text{ALERT}}$ Output as an Interrupt

The SN1086's $\overline{\text{ALERT}}$ output can be implemented as a simple interrupt signal when it is used to trigger an interrupt service routine. In such systems it is undesirable for the interrupt flag to repeatedly trigger during or before the interrupt service routine has been completed. Under this method of operation, during a read of the STATUS REGISTER the SN1086 will set the ALERT mask bit (D7 of the Configuration register) if any bit in the STATUS REGISTER is set, with the exception of Busy (D7) and OPEN (D2). This prevents further $\overline{\text{ALERT}}$ triggering until the master has reset the ALERT mask bit, at the end of the interrupt service routine. The STATUS REGISTER bits are cleared only upon a read command from the master (see Figure 4) and will be re-asserted at the end of the next conversion if the triggering condition(s) persist(s). In order for the $\overline{\text{ALERT}}$ to be used as a dedicated interrupt signal, bit D0 (the $\overline{\text{ALERT}}$ configure bit) in the FILTER and ALERT CONFIGURE REGISTER (xBF) must be set low. This is the power on default state.

The following sequence describes the response of a system that uses the $\overline{\text{ALERT}}$ output pin as a interrupt flag:

1. Master Senses $\overline{\text{ALERT}}$ low
2. Master reads the SN1086 STATUS REGISTER to determine what caused the $\overline{\text{ALERT}}$
3. SN1086 clears STATUS REGISTER, resets the $\overline{\text{ALERT}}$ HIGH and sets the ALERT mask bit (D7 in the Configuration register).
4. Master attends to conditions that caused the $\overline{\text{ALERT}}$ to be triggered. The fan is started; setpoint limits are adjusted, etc.
5. Master resets the $\overline{\text{ALERT}}$ mask (D7 in the Configuration register).

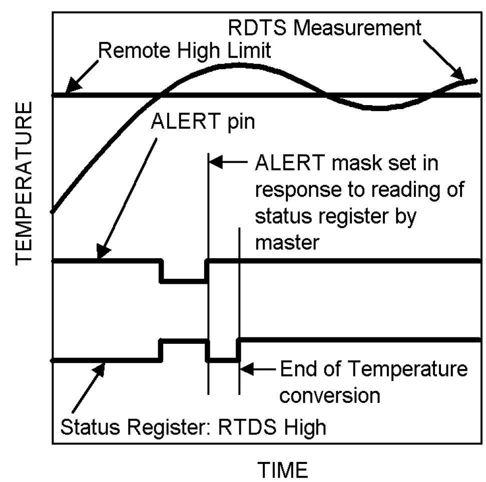


Figure 4 $\overline{\text{ALERT}}$ Output as an Interrupt Temperature Response diagram

1.2.3 $\overline{\text{ALERT}}$ Output as an SMBus Alert

When the $\overline{\text{ALERT}}$ output is connected to one or more $\overline{\text{ALERT}}$ outputs of other SMBus compatible devices and to a master, an SMBus alert line is created. Under this implementation, the SN1086's ALERT should be operated using theARA(Alert Response Address) protocol. The SMBus 2.0 ARA protocol, defined in the SMBus specification 2.0, is a procedure designed to assist the master in resolving which part generated an interrupt and service that interrupt while impeding system operation as little as possible.

The SMBus alert line is connected to the open-drain ports of all devices on the bus thereby AND'ing them together. The ARA is a method by which with one command the SMBus master may identify which part is pulling the SMBus alert line LOW and prevent it from pulling it LOW again for the same triggering condition. When an ARA command is received by all devices on the bus, the devices pulling the SMBus alert line LOW, first, send their address to the master and second, release the SMBus alert line after recognizing a successful transmission of their address.

The SMBus 1.1 and 2.0 specifications state that in response to an ARA (Alert Response Address) "after acknowledging the slave address the device must disengage its $\overline{\text{SMBALERT}}$ pulldown". Furthermore, "if the host still sees $\overline{\text{SMBALERT}}$ low when the message transfer is complete, it knows to read the ARA again". This SMBus "disengaging of $\overline{\text{SMBALERT}}$" requirement prevents locking up the SMBus alert line. Competitive parts may address this "disengaging of $\overline{\text{SMBALERT}}$" requirement differently than the SN1086 or not at all. SMBus systems that implement the ARA protocol as suggested for the SN1086 will be fully compatible with all competitive parts.

The SN1086 fulfills "disengaging of $\overline{\text{SMBALERT}}$" by setting the ALERT mask bit (bit D7 in the Configuration register, at address 09h) after successfully sending out its address in response to an ARA and releasing the $\overline{\text{ALERT}}$ output pin. Once the $\overline{\text{ALERT}}$ mask bit is activated, the $\overline{\text{ALERT}}$ output pin will be disabled until enabled by software. In order to enable the $\overline{\text{ALERT}}$ the master must read the STATUS REGISTER, at address 02h, during the interrupt service routine and then reset the ALERT mask bit in the Configuration register to 0 at the end of the interrupt service routine.

The following sequence describes the ARA response protocol.

1. Master Senses SMBus alert line low

2. Master sends a START followed by the Alert Response Address (ARA) with a Read Command.

3. Alerting Device(s) send ACK.

4. Alerting Device(s) send their Address. While transmitting their address, alerting devices sense whether their address has been transmitted correctly. (The SN1086 will reset its $\overline{\text{ALERT}}$ output and set the ALERT mask bit once Its complete address has been transmitted successfully.)

5. Master/slave NoACK

6. Master sends STOP

7. Master attends to conditions that caused the $\overline{\text{ALERT}}$ to be triggered. The STATUS REGISTER is read and fan started, setpoint limits adjusted, etc.

8. Master resets the ALERT mask (D7 in the Configuration register).

The ARA, 000 1100, is a general call address. No device should ever be assigned this address.

Bit D0 (the $\overline{\text{ALERT}}$ configure bit) in the FILTER and ALERT CONFIGURE REGISTER (xBF) must be set low in order for the SN1086 to respond to the ARA command.

The $\overline{\text{ALERT}}$ output can be disabled by setting the ALERT mask bit, D7, of the Configuration register. The power on default is to have the ALERT mask bit and the $\overline{\text{ALERT}}$ configure bit low.

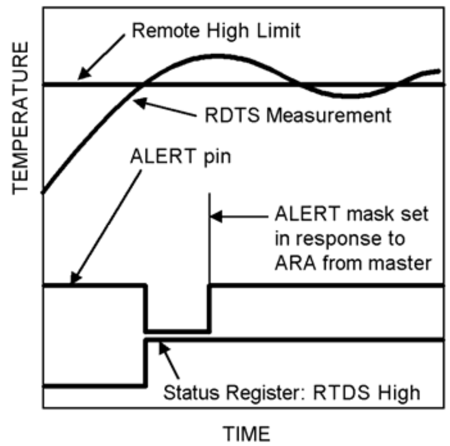


Figure 5 $\overline{\text{ALERT}}$ Output as an SMBus ALERT Temperature Response Diagram

1.3 $\overline{\text{T\_CRIT\_A}}$ Output and T_CRIT Limit

$\overline{\text{T\_CRIT\_A}}$ is activated when any temperature reading is greater than the limit preset in the critical temperature setpoint register (T_CRIT), as shown in Figure 6. The Status Register can be read to determine which event caused the alarm. A bit in the Status Register is set high to indicate which temperature reading exceeded the T_CRIT setpoint temperature and caused the alarm, see Section 2.3.

Local and remote temperature diodes are sampled in sequence by the A/D converter. The $\overline{\text{T\_CRIT\_A}}$ output and the Status Register flags are updated after every Local and Remote temperature conversion. $\overline{\text{T\_CRIT\_A}}$ follows the state of the comparison, it is reset when the temperature falls below the setpoint RCS-TH. The Status Register flags are reset only after the Status Register is read and if a temperature conversion(s) is/are below the T_CRIT setpoint, as shown in. Figure 6

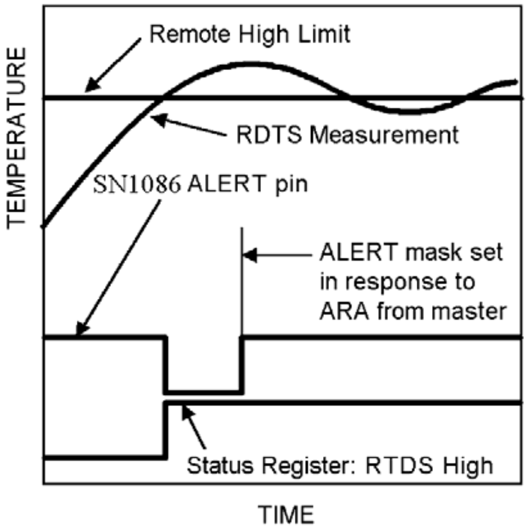


Figure 6 T_CRIT_A Temperature Response Diagram

1.4 Power On Reset Default States

SN1086 always powers up to these known default states. The SN1086 remains in these states until after the first conversion.

1. Command Register set to 00h
2. Local Temperature set to 0˚C
3. Remote Diode Temperature set to 0˚C until the end of the first conversion.
4. Status Register set to 00h.
5. Configuration register set to 00h; $\overline{\text{ALERT}}$ enabled, Remote T_CRIT alarm enabled and Local T_CRIT alarm enabled
6. 85˚C Local and Remote T_CRIT temperature setpoints
7. 70˚C Local and Remote HIGH temperature setpoints
8. 0˚C Local and Remote LOW temperature setpoints
9. Filter and Alert Configure Register set to 00h; filter disabled, $\overline{\text{ALERT}}$ output set as an SMBus ALERT
10. Conversion Rate Register set to 8h; conversion rate set to 16 conv./sec.

1.5 SMBus Interface

The SN1086 operates as a slave on the SMBus, so the SMBCLK line is an input and the SMBData line is bi-directional. The SN1086 never drives the SMBCLK line and it does not support clock stretching. According to SMBus specifications, the SN1086 has a 7-bits lave address. All bits A6 through A0 are internally programmed and can not be changed by software or hardware.

The complete slave address is:

A6	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	0

1.6 Temperature Data Format

Temperature data can only be read from the Local and Remote Temperature registers; the setpoint registers (T_CRIT, LOW, HIGH) are read/write.

Remote temperature data is represented by an 11-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.125˚C. The data format is a left justified 16-bit word available in two 8-bit registers:

Temperature	Digital Output	
	Binary	Hex
+125˚C	0111 1101 0000 0000	7D00h
+25˚C	0001 1001 0000 0000	1900h
+1˚C	0000 0001 0000 0000	0100h
+0.125˚C	0000 0000 0010 0000	0020h
0˚C	0000 0000 0000 0000	0000h
−0.125˚C	1111 1111 1110 0000	FFE0h
−1˚C	1111 1111 0000 0000	FF00h
−25˚C	1110 0111 0000 0000	E700h
−55˚C	1100 1001 0000 0000	C900h

Local Temperature data is represented by an 8-bit, two's complement byte with an LSB (Least Significant Bit) equal to 1˚C:

Temperature	Digital Output	
	Binary	Hex
+125˚C	0111 1101	7Dh
+25˚C	0001 1001	19h
+1˚C	0000 0001	01h
0˚C	0000 0000	00h
−1˚C	1111 1111	FFh
−25˚C	1110 0111	E7h
−55˚C	1100 1001	C9h

1.7 Open-Drain Outputs

The SMBData, $\overline{\text{ALERT}}$ and $\overline{\text{T\_CRIT\_A}}$ outputs are open-drain outputs and do not have internal pull-ups. A "high" level will not be observed on these pins until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible. This will minimize any internal temperature reading errors due to internal heating of the SN1086. The maximum resistance of the pull-up to provide a 2.1V high level, based on SN1086 specification for High Level Output Current with the supply voltage at 3.0V, is 82kΩ(5%) or 88.7kΩ(1%).

1.8 Diode Fault Detection

The SN1086 is equipped with operational circuitry designed to detect fault conditions concerning the remote diode. In the event that the D+ pin is detected as shorted to V_{DD} or floating, the Remote Temperature High Byte (RTHB) register is loaded with +127˚C, the Remote Temperature Low Byte (RTLB) register is loaded with 0, and the OPEN bit (D2) in the status register is set. As a result, if the Remote T_CRIT setpoint register (RCS) is set to a value less than +127˚C the $\overline{\text{ALERT}}$ and T_Crit output pins will be pulled low, if the Alert Mask and T_Crit Mask are disabled. If the Remote HIGH Setpoint High Byte Register (RHSHB) is set to a value less than +127˚C then $\overline{\text{ALERT}}$ will be pulled low, if the Alert Mask is disabled. The OPEN bit itself will not trigger and ALERT.

In the event that the D+ pin is shorted to ground or D−, the Remote Temperature High Byte (RTHB) register is loaded with −128˚C (1000 0000) and the OPEN bit (D2) in the status register will not be set. Since operating the SN1086 at −128˚C is beyond it's operational limits, this temperature reading represents this shorted fault condition. If the value in the Remote Low Setpoint High Byte Register (RLSHB) is more than −128˚C and the Alert Mask is disabled, $\overline{\text{ALERT}}$ will be pulled low.

Remote diode temperature sensors that have been previously released and are competitive with the SN1086 output a code of 0˚C if the external diode is short-circuited. This change is an improvement that allows a reading of 0˚C to be truly interpreted as a genuine 0˚C reading and not a fault condition.

1.9 Communicating with the SN1086

The data registers in the SN1086 are selected by the Command Register. At power-up the Command Register is set to "00", the location for the Read Local Temperature Register. The Command Register latches the last location it was set to. Each data register in the SN1086 falls into one of four types of user accessibility:

1. Read only
2. Write only
3. Read/Write same address
4. Read/Write different address

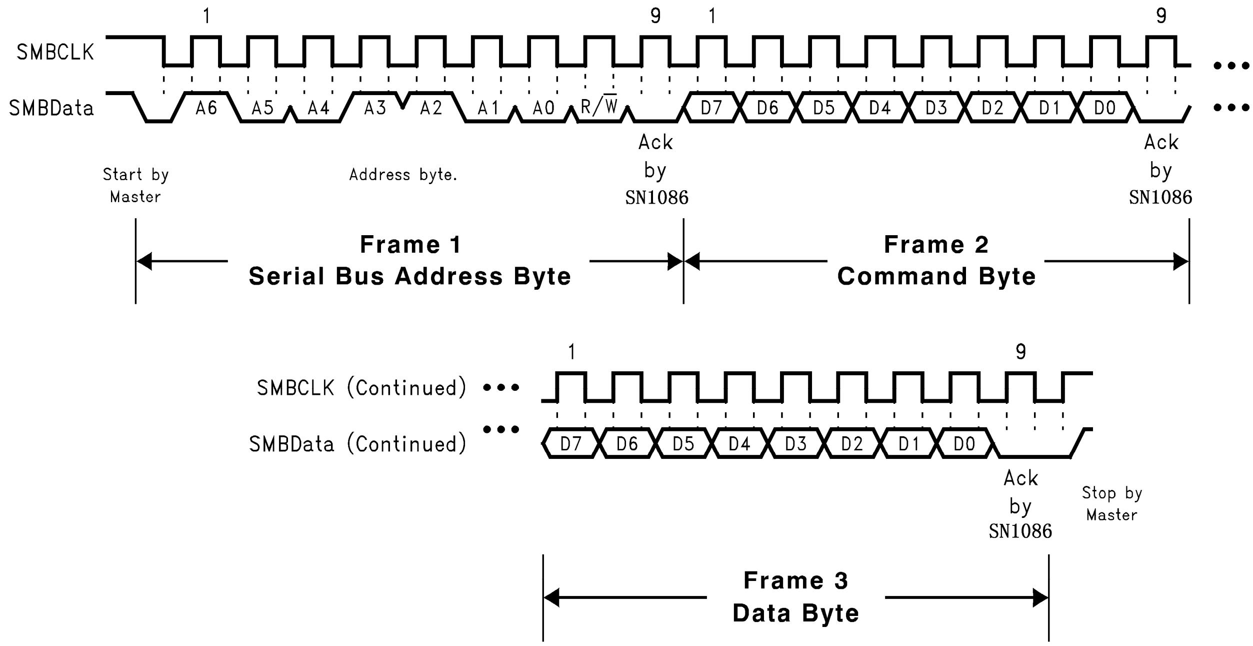
A **Write** to the SN1086 will always include the address byte and the command byte. A write to any register requires one data byte.

Reading the SN1086 can take place either of two ways:

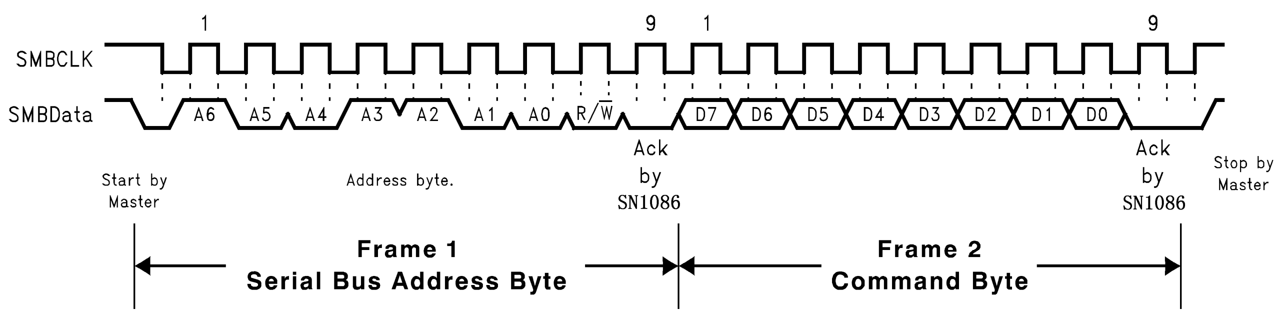
1. If the location latched in the Command Register is correct (most of the time it is expected that the Command Register will point to one of the Read Temperature Registers because that will be the data most frequently read from the SN1086), then the read can simply consist of an address byte, followed by retrieving the data byte.
2. If the Command Register needs to be set, then an address byte, command byte, repeat start, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, the SN1086 can accept either acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes the SN1086 125ms to measure the temperature of the remote diode and internal diode. When retrieving all 10 bits from a previous remote diode temperature measurement, the master must insure that all 10 bits are from the same temperature conversion. This may be achieved by using one-shot mode or by setting the conversion rate and monitoring the busy bit such that no conversion occurs in between reading the MSB and LSB of the last temperature conversion

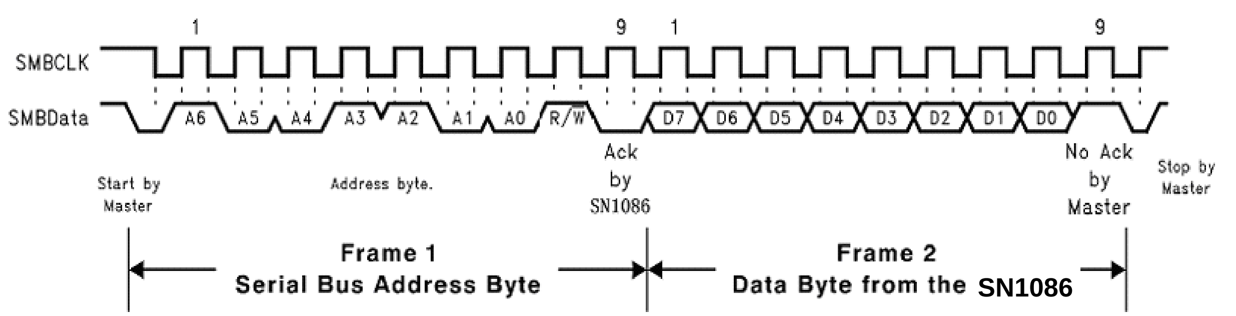
1.9.1 SMBus Timing Diagrams



(a) Serial Bus Write to the internal Command Register followed by a the Data Byte



(b) Serial Bus Write to the Internal Command Register



(c) Serial Bus Read from a Register with the Internal Command Register preset to desired value.

Figure 7 SMBus Timing Diagrams

1.10 Serial Interface Reset

In the event that the SMBus Master is RESET while the SN1086 is transmitting on the SMBData line, the SN1086 must be returned to a known state in the communication protocol. This may be done in one of two ways:

1. When SMBData is LOW, the SN1086 SMBus state machine resets to the SMBus idle state if either SMBData or SMBCLK are held low for more than 35ms ($t_{TIMEOUT}$). Note that according to SMBus specification 2.0 all devices are to timeout when either the SMBCLK or SMBData lines are held low for 25-35ms. Therefore, to insure a timeout of all devices on the bus the SMBCLK or SMBData lines must be held low for at least 35ms.
2. When SMBData is HIGH, have the master initiate an SMBus start. The SN1086 will respond properly to an SMBus start condition at any point during the communication. After the start the SN1086 will expect an SMBus Address address byte.

1.11 Digital Filter

In order to suppress erroneous remote temperature readings due to noise, the SN1086 incorporates a user-configured digital filter. The filter is accessed in the FILTER and ALERT CONFIGURE REGISTER at BFh. The filter can be set according to the following table.

D2	D1	Filter
0	0	No Filter
0	1	Level 1
1	0	Level 1
1	1	Level 2

Level 2 sets maximum filtering.

Figure 8 depict the filter output to in response to a step input and an impulse input. Figure 9 depicts the digital filter in use in a Pentium 4 processor system. Note that the two curves, with filter and without, have been purposely offset so that both responses can be clearly seen. Inserting the filter does not induce an offset as shown.

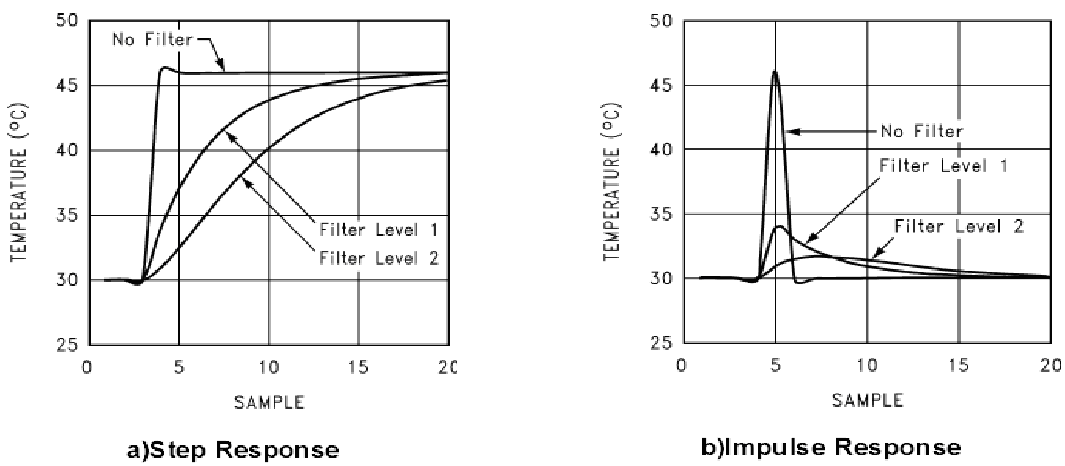


Figure 8 Filter Output Response to a Step Input

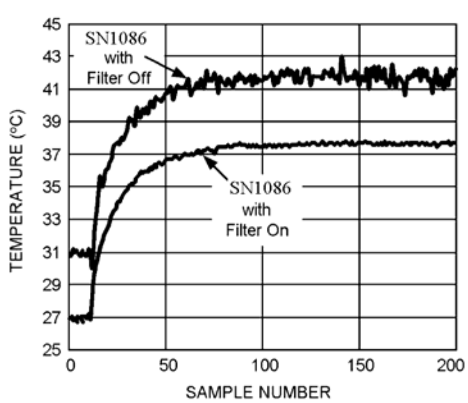


Figure 9 Digital Filter Response in a Pentium 4 processor System. The filter on and off curves were purposely offset to better show noise performance.

1.12 Fault Queue

In order to suppress erroneous ALERT or T_CRIT triggering the SN1086 incorporates a Fault Queue. The Fault Queue acts to insure a remote temperature measurement is genuinely beyond a HIGH, LOW or T_CRIT setpoint by not triggering until three consecutive out of limit measurements have been made, see Figure 10. The fault queue defaults off upon power-up and may be activated by setting bit D0 in the Configuration register (09h) to "1".

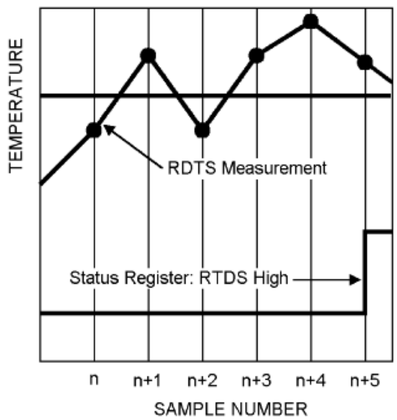


Figure 10 Fault Queue Temperature Response Diagram

1.13 One-Shot Register

The One-Shot register is used to initiate a single conversion and comparison cycle when the device is in standby mode, after which the device returns to standby. This is not a data register and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this register.

2.0 SN1086 Registers

2.1 Command Register

Selects which registers will be read from or written to. Data for this register should be transmitted during the Command Byte of the SMBus write communication.

P7	P6	P5	P4	P3	P2	P1	P0
Command Select							

P0-P7: Command Select

Command Select Address		**Command Select Address**		**Register Name**	**Register Function**
Read Address <P7:P0> hex	**Write Address <P7:P0> hex**	**<D7:D0> binary**	**<D7:D0> decimal**		
00h	NA	0000 0000	0	LT	Local Temperature
01h	NA	0000 0000	0	RTHB	Remote Temperature High Byte
02h	NA	0000 0000	0	SR	Status Register
03h	09h	0000 0000	0	C	Configuration
04h	0Ah	0000 1000	8(16conv./sec)	CR	Conversion Rate
05h	0Bh	0100 0110	70	LHS	Local HIGH Setpoint
06h	0Ch	0000 0000	0	LLS	Local LOW Setpoint
07h	0Dh	0100 0110	70	RHSHB	Remote HIGH Setpoint High Byte
08h	0Eh	0000 0000	0	RLSHB	Remote LOW Setpoint High Byte
NA	0Fh		0	One Shot	Writing to this register will initiate a one shot conversion
10h	NA	0000 0000	0	RTLB	Remote Temperature Low Byte
11h	11h	0000 0000	0	RTOHB	Remote Temperature Offset High Byte
12h	12h	0000 0000	0	RTOLB	Remote Temperature Offset Low Byte
13h	13h	0000 0000	0	RHSLB	Remote HIGH Setpoint Low Byte
14h	14h	0000 0000	0	RLSLB	Remote LOW Setpoint Low Byte
19h	19h	0101 0101	85	RCS	Remote T_CRIT Setpoint
20h	20h	0101 0101	85	LCS	Local T_CRIT Setpoint
21h	21h	0000 1010	10	TH	T_CRIT Hysteresis
B0h-BEh	B0h-BEh				Manufacturers Test Registers

BFh	BFh	0000 0000	0	RDTF	Remote Diode Temperature Filter
FEh	NA	0100 0111	71	RMID	Read Manufacturer's ID
FFh	NA	0001 0001	17	RDR	Read Stepping or Die Revision Code

2.2 Local and Remote Temperature Registers (LT, RTHB, RTLB)

(Read Only Address 00h, 01h) :

BIT	D7	D6	D5	D4	D3	D2	D1
Value	SIGN	64	32	16	8	4	2

For LT and RTHB D7–D0: Temperature Data. LSB = 1°C. Two's complement format.

(Read Only Address 10h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

For RTLB D7–D5: Temperature Data. LSB = 0.125°C. Two's complement format.
The maximum value available from the Local Temperature register is 127; the minimum value available from the Local Temperature register is -128. The maximum value available from the Remote Temperature register is 127.875; the minimum value available from the Remote Temperature registers is -128.875.

2.3 Status Register (SR)

(Read Only Address 02h):

D7	D6	D5	D4	D3	D2	D1	D0
Busy	LHIGH	LLOW	RHIGH	RLOW	OPEN	RCRIT	LCRIT

Power up default is with all bits "0" (zero).
D0: LCRIT: When set to "1" indicates a Local Critical Temperature alarm.
D1: RCRIT: When set to "1" indicates a Remote Diode Critical Temperature alarm.
D2: OPEN: When set to "1" indicates a Remote Diode disconnect.
D3: RLOW: When set to "1" indicates a Remote Diode LOW Temperature alarm
D4: RHIGH: When set to "1" indicates a Remote Diode HIGH Temperature alarm.
D5: LLOW: When set to "1" indicates a Local LOW Temperature alarm.
D6: LHIGH: When set to "1" indicates a Local HIGH Temperature alarm.
D7: Busy: When set to "1" ADC is busy converting.

2.4 Configuration Register

(Read Address 03h /Write Address 09h):

D7	D6	D5	D4	D3	D2	D1	D0
ALERT mask	RUN/STOP	SPNP	Remote T_CRIT_A	0	Local T_CRIT_A mask	0	Fault Queue

Power up default is with all bits "0" (zero)
D7: $\overline{\text{ALERT}}$ mask: When set to "1" $\overline{\text{ALERT}}$ interrupts are masked.
D6: RUN/STOP: When set to "1" SHUTDOWN is enabled.
D5: SPNP: When set to "1" 65nm or 90 nm process is selected and β compensation measure is enable.
D4: Remote T_CRIT mask: When set to "1" a diode temperature reading that exceeds T_CRIT setpoint will not activate the $\overline{\text{T\_CRIT\_A}}$ pin.
D3: is not defined and defaults to "0".
D2: Local T_CRIT mask: When set to "1" a Local temperature reading that exceeds T_CRIT setpoint will not activate the $\overline{\text{T\_CRIT\_A}}$ pin.
D1: is not defined and defaults to "0".
D0: Fault Queue: when set to "1" three consecutive remote temperature measurements outside the HIGH, LOW, or T_CRIT setpoints will trigger an "Outside Limit" condition resulting in setting of status bits and associated output pins.

2.5 Conversion Rate Register

(Read Address 04h /Write Address 0Ah)

Value	Conversio Rate
00	62.5mHz
01	125mHz
02	250mHz
03	500mHz
04	1Hz
05	2Hz
06	4Hz
07	8Hz
08	16Hz
09	16Hz
10-255	Undefined

2.6 Local And Remote High Setpoint Registers (LHS, RHSHB, and RHSLB)

(Read Address 05h, 07h /Write Address 0Bh, 0Dh):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

For LHS and RHSHB: HIGH setpoint temperature data. Power up default is LHIGH = RHIGH = 70˚C. 1LSB = 1˚C. Two's complement format.

(Read/Write Address 13h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

For RHSLB: Remote HIGH Setpoint Low Byte temperature data. Power up default is 0˚C. 1LSB = 0.125˚C. Two's complement format.

2.7 Local And Remote Low Setpoint Registers (LLS, RLSHB, and RLSLB)

(Read Address 06h, 08h, /Write Address 0Ch, 0Eh):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

For LLS and RLSHB: HIGH setpoint temperature data. Power up default is LHIGH = RHIGH = 0˚C. 1LSB = 1˚C. Two's complement format.

(Read/Write Address 14h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

For RLSLB: Remote HIGH Setpoint Low Byte temperature data. Power up default is 0˚C. 1LSB = 0.125˚C. Two's complement format.

2.8 Remote Temperature Offset Registers (RTOHB and RTOLB)

(Read/Write Address 11h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

For RTOHB: Remote Temperature Offset High Byte. Power up default is LHIGH = RHIGH = 0˚C. 1LSB = 1˚C. Two's complement format.

(Read/Write Address 12h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0.5	0.25	0.125	0	0	0	0	0

For RTOLB: Remote Temperature Offset High Byte. Power up default is 0˚C. 1LSB = 0.125˚C. Two's complement format.
The offset value written to these registers will automatically be added to or subtracted from the remote temperature measurement that will be reported in the Remote Temperature registers.

2.9 Local And Remote T_CRIT Registers (RCS and LCS)

(Read/Write Address 20h, 19h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	SIGN	64	32	16	8	4	2	1

D7–D0: T_CRIT setpoint temperature data. Power up default is T_CRIT = 85˚C. 1 LSB = 1˚C, two's complement format.

2.10 T_CRIT Hysteresis Register (TH)

(Read and Write Address 21h):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value				16	8	4	2	1

D7–D0: T_CRIT Hysteresis temperature. Power up default is TH = 10˚C. 1 LSB = 1˚C, maximum value = 31.

2.11 Filter And Alert Configure Register

(Read and Write Address BFh):

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	0	0	0	0	Filter Level		$\overline{\text{ALERT}}$ Configure

D7-D3: is not defined defaults to '0'.
D2-D1: input filter setting as defined the table below:

D2	D1	Filter Level
0	0	No Filter
0	1	Level 1
1	0	Level 1
1	1	Level 2

Level 2 sets maximum filtering.

D0: when set to ’1’ comparator mode is enabled.

2.12 Manufacturers ID Register

(Read Address FEh) Default value 47h.

2.13 Die Revision Code Register

(Read Address FFh) Default value 11h.

3.0 Application Hints

The SN1086 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed circuit board lands and traces soldered to the SN1086's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the SN1086 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

To measure temperature external to the SN1086's die, use a remote diode. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the SN1086's temperature. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads. Most silicon diodes do not lend themselves well to this application. It is recommended that an MMBT3904 transistor base-emitter junction be used with the collector tied to the base.

The SN1086's β compensation technology allows accurate sensing of integrated thermal diodes, such as those found on most processors. With β compensation technology turned off, the SN1086 can measure a diode-connected transistor such as the MMBT3904 or the thermal diode found in an AMD processor.

The SN1086 has been optimized to measure the remote thermal diode integrated in a typical Intel processor on 65nm or 90nm process or an MMBT3904 transistor. Using the Remote Diode Model Select register either pair of remote inputs can be assigned to be either a typical Intel processor on 65nm or 90nm process or an MMBT3904.

3.1 Diode Non-Ideality

3.1.1 Diode Non-Ideality Factor Effect on Accuracy

When a transistor is connected as a diode, the following relationship holds for variables V_{BE}, T and I_F:

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t}\right)} - 1 \right] \quad (1)$$

Where:

$$V_t = \frac{kT}{q}$$

- $q = 1.6 \times 10^{-19}$ Coulombs (the electron charge),
- T = Absolute Temperature in Kelvin
- $k = 1.38 \times 10^{-23}$ joules/K (Boltzmann's constant),
- η is the non-ideality factor of the process the diode is manufactured on,
- I_S = Saturation Current and is process dependent,
- I_f = Forward Current through the base-emitter junction
- V_{BE} = Base-Emitter Voltage drop

In the active region, the -1 term is negligible and may be eliminated, yielding the following equation

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t}\right)} \right] \quad (2)$$

In *Equation 2*, η and I_S are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a very controlled ratio (I_{F2} / I_{F1}) and measuring the resulting voltage difference, it is possible to eliminate the I_S term. Solving for the forward voltage difference yields the relationship:

$$\Delta V_{BE} = \eta \times \left(\frac{kT}{q}\right) \times \ln\left(\frac{I_{F2}}{I_{F1}}\right) \quad (3)$$

Solving *Equation 3* for temperature yields:

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{F2}}{I_{F1}}\right)} \quad (4)$$

Equation 4 holds true when a diode connected transistor such as the MMBT3904 is used. When this "diode" equation is applied to an integrated diode such as a processor transistor with its collector tied to GND as shown in *Figure 7* it will yield a wide non-ideality spread. This wide non-ideality spread is not due to true process variation but due to the fact that *Equation 4* is an approximation.

β compensation technology uses the transistor equation, *Equation 5*, which is a more accurate representation of the topology of the thermal diode found in an FPGA or processor.

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{C2}}{I_{C1}}\right)} \quad (5)$$

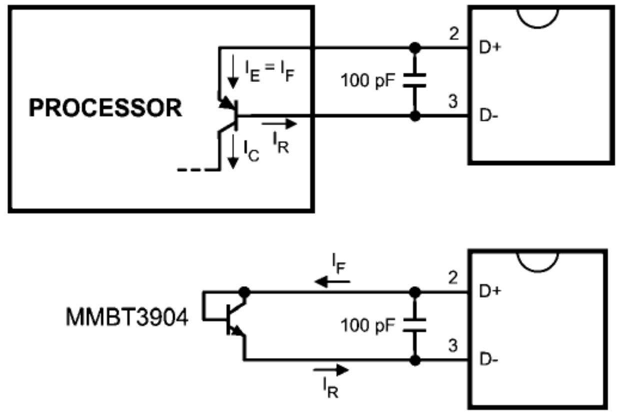


Figure 11 Thermal Diode Current Paths

β compensation should only be enabled when measuring the temperature of a transistor integrated as shown in the processor of *Figure 11*, because *Equation 5* only applies to this topology.

3.1.2 Calculating Total System Accuracy

The voltage seen by the SN1086 also includes the $I_F R_S$ voltage drop of the series resistance. The non-ideality factor, η, is the only other parameter not accounted for and depends on the diode that is used for measurement. Since ΔV_{BE} is proportional to both η and T, the variations in η cannot be distinguished from variations in temperature. Since the nonideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the for Intel processor on 65nm process, Intel specifies a +4.06%/−0.897% variation in η from part to part when the processor diode is measured by a circuit that assumes diode equation, *Equation 4*, as true. As an example, assume a temperature sensor has an accuracy specification of ±1.0°C at a temperature of 80°C (353 Kelvin) and the processor diode has a nonideality variation of +1.19%/−0.27%. The resulting system accuracy of the processor temperature being sensed will be:

T_{ACC} = + 1.0°C + (+4.06% of 353 K) = +15.3 °C

and

T_{ACC} = - 1.0°C + (−0.89% of 353 K) = −4.1 °C

β compensation technology uses the transistor equation, *Equation 5*, resulting in a non-ideality spread that truly reflects the process variation which is very small. The transistor equation non-ideality spread is ±0.39% for the Pentium 4 processor on 90 nm process. The resulting accuracy when using β compensation technology improves to:

T_{ACC} = ±0.75°C + (±0.39% of 353 K) = ± 2.16 °C

The next error term to be discussed is that due to the series resistance of the thermal diode and printed circuit board traces. The thermal diode series resistance is specified on most processor datasheets. For Intel processors in 65 nm process, this is specified at 4.52Ω typical. The SN1086 accommodates the typical series resistance of Intel Processor on 65 nm process. The error that is not accounted for is the spread of the processor's series resistance that is 2.79Ω to 6.24Ω or ±1.73Ω. The equation to calculate the temperature error due to series resistance (T_{ER}) for the SN1086 is simply:

$$T_{ER} = \left(0.62\frac{°C}{\Omega}\right) \times R_{PCB} \quad (6)$$

Solving *Equation 6* for R_{PCB} equals to ±1.73Ω results in the additional error due to the spread in the series resistance of ±1.07°C. The spread in error cannot be canceled out, as it would require measuring each individual thermal diode device. This is quite difficult and impractical in a large volume production environment.

Equation 6 can also be used to calculate the additional error caused by series resistance on the printed circuit board. Since the variation of the PCB series resistance is minimal, the bulk of the error term is always positive and can simply be cancelled out by subtracting it from the output readings of the SN1086.

Processor Family	Transistor Equation ηT, non-ideality			Series R,Ω
	min	typ	max	
Intel Processor on 65 nm process	0.997	1.001	1.005	4.52

Processor Family	Diode Equation ηD, non ideality -			Series R,Ω
	min	typ	max	
Pentium III CPUID 67h	1	1.0065	1.0125	
Pentium III CPUID 68h/ PGA370Socket/ Celeron	1.0057	1.008	1.0125	
Pentium 4423 pin	0.9933	1.0045	1.0368	
Pentium 4478 pin	0.9933	1.0045	1.0368	
Pentium 4 on 0.13 micron process, 2 - 3.06 GHz	1.0011	1.0021	1.0030	3.64
Pentium 4 on 90 nm process	1.0083	1.011	1.023	3.33
Intel Processor on 65 nm process	1.000	1.009	1.050	4.52
Pentium M (Centrino)	1.00151	1.00220	1.00289	3.06
MMBT3904		1.003		
AMD Athlon MP model 6	1.002	1.008	1.016	
AMD Athlon 64	1.008	1.008	1.096	
AMD Opteron	1.008	1.008	1.096	
AMD Sempron		1.00261		0.93

3.1.3 Compensating for Different Non-Ideality

In order to compensate for the errors introduced by non-ideality, the temperature sensor is calibrated for a particular processor. National Semiconductor temperature sensors are always calibrated to the typical non-ideality and series resistance of a given processor type. The SN1086 is calibrated for two non-ideality factors and series resistance values thus supporting the MMBT3904 transistor and Intel processors on 65nm process without the requirement for additional trims. For most accurate measurements β compensation mode should be turned on when measuring the Intel processor on 65nm process to minimize the error introduced by the false non-ideality spread (see *3.1.1 Diode Non-Ideality Factor Effect on Accuracy*). When a temperature sensor calibrated for a particular processor type is used with a different processor type, additional errors are introduced.

Temperature errors associated with non-ideality of different processor types may be reduced in a specific temperature range of concern through use of software calibration. Typical Non-ideality specification differences cause a gain variation of the transfer function, therefore the center of the temperature range of interest should be the target temperature for calibration purposes. The following equation can be used to calculate the temperature correction factor (T_{CF}) required to compensate for a target non-ideality differing from that supported by the SN1086.

$$T_{CF} = \left(\frac{\eta_S - \eta_{PROCESSOR}}{\eta_S}\right) \times (T_{CR} + 273K) \quad (7)$$

where

• η_S = SN1086 non-ideality for accuracy specification

• $\eta_{PROCESSOR}$ = Processor thermal diode typical non-ideality

• T_{CR} = center of the temperature range of interest in °C

The correction factor should be directly added to the temperature reading produced by the SN1086. For example when using the SN1086, with the 3904 mode selected, to measure a AMD Athlon processor, with a typical non-ideality of 1.008, for a temperature range of 60 °C to 100 °C the correction factor would calculate to:

$$T_{CF} = \left(\frac{1.003 - 1.008}{1.003}\right) \cdot (80 + 273) = -1.75^{o}C \quad (8)$$

Therefore, 1.75 ° C should be subtracted from the temperature readings of the SN1086 to compensate for the differing typical non-ideality target.

3.2 PCB Layout For Minimizing Noise

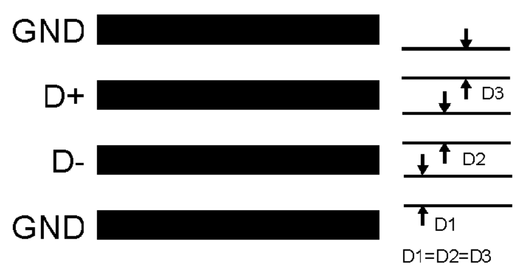


Figure 13 Ideal Diode Trace Layout

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the SN1086 can cause temperature conversion errors. Keep in mind that the signal level the SN1086 is trying to measure is in microvolts. The following guidelines should be followed:

1. Place a 0.1 µF power supply bypass capacitor as close as possible to the V_{DD} pin and the recommended 2.2 nF capacitor as close as possible to the SN1086's D+ and D− pins. Make sure the traces to the 2.2nF capacitor are matched.

2. The recommended 2.2nF diode bypass capacitor actually has a range of TBDpF to 3.3nF. The average temperature accuracy will not degrade. Increasing the capacitance will lower the corner frequency where differential noise error affects the temperature reading thus producing a reading that is more stable. Conversely, lowering the capacitance will increase the corner frequency where differential noise error affects the temperature reading thus producing a reading that is less stable.

3. Ideally, the SN1086 should be placed within 10cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 1Ω can cause as much as 1˚C of error. This error can be compensated by using the Remote Temperature Offset Registers, since the value placed in these registers will automatically be subtracted from or added to the remote temperature reading.

4. Diode traces should be surrounded by a GND guard ring to either side, above and below if possible. This GND guard should not be between the D+ and D− lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D− lines.

5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.

6. Avoid running diode traces close to or parallel to high speed digital and bus lines. Diode traces should be kept at least 2cm apart from the high speed digital traces.

7. If it is necessary to cross high speed digital traces, the diode traces and the high speed digital traces should cross at a 90 degree angle.

8. The ideal place to connect the SN1086's GND pin is as close as possible to the Processors GND associated with the sense diode.

9. Leakage current between D+ and GND should be kept to a minimum. One nano-ampere of leakage can cause as much as 1˚C of error in the diode temperature reading. Keeping the printed circuit board as clean as possible will minimize leakage current.

Noise coupling into the digital lines greater than 400mVp-p (typical hysteresis) and undershoot less than 500mV below GND, may prevent successful SMBus communication with the SN1086. SMBus no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the SMBus maximum frequency of communication is rather low (100kHz max), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed circuit board traces. An RC low pass filter with a 3db corner frequency of about 40MHz is included on the SN1086's SMBCLK input. Additional resistance can be added in series with the SMBData and SMBCLK lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high speed data communications cross at right angles to the SMBData and SMBCLK lines.

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

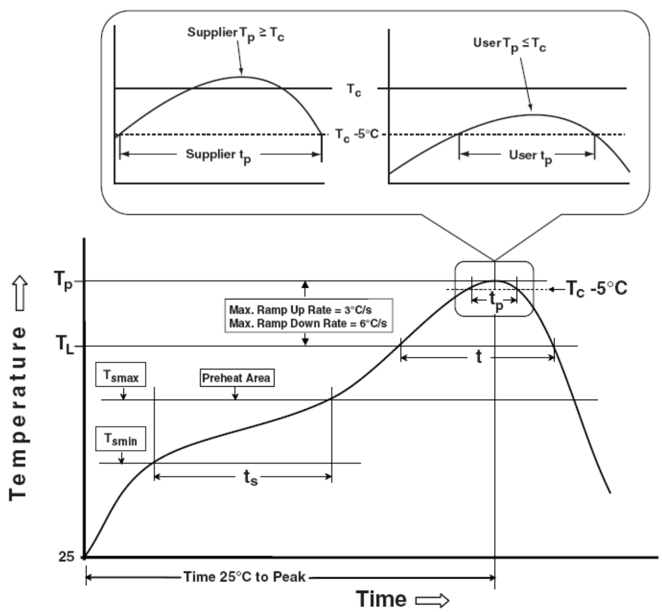
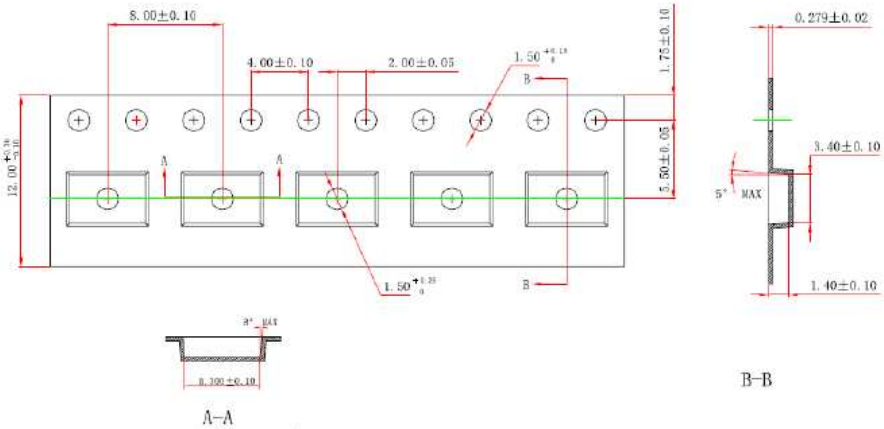
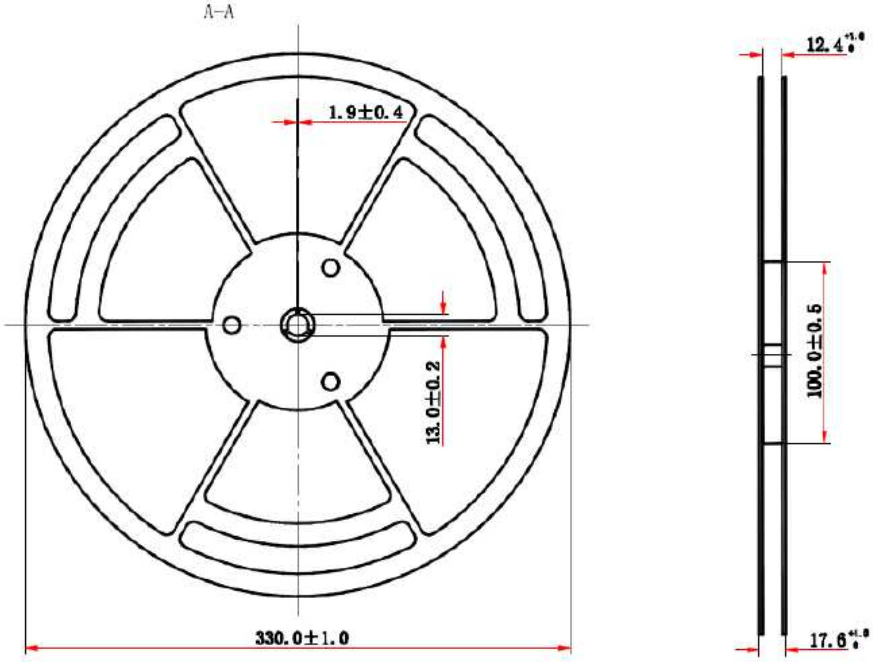


Figure 12 Classification Profile

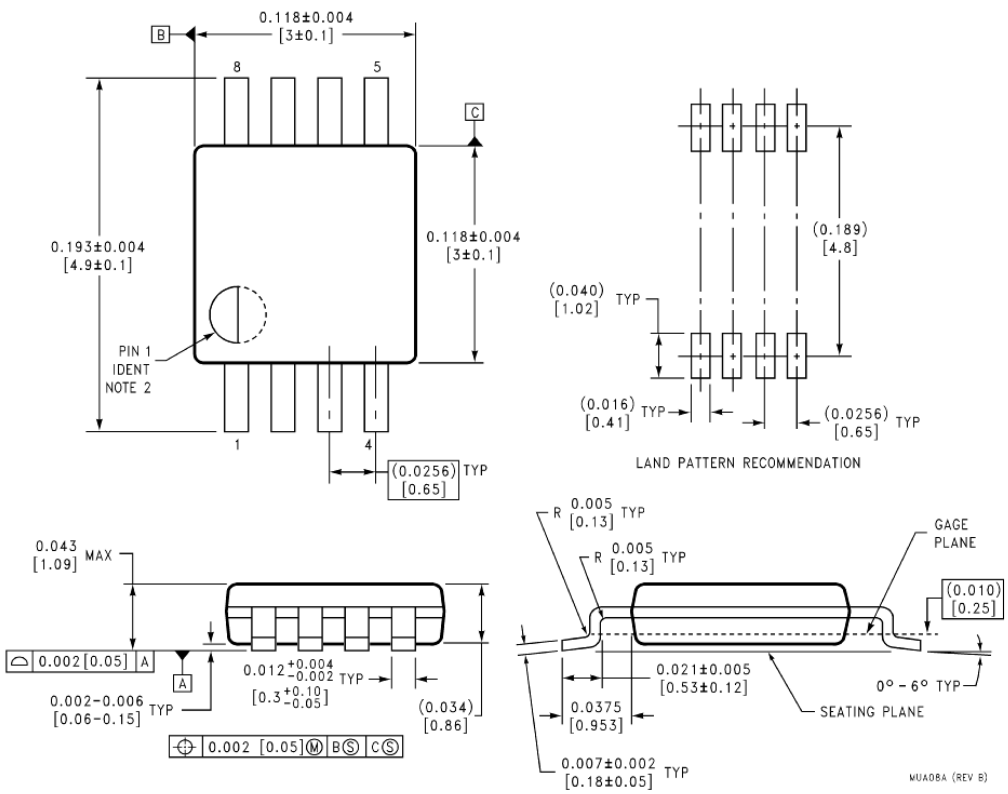
Tape and Reel Information





Package Information

MSOP-8



Note: All dimensions in millimeters unless otherwise stated.

IMPORTANT NOTICE

SI-EN Technology cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a SI-EN Technology product. SI-EN Technology reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its specifications, products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.