Dual 2.84W Stereo Audio Amplifier Plus Headphone Driver

General Description

The SN4088A is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.84W to a 4Ω load.

To simplify audio system design, the SN4088A combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The SN4088A features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

Applications

- Cell phones, PDA, MP4,PMP
- Portable and desktop computers
- Desktops Audio System
- Multimedia monitors

Key Specifications

- P_O at 1% THD+N, VDD = 5V
  - RL = 4Ω 2.30W (typ)
  - RL = 8Ω 1.38W (typ)
- P_O at 10% THD+N, VDD = 5V
  - RL = 4Ω 2.84W (typ)
  - RL = 8Ω 1.71W (typ)
- P_O at 1% THD+N, VDD = 4V
  - RL = 4Ω 1.40W (typ)
  - RL = 8Ω 0.89W (typ)
- Shutdown current 0.04μA (typ)
- Supply voltage range 2.7V to 5.5V
- QFN16(4mm*4mm*0.75mm) Package

Features

- Suppress "click and pop"
- Thermal shutdown protection circuitry
- Stereo headphone amplifier mode
- Micro power shutdown mode

Connection Diagram (Top View)

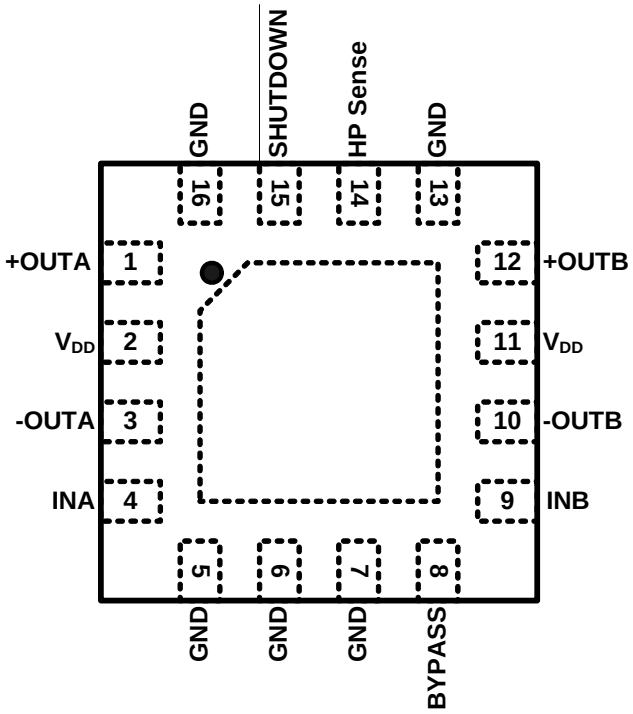


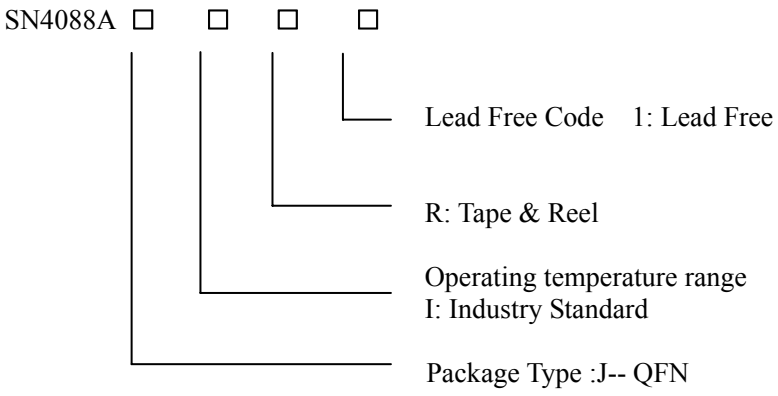
Figure1

Pin Description

Pin	Pin	I/O	Description
INA	4	I	Left Channel Input
INB	8	I	Right Channel Input
-OUTA	3	O	Left channel –output
+OUTA	1	O	Left channel +output
-OUTB	10	O	Right channel –output
+OUTB	12	O	Right channel +output
V_{DD}	2,11		Supply Voltage
Hp sense	14	I	Headphone sense control
$\overline{\text{Shutdown}}$	15	I	Shut down control, hold low for shutdown mode
Bypass	9		Bypass capacitor which provides the common mode voltage
GND	5，6，7，13，16		GND

Ordering Information

Order Number	Package Type	Operating Temperature range
SN4088AJIR1	QFN16	-40 °C to 85°C



Typical Application

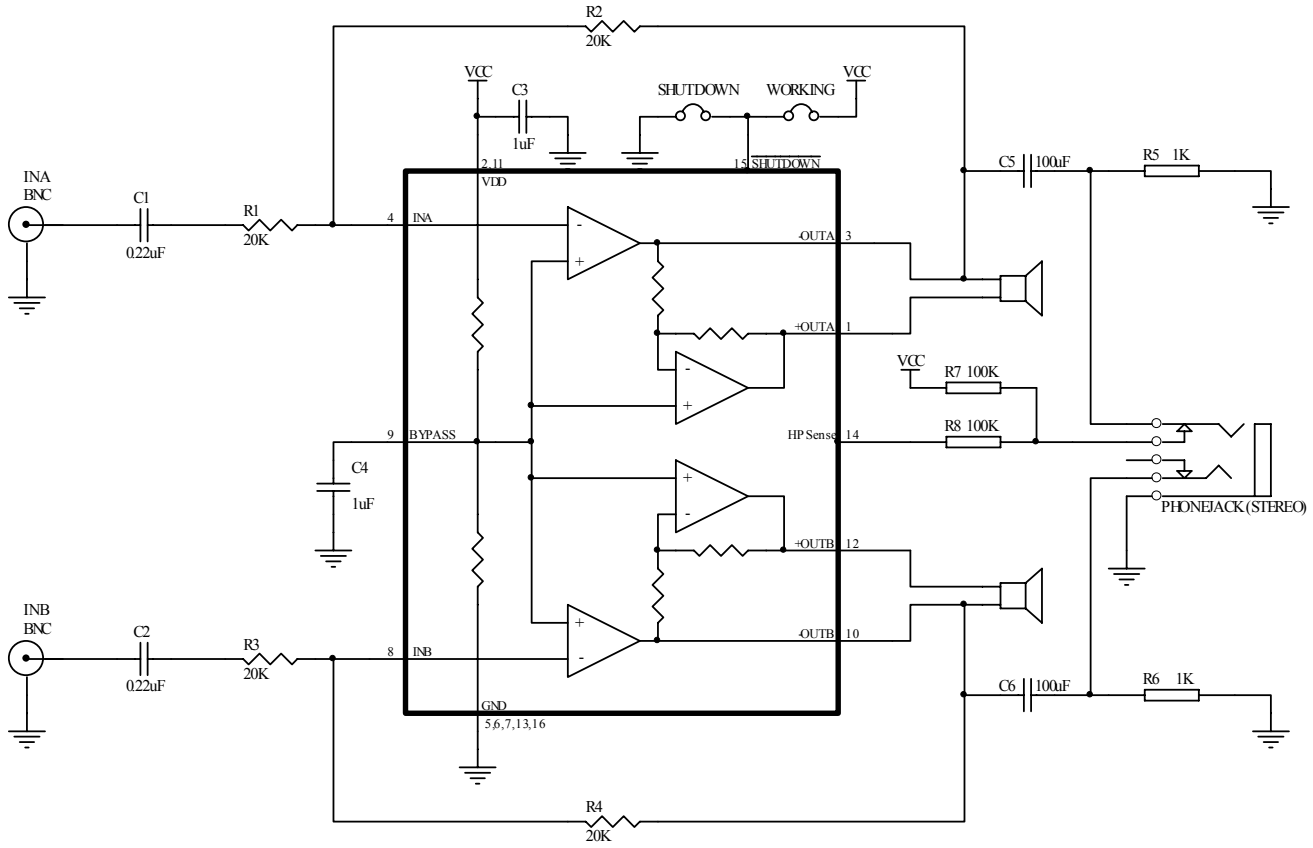


Figure 2. Typical Audio Amplifier Application Circuit

Absolute Maximum Ratings

Supply Voltage 6.0V
Solder Information
  Small Outline Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C
Storage Temperature ..... −65°C to +150°C
Input Voltage ..... −0.3V to V_{DD}+0.3V
Junction Temperature ..... 150°C

Operating Ratings

Temperature Range
$T_{MIN} \leqslant T_A \leqslant T_{MAX}$ .....−40°C $\leqslant T_A \leqslant$ 85°C
Supply Voltage ..... 2.7V $\leqslant V_{DD} \leqslant$ 5.5V

Electrical Characteristics (5V)

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T = 25°C

Symbol	Parameter	condition	SN4088A		Units (Limits)
			Typical	Limit	
V_{DD}	Supply Voltage			2.7	V(min)
				5.5	V(max)
I_{DD}	Quiescent power supply current	Vin=0V, Io=0A, BTL Vin=0V, Io=0A, SE	5.7 3	7.5 4	mA(max) mA(max)
I_{SD}	Shutdown current	GND applied to the shutdown pin	0.036	1	uA(max)
V_{IH}	Shutdown, HP sense Input Voltage High			1.4	V(min)
V_{IL}	Shutdown, HP sense Input Voltage Low			0.4	V(max)
T_{WU}	Turn on time	1uF bypass cap(C4)	113		ms

Electrical Characteristics Operation (5V)

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T = 25°C

Symbol	Parameter	Conditions	SN4088A		Units (Limits)
			Typical	Limit	
Vos	Output offset voltage	V_{IN}=0V	5	25	mV(max)
Po	Output power	THD+N=1%, f=1kHz,R_L=8Ω,BTL mode	1.38	1.2	W(min)
		THD+N=10%, f=1kHzR_L=8Ω,BTL mode	1.71	1.5	W(min)
		THD+N=1%, f=1kHz,R_L=4Ω,BTL mode	2.30	2.0	W(min)
		THD+N=10%, f=1kHz,R_L=4Ω,BTL mode	2.84	2.5	W(min)
THD+N	Total Harmonic Distortion +noise	1KHz, Avd=2 R_L=8Ω, Po=0.4W	0.055		%
PSRR	Power Supply Rejection Ratio	Input unterminated 217Hz Vripple=200mVp-p C4=1uF, R_L=8Ω	82		dB
		Input unterminated 1KHz, Vripple=200mVp-p C4=1uF, R_L=8Ω	70		dB
		Input grounded 217Hz Vripple=200mVp-p C4=1uF, R_L=8Ω	80		dB
		Input grounded 1KHz Vripple=200mVp-p C4=1uF, R_L=8Ω	75		dB
Xtalk	Channel separation	f=1KHz, C4=1uF, BTL mode, 8Ohm	-91		dB
V_{NO}	Output noise voltage	1KHz, A-weighted	30		uV

Electrical Characteristics for Single-Ended Operation (5V)

Symbol	Parameter	Condition	SN4088A		Units (Limits)
			Typical	Limit	
Po	Output power	THD+N=0.5%,f=1KHz, RL=32Ω, SE mode	98.5	83	mW(min)
THD+N	Total harmonic distortion+noise	Po=20mW,1KHz, RL=32Ω	0.013		%
PSRR	Power Supply Rejection Raito	Input unterminated 217Hz Vripple=200mVp-p C4=1uF, R_L=8Ω	84		dB
		Input unterminated 1KHz, Vripple=200mVp-p C4=1uF, R_L=8Ω	80		dB
		Input grounded 217Hz Vripple=200mVp-p C4=1uF, R_L=8Ω	82		dB
		Input grounded 1KHz Vripple=200mVp-p C4=1uF, R_L=8Ω	80		dB
Xtalk	Channel separation	f=1KHz, C6=1uF, Stereo Enhanced control=Low	-68		dB
V_{NO}	Output noise voltage	1KHz, A-weighted	20		uV

Electrical Characteristics (3V)

The following specifications apply for V_{DD}= 3V unless otherwise noted. Limits apply for T = 25°C

Symbol	Parameter	Condition	SN4088A		Units (Limits)
			Typical	Limit	
I_{DD}	Quiescent power supply current	Vin=0V, Io=0A ,BTL Vin=0V, Io=0A ,SE	5 2.6		mA mA
I_{SD}	Shutdown current	GND applied to the shutdown pin	0.02		uA
V_{IH}	Shutdown, HP sense Input Voltage High			1.1	V(min)
V_{IL}	Shutdown, HP sense Input Voltage Low			0.4	V(max)
T_{WU}	Turn on time	1uF bypass cap(C4)	120		ms

Electrical Characteristics Operation (3V)

The following specifications apply for V_{DD}= 3V unless otherwise noted. Limits apply for T = 25°C

Symbol	Parameter	Conditions	SN4088A		Units (Limits)
			Typical	Limit	
Vos	Output offset voltage	V_{IN}=0V	2.5		mV
Po	Output power	THD+N=1%, f=1kHz,R_L=8Ω,BTL mode	0.48		W(min)
		THD+N=10%, f=1kHzR_L=8Ω,BTL mode	0.6		W(min)
		THD+N=1%, f=1kHz,R_L=4Ω,BTL mode	0.78		W(min)
		THD+N=10%, f=1kHz,R_L=4Ω,BTL mode	0.97		W(min)
THD+N	Total Harmonic Distortion+noise	1KHz, Avd=2 R_L=8Ω, Po=0.15W	0.078		%
PSRR	Power Supply Rejection Ratio	Input unterminated 217Hz, Vripple=200mVp-p, C4=1uF, R_L=8Ω	85		dB
		Input unterminated 1KHz, Vripple=200mVp-p, C4=1uF, R_L=8Ω	75		dB
		Input grounded 217Hz, Vripple=200mVp-p, C4=1uF, R_L=8Ω	84		dB
		Input grounded 1KHz, Vripple=200mVp-p, C4=1uF, R_L=8Ω	75		dB
Xtalk	Channel separation	f=1KHz, C4=1uF	-92		dB
V_{NO}	Output noise voltage	1KHz, A-weighted	30		uV

Electrical Characteristics for Single-Ended Operation (3V)

Symbol	Parameter	Condition	SN4088A		Units (Limits)
			Typical	Limit	
Po	Output power	THD+N=0.5%,f=1KHz, RL=32Ω	36.7		mw
THD+N	Total harmonic distortion+noise	Po=20mW,1KHz, RL=32Ω	0.016		%
PSRR	Power Supply Rejection Raito	Input unterminated 217Hz Vripple=200mVp-p C6=1uF RL=32Ω	87		dB
		Input unterminated 1KHz Vripple=200mVp-p C6=1uF RL=32Ω	80		dB
		Input grounded 217Hz Vripple=200mVp-p C6=1uF RL=32Ω	82		dB
		Input grounded 1KHz Vripple=200mVp-p C6=1uF RL=32Ω	82		dB
Xtalk	Channel separation	f=1KHz, C6=1uF, Stereo Enhanced control=Low	-66		dB
V_{NO}	Output noise voltage	1KHz, A-weighted	20		uV

Typical Performance Characteristics

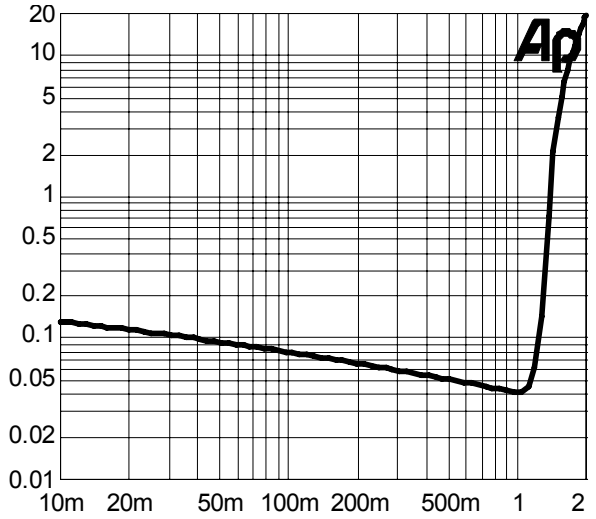


Figure 3, THD+N vs. Output Power
5V, 8Ohm, BTL at f=1 kHz

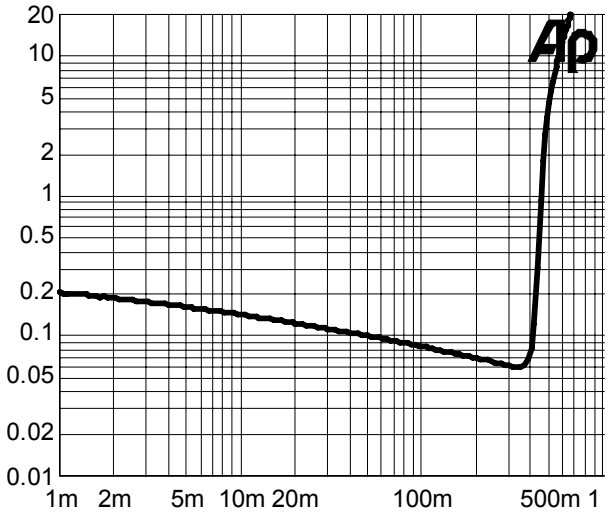


Figure 4. THD+N vs. Output Power
3V, 8Ohm, BTL at f=1 kHz

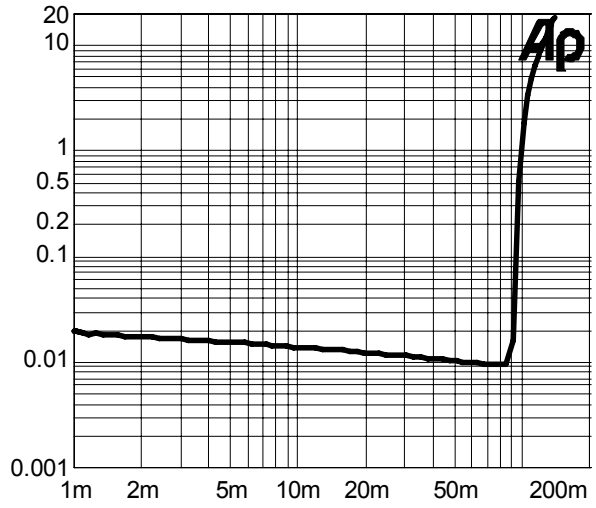


Figure 5. THD+N vs. Output Power
SE mode, 5V, 32Ohm, f=1 kHz

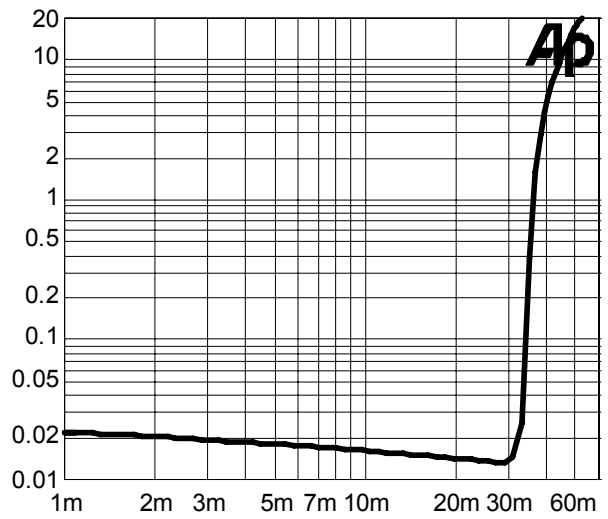


Figure 6. THD+N vs. Output Power
SE mode, 3V, 32Ohm, f=1 kHz

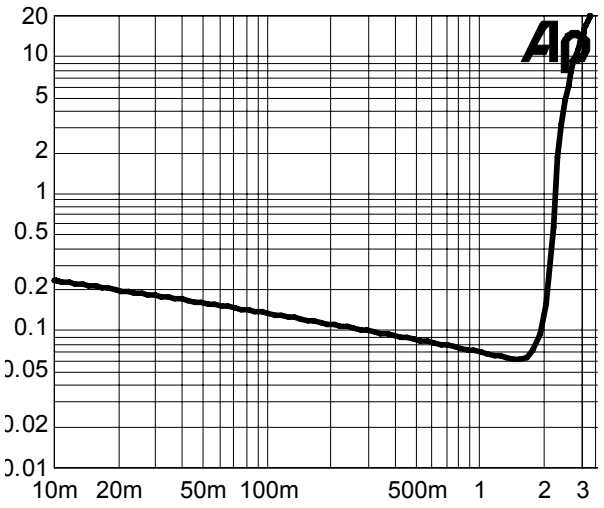


Figure 7. THD+N vs. Output Power
BTL mode, 5V, 4Ohm, f=1 kHz

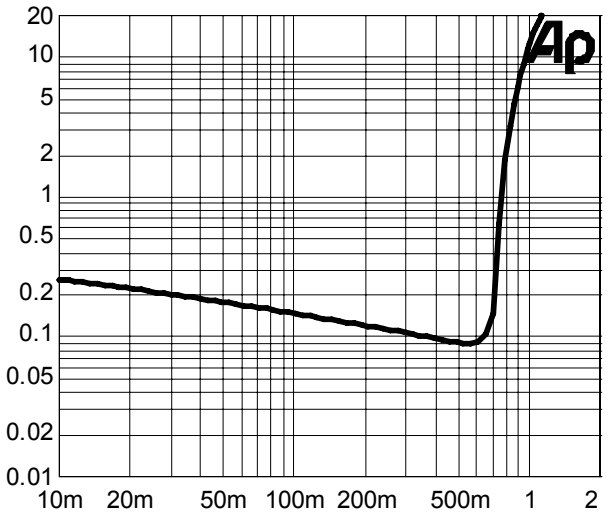


Figure 8. THD+N vs. Output Power
BTL mode, 3V, 4Ohm, f=1 kHz

Typical Performance Characteristics (Continued)

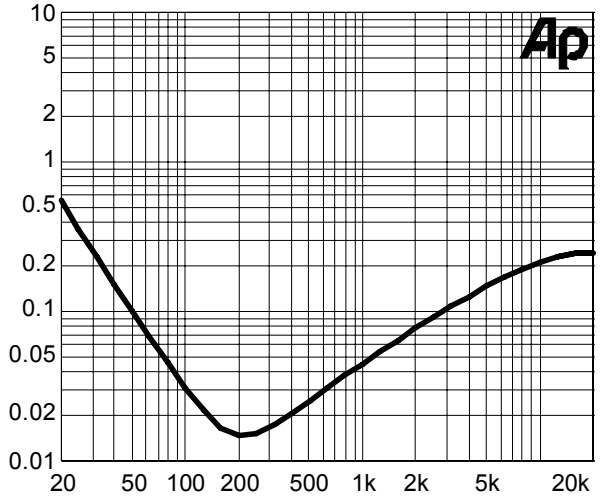


Figure 9. THD+N vs. Frequency
BTL mode, 5V, 8Ohm, Po=800mW

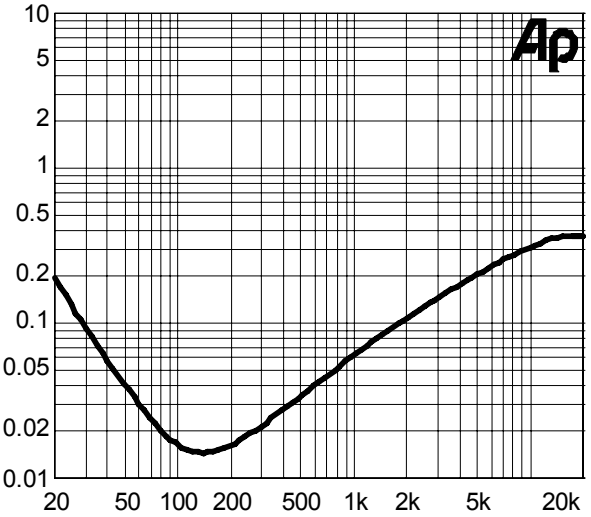


Figure 10. THD+N vs. Frequency
BTL mode, 3V, 8Ohm, Po=300mW

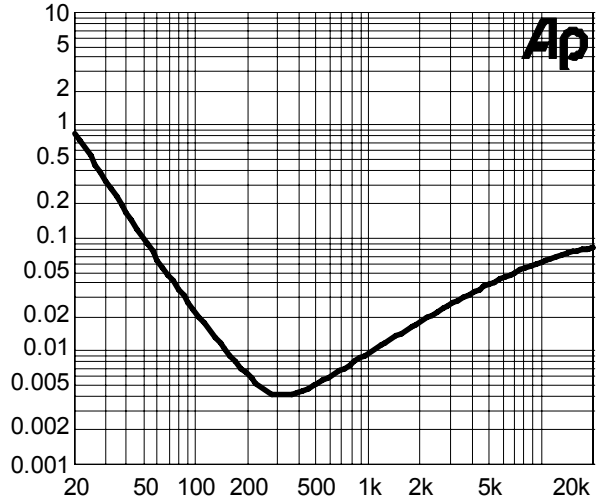


Figure 11. THD+N vs. Frequency
SE mode, 5V, 32Ohm, Po=70mW

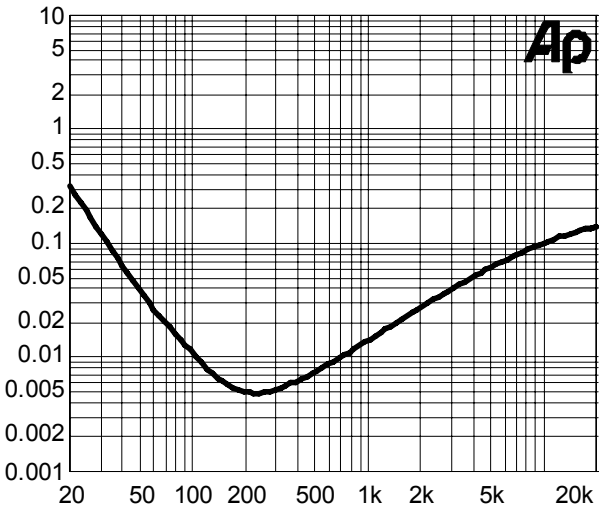


Figure 12. THD+N vs. Frequency
SE mode, 3V, 32Ohm, Po=20mW

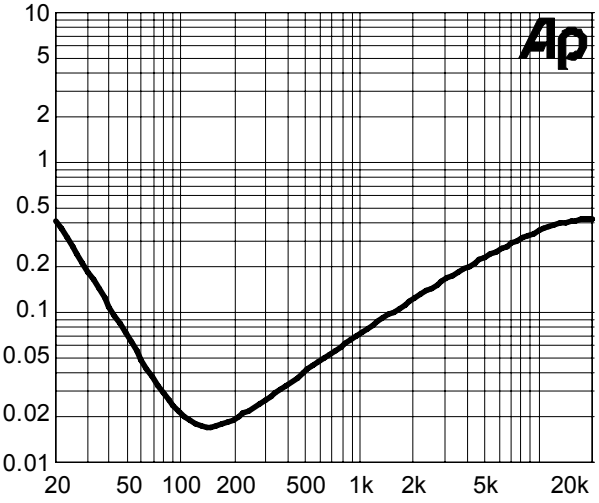


Figure 13. THD+N vs. Frequency
BTL mode, 5V, 4Ohm, Po=1W

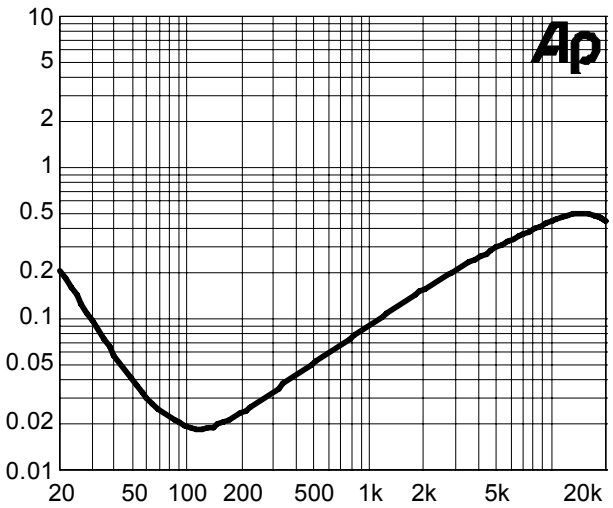


Figure 14. THD+N vs. Frequency
BTL mode, 3V, 4Ohm, Po=500mW

Typical Performance Characteristics (Continued)

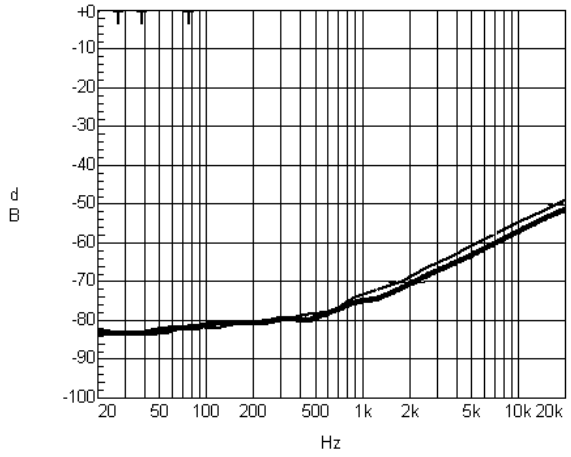


Figure 15. PSRR vs. Freq
BTL mode, 5V, 8Ohm, 200mVpp
Input terminated

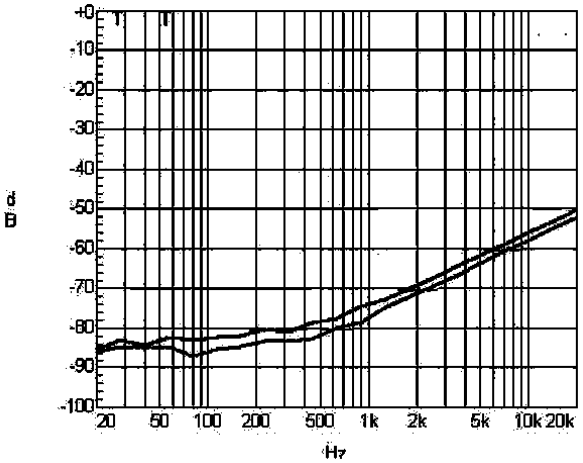


Figure 16. PSRR vs. Freq
BTL mode, 3V, 8Ohm, 200mVpp
Input terminated

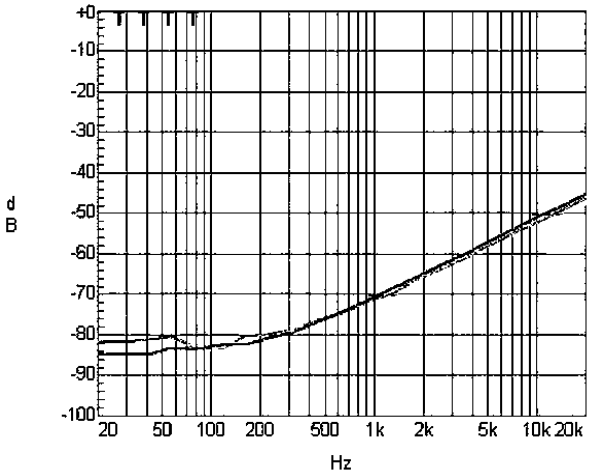


Figure 17. PSRR vs. Freq
BTL mode, 5V, 8Ohm, 200mVpp
Input unterminated

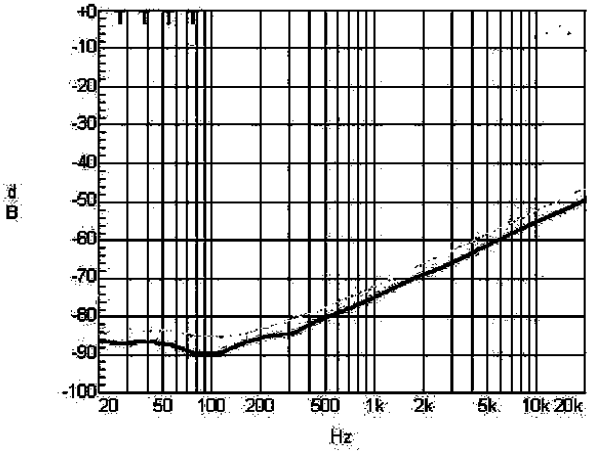


Figure 18. PSRR vs. Freq
BTL mode, 3V, 8Ohm, 200mVpp
Input unterminated

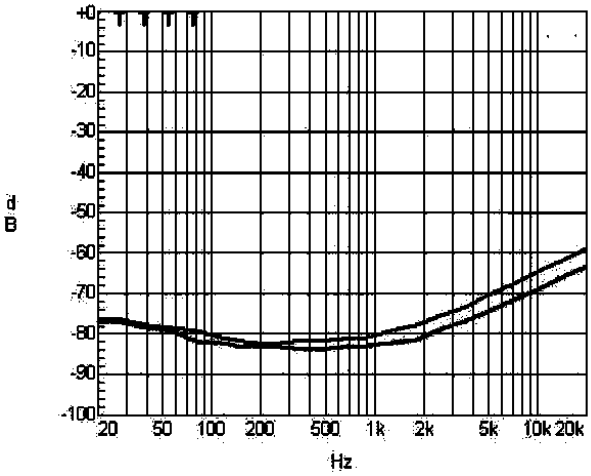


Figure 19. PSRR vs. Freq
SE mode, 5V, 32Ohm, 200mVpp
Input terminated

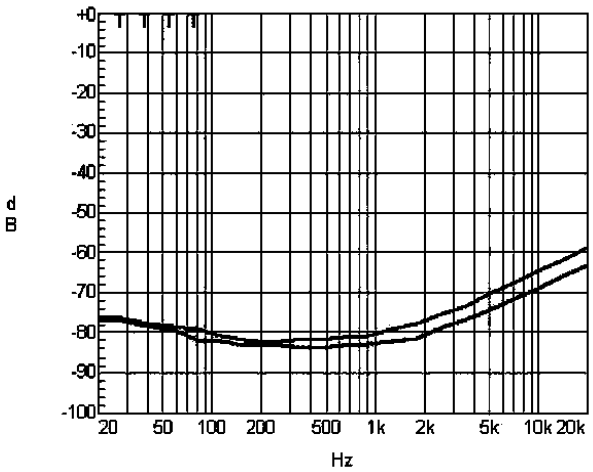


Figure 20. PSRR vs. Freq
SE mode, 3V, 32Ohm, 200mVpp
Input terminated

Typical Performance Characteristics (Continued)

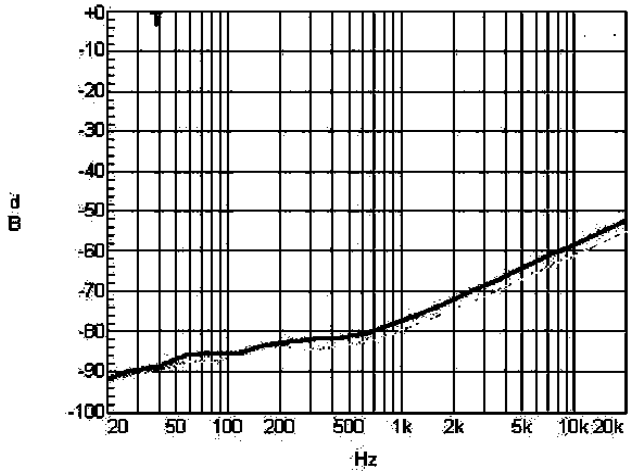


Figure 21. PSRR vs. Freq
SE mode, 5V, 32Ohm, 200mVpp
Input unterminated

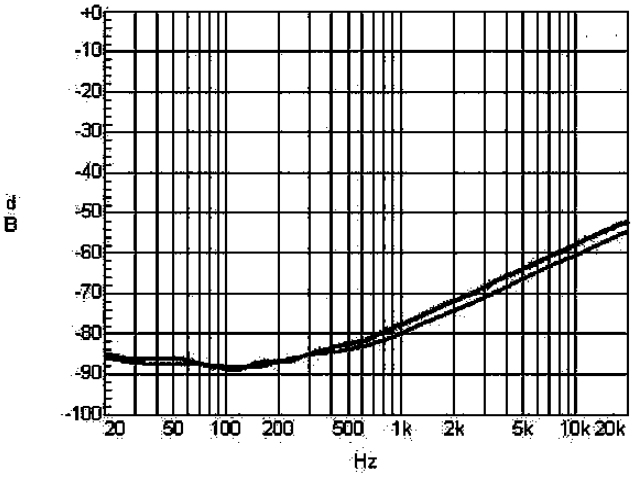


Figure 22. PSRR vs. Freq
SE mode, 3V, 32Ohm, 200mVpp
Input unterminated

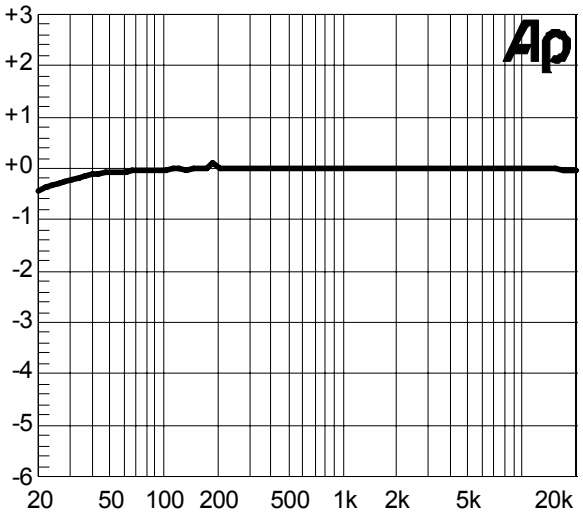


Figure 23. Frequency Response
BTL mode, 5V, 8Ohm

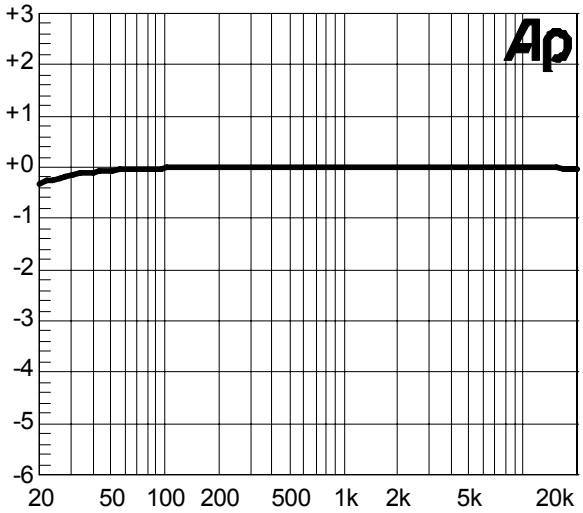


Figure 24. Frequency Response
BTL mode, 3V, 8Ohm

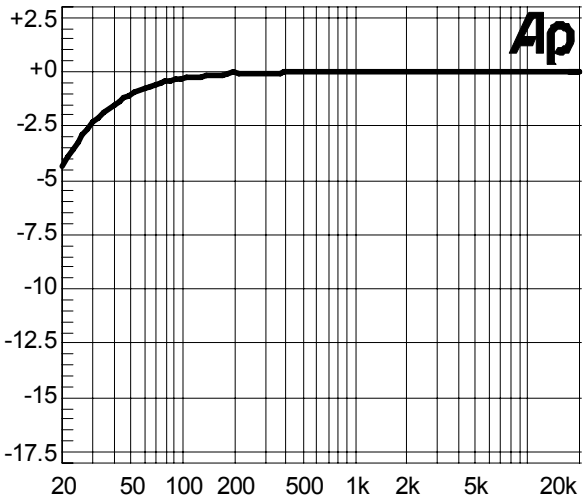


Figure 25. Frequency Response
SE mode, 5V, 32Ohm, C5/C6=220uF

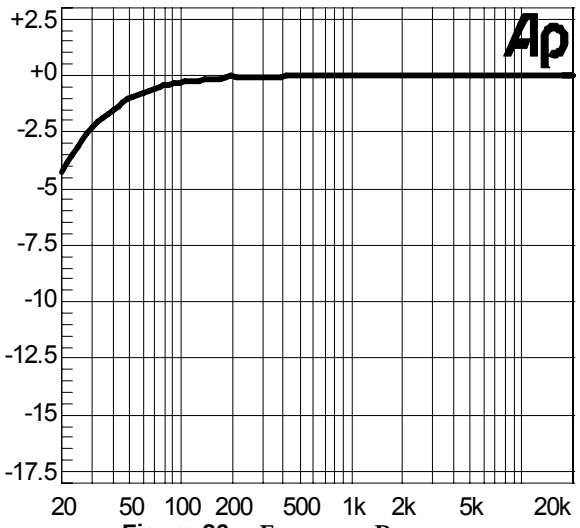


Figure 26. Frequency Response
SE mode, 3V, 32Ohm, C5/C6=220uF

Typical Performance Characteristics (Continued)

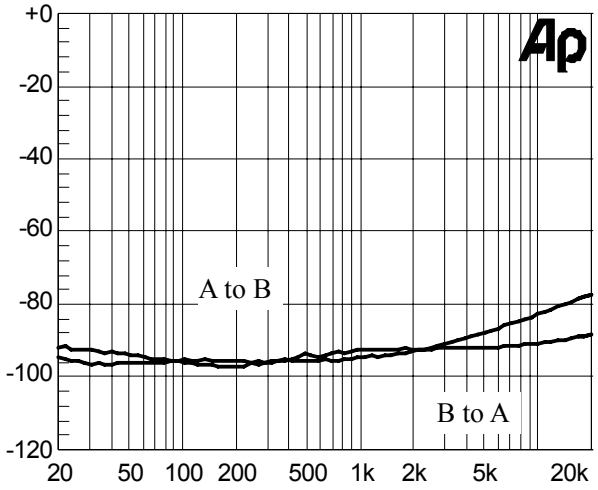


Figure 27. Crosstalk
BTL mode, 5V, 8Ohm, Po=1W

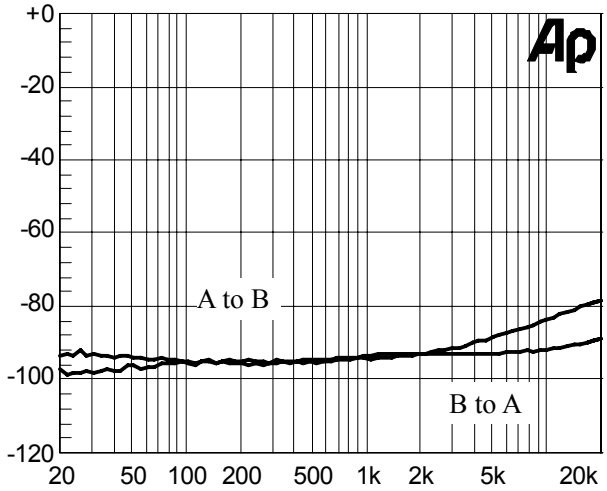


Figure 28. Crosstalk
BTL mode, 3V, 8Ohm, Po=0.3W

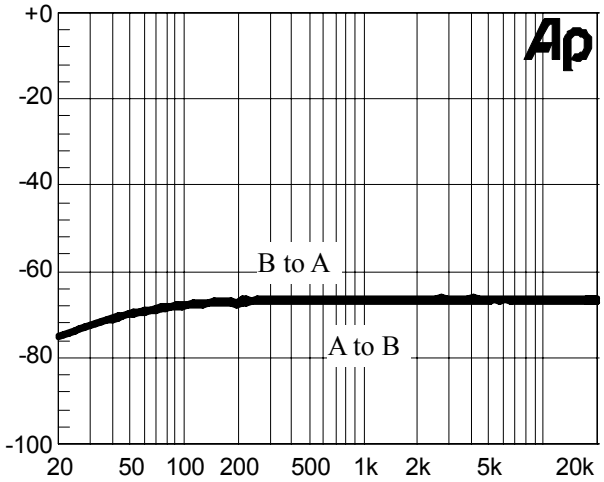


Figure 29. Crosstalk
SE mode, 5V, 32Ohm, Po=80mW

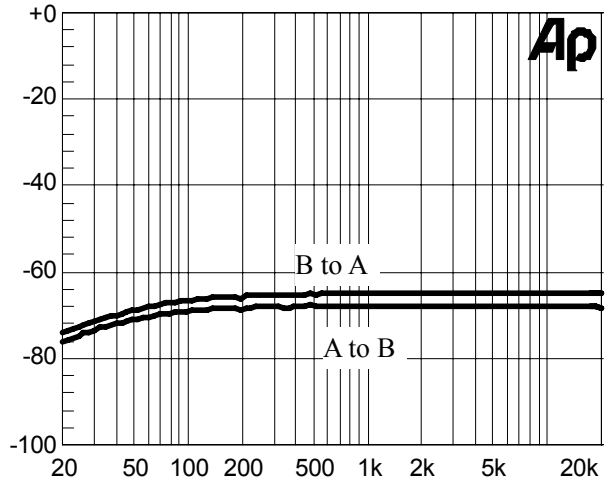


Figure 30. Crosstalk
SE mode, 3V, 32Ohm, Po=30mW

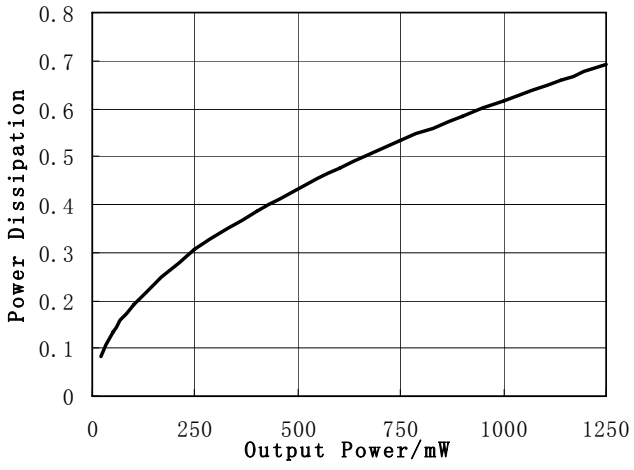


Figure 31. Power Dissipation vs. Output Power
BTL mode, 5V, f=1 kHz, RL=8Ohm, THD+N<=1%

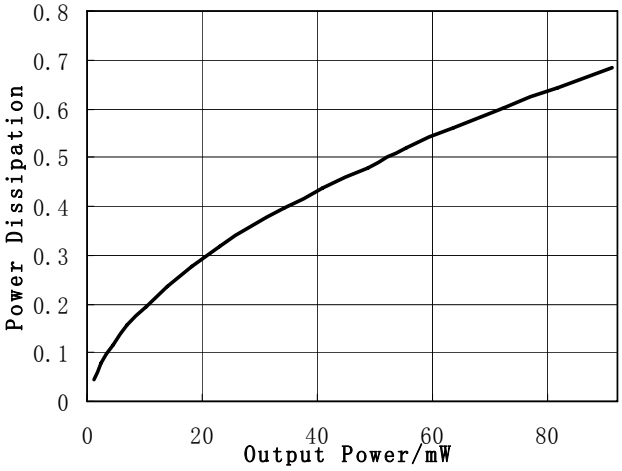


Figure 32. Power Dissipation vs. Output Power
SE mode, 5V, f=1 kHz, RL=32Ohm

Typical Performance Characteristics (Continued)

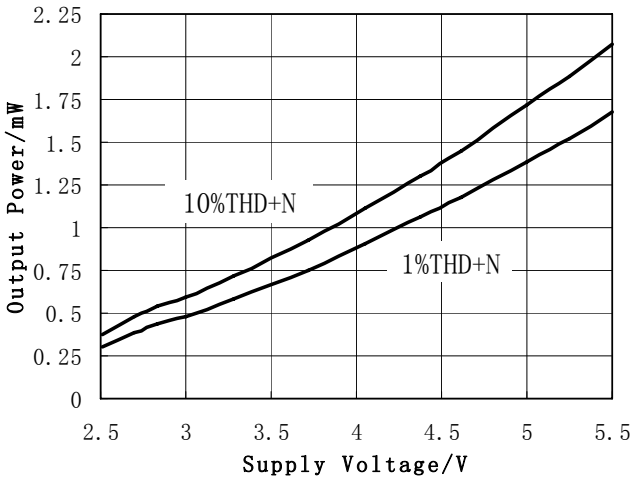


Figure 31. Output Power vs. Power Supply
BTL mode, f=1 kHz, RL=8 Ohm

Application Information

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The SN4088A's QFN (die attach paddle) package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air.

The QFN package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 2, the SN4088 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors R2, R4 and input resistors R1 and R3 set the closed-loop gain of Amp A (-out) and Amp B (-out) whereas two internal 20kΩ resistors set Amp A's (+out) and Amp B's (+out) gain at 1. The SN4088 drives a load, such speaker, connected between the two amplifier outputs, −OUTA and +OUTA.

Figure 2 shows that Amp A's (-out) output serves as Amp A's (+out) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$AVD = 2 * (Rf/Ri) \qquad (1)$$

or

$$AVD = 2 * (R2/R1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single ended amplifier operating at a given supply voltage and driving a specified output load.

$$PDMAX = (VDD)^2/(2\pi^2 RL) \quad \text{Single-Ended} \qquad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The SN4088A has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and an 8Ω load, the maximum single ended amplifier power dissipation is 0.63W or 1.23W for BTL mode per channel.

$$PDMAX = 4 * (VDD)^2/(2\pi^2 RL) \quad \text{Bridge Mode} \qquad (3)$$

The SN4088A's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the Stereo Mode. And in stereo mode, twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$PDMAX' = (TJMAX - TA)/\theta JA \qquad (4)$$

The SN4088A's TJMAX = 150°C. In the QFN package soldered to a DAP pad that expands to a copper area of 5in2 on a PCB, the SN4088A's θJA is 20°C/W. At any given ambient temperature TA, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging

Equation (4) and substituting PDMAX for PDMAX' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the SN4088A's maximum junction temperature.

$$TA = TJMAX - 2*PDMAX\ \theta JA \qquad (5)$$

For a typical application with a 5V power supply and a 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the QFN package.

$$TJMAX = PDMAX\ \theta JA + TA \qquad (6)$$

Equation (6) gives the maximum junction temperature TJMAX. If the result violates the SN4088A's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θJA. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heat sinks such as the Thermally 7106D can also improve power dissipation. When adding a heat sink, the θJA is the sum of θJC, θCS, and θSA. (θJC is the junction-to-case thermal impedance, θCS is the case-to-sink thermal impedance, and θSA is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 μF in parallel with a 0.1 μF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 μF tantalum bypass capacitance connected between the SN4088A's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation.

Keep the length of leads and traces that connect capacitors between the SN4088A's power supply pin and ground as short as possible.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the SN4088A's shutdown function. Activate micro-power shutdown by applying GND to the SHUTDOWN pin. When active, the SN4088A's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.04 μA typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the SHUTDOWN pin. Table 1 shows the logic signal levels that activate and deactivate micro-power shutdown and headphone amplifier operation.

There are a few ways to control the micro-power shutdown.

These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100k resistor between the SHUTDOWN pin and GND. Select normal amplifier operation by closing the switch. Opening the switch sets the SHUTDOWN pin to GND through the 100k resistor, which activates the micropower shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Shut down Pin	Headphone Jack Sense Pin	Operational Shutdown mode
Logic High	Low(HP not Plugged in)	Bridged /BTL
Logic High	High(HP Plugged in)	Single Ended
Logic Low	Don't care	Micro Power Shutdown

Applying a logic level to the SN4088A's HP Sense headphone control pin turns off Amp A (+out) and Amp B (+out) muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 2-1 shows the implementation of the SN4088A's headphone control function. With no headphones connected to the headphone jack, the R5-R8 voltage divider sets the voltage applied to the HP Sense pin (pin 14) at approximately 50mV. This 50mV enables Amp A (+out) and Amp B (+out) placing the SN4088A in bridged mode operation.

While the SN4088A operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false single ended trigger. Connecting headphones to the Headphone jack disconnects the headphone jack contact pin from −OUTA and allows R7. to pull the HP Sense pin up to VDD

This enables the headphone function, turns off Amp A (+out) and Amp B (+out) which mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistors R5 and R6. These resistors have negligible effect on the SN4088A's output drive capability since the typical impedance of headphones is 32Ω.

Figure 2-1 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return.

A headphone jack with one control pin contact is sufficient to drive the HP Sense pin when connecting headphones.

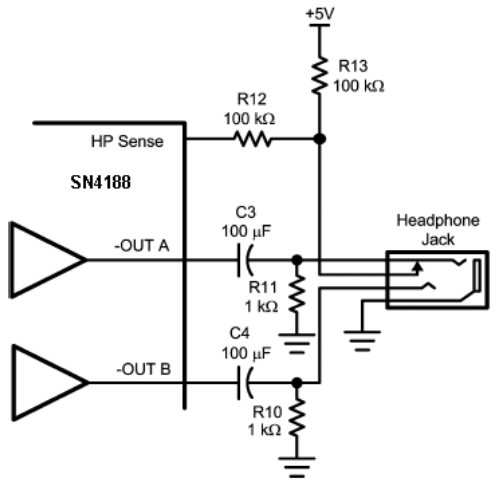


Figure2-1 Headphone Circuit

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the SN4088A's performance requires properly selecting external components. Though the SN4088A operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The SN4088A is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio.

These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1VRMS (2.83VP-P). Please refer to the Audio Power Amplifier Design section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C1 and C2) in Figure 2. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor. Besides effecting system cost and size, C1 and C2 have an effect on the SN4088A's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually VDD/2) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors, R2 and R8. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

A shown in Figure 2, the input resistors (R1, 4, 5, and 6) and the input capacitors, C1 and C2 produce a −3dB high pass filter cutoff frequency that is found using Equation (7).

$$F_{-3dB} = 1/2\pi RinCin = 1/2\pi R1C1 \qquad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz, C1, using Equation (7) is 0.053µF. The 0.33µF C1 shown in Figure 2 allows the SN4088A to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C6, the capacitor connected to the BYPASS pin. Since C6 determines how fast the SN4088A settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the SN4088A's outputs ramp to their quiescent DC voltage (nominally 1/2 VDD), the smaller the turn-on pop. Choosing C6 equal to 1.0 µF along with a small value of C1 (in the range of 0.1 µF to 0.39 µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C1 no larger than necessary for the desired bandwidth helps minimize clicks and pops. Connecting a 1µF capacitor, C6, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The SN4088A contains circuitry that minimizes turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 VDD. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C6 alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C6 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C6 increases, the turn-on time increases. There is a linear relationship between the size of C6 and the turn-on time. Here are some typical turn-on times for various values of C6 (all tested at VDD=5V):

C6	T_{ON}
0.01µF	13ms
0.1µF	26ms
0.22µF	44ms
0.47µF	68ms
1.0µF	113 ms

In order to eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching VDD on and off may not allow the capacitors to fully discharge, which may cause "clicks and pops".

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load. The following are the desired operational parameters:

Power Output:	1WRMS
Load Impedance:	8Ω
Input Level:	1Vrms
Input Impedance:	20kΩ
Bandwidth:	100Hz−20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs. Supply Voltage curve in the **Typical Performance Characteristics** section. Another way, using Equation (8), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs. Supply Voltage in the Typical Performance Characteristics curves, must be added to the result obtained by Equation (8). The result is in Equation (9).

$$V_{OUTPEAK} = \sqrt{(2R_L P_O)} \quad (8)$$

$$VDD \geq (VOUTPEAK + (VODTOP + VODBOT)) \quad (9)$$

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.35V for a 1W output at 1% THD+N. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the SN4088A to produce peak output power in excess of 1.2W at 5V of VDD and 1% THD+N without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the **Power Dissipation** section.

After satisfying the SN4088A's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation (10).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (10)$$

Thus, a minimum gain of 2.83 allows the SN4088A's to reach full output swing and maintain low noise and THD+N performance. For this example, let AVD = 3.

The amplifier's overall gain (non Stereo Enhanced mode) is set using the input (R1 and R9) and feedback resistors R2 and R8. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R2/R1 = AVD/2 \quad (11)$$

The value of Rf is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

fL = 100Hz/5 = 20Hz

and an

fH = 20kHz*5 = 100kHz.

As mentioned in the External Components section, R1 and C1 create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the coupling capacitor's value using Equation (12).

$C1 \geq 1/(2\pi R1fL)$ (12)

The result is

$1/(2\pi*20k\Omega*20Hz) = 0.398\mu F$.

Use a 0.39μF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100 kHz in this example) and the differential gain, AVD, determines the upper pass band response limit. With AVD = 3 and fH = 100 kHz, the closed-loop gain bandwidth product (GBWP) is 300 kHz. This is less than the SN4088A's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

Stereo Enhanced Stereo ENHANCEMENT

The SN4088A features a Stereo Enhanced audio enhancement effect that widens the perceived soundstage from a stereo audio signal.

The Stereo Enhanced audio enhancement improves the apparent stereo channel separation whenever the left and right speakers are too close to one another, due to system size constraints or equipment limitations.

An external RC network, Shown in figure 2, is required to enable the Stereo Enhanced effect. The amount of the Stereo Enhanced effect is set by the R5 and C7 or Cadj. Decreasing the value of R5 will increase the Stereo Enhanced effect. Increasing the value of the capacitors (C7 or Cadj) will decrease the low cutoff frequency at which the Stereo Enhanced effect starts to occur., as shown by Equation 13.

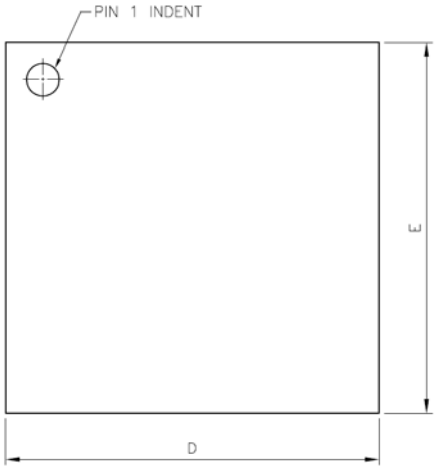
$F(-3dB) = 1 / 2\pi R5*Cadj$ (13)

The amount of perceived Stereo Enhanced is also dependent on many other factors such as speaker placement and the distance to the listener. Therefore, it is recommended that the user try various values of R5 and Cadj to get a feel for how the Stereo Enhanced effect works in the application. There is not a "right or wrong" for the effect, it is merely what is most pleasing to the individual user. Take note that R3 and R4 replace R2, and R7 and R6 replace R8 when Stereo Enhanced mode is enabled.

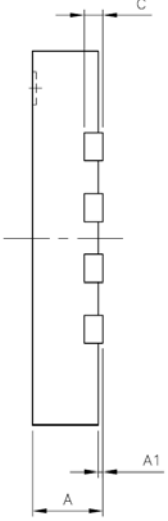
Package Information:

QFN-16

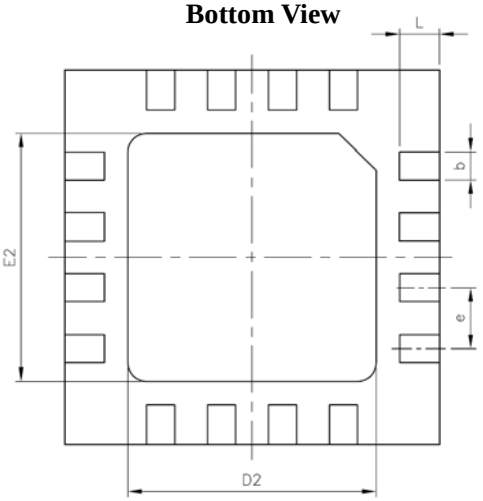
Top View



Side View



Bottom View



Symbol	Dimension (mm)		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
C	——	0.02 REF.	——
D	3.90	4.00	4.10
D2	2.00	2.65	2.80
E	3.90	4.00	4.10
E2	2.00	2.65	2.80
e	——	0.65	——
L	0.30	0.425	0.65
y	0.00	——	0.076