1.2W Audio Power Amplifier with Active-low Shutdown Mode

General Description

The SN4990D has been designed for demanding audio applications such as mobile phones and permits the reduction of the number of external components.

It is capable of delivering 1.2W of continuous RMS output power into an 8Ω load @ 5V.

An externally-controlled shutdown mode reduces the supply current to less than 1μA. It also includes internal thermal shutdown protection.

The unity-gain stable amplifier can be configured by external gain setting resistors.

Features

- Operating from V_{DD} = 2.7V to 5.5V
- 1.2W output power @ V_{DD} = 5V, THD+N= 1%, f = 1kHz, with 8Ω load
- Ultra-low consumption in shutdown mode (1μA)
- Near-zero pop & click
- Ultra-low distortion
- Unity gain stable
- UTQFN-9L (1.5mm × 1.5mm) package

Applications

- Mobile phones
- PDAs
- Portable electronic devices
- Notebook computer

Typical Application Circuit

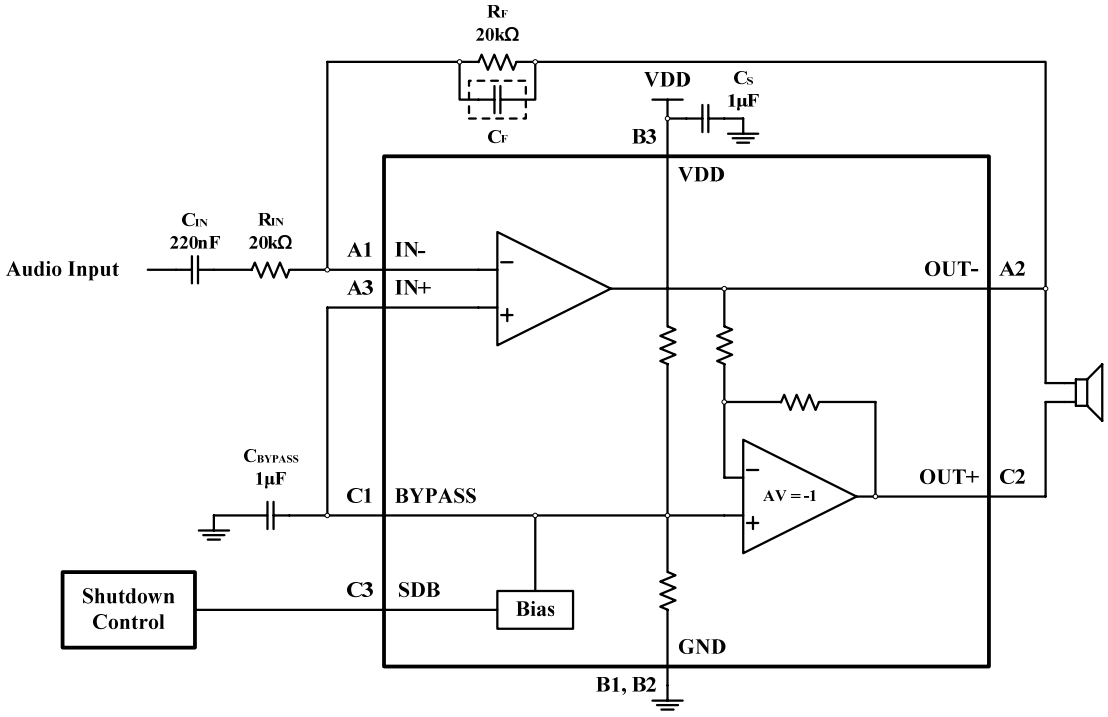
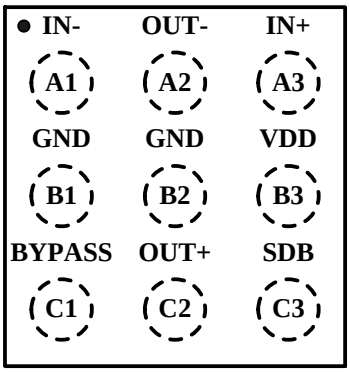


Figure 1 Typical Application Circuit

Pin Configuration

Package	Pin Configuration (Top View)
UTQFN-9L	

Pin Description

No.	Pin	I/O	Function Description
A1	IN−	I	Negative input of the first amplifier. Connected to the feedback resistor R_F and to the input resistor R_I.
A2	OUT−	O	Negative output. Connected to the load and to the feedback resistor R_F.
A3	IN+	I	Positive input of the first amplifier.
B1,B2	GND	−	Ground.
B3	VDD	−	Supply voltage.
C1	BYPASS	O	Bypass capacitor pin which provides the common mode voltage (V_{DD}/2).
C2	OUT+	O	Positive output. Connected to the load.
C3	SDB	I	The device enters in shutdown mode when a low level is applied on this pin.

Ordering Information

Order Number	Package Type	QTY/Reel	Operating Temperature Range
SN4990DIF09E	UTQFN-9L	3000	−40°C ~ +85°C

SN4990D----- [I] [F] [09] [E]

- [E] Environmental Code: E: Lead Free
- [09] Pin Code: 09: 9 Pins
- [F] Package Type: F: UTQFN-9L (1.5mm × 1.5mm)
- [I] Temperature Code: I: Industrial, −40°C ~ +85°C

Absolute Maximum Ratings *(Note 1)*

Supply voltage ---------- −0.3V ~ +6.0V
Input voltage ---------- −0.3V ~ V_{DD} + 0.3V
Thermal resistance θ_{JA}(UTQFN-9L) ---------- 52.3°C/W
Power dissipation *(Note 2)* ---------- Internally Limited
Storage temperature range---------- −65°C ~ +150°C
Junction temperature ---------- +150°C
Operation temperature range ---------- −40°C ~ +85°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

T_A = −40°C ~ +85°C, V_{DD} = 2.7V ~ 5.5V, unless otherwise noted. Typical value are T_A = +25°C.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{DD}	Power supply			2.7		5.5	V
I_{DD}	Quiescent current	V_{DD} = 5V, V_{IN} = 0V, I_O = 0A, no load				3.8	mA
		V_{DD} = 3V, V_{IN} = 0V, I_O = 0A, no load				2.8	
I_{SD}	Shutdown current	V_{SDB} = GND, no load				1	μA
V_{IH}	Shutdown voltage input high			1.4			V
V_{IL}	Shutdown voltage input low					0.4	V
V_{OS}	Output offset voltage					25	mV
Po	Output power (8Ω)	V_{DD} = 5V	THD+N = 1%, f = 1kHz		1.20		W
			THD+N = 10%, f = 1kHz		1.46		
		V_{DD} = 3V	THD+N = 1%, f = 1kHz		0.418		
			THD+N = 10%, f = 1kHz		0.607		
t_{WU}	Wake-up time *(Note 3)*	V_{DD} = 5V, C_{BYPASS} = 1μF			115		ms
		V_{DD} = 3V, C_{BYPASS} = 1μF			102		
THD+N	Total harmonic distortion + noise *(Note 3)*	V_{DD} = 5V, P_O = 0.5Wrms, f = 1kHz			0.048		%
		V_{DD} = 3V, Po = 0.3Wrms, f = 1kHz			0.021		
PSRR	Power supply rejection ratio *(Note 3)*	V_{DD} = 5V $V_{Ripple\ p\text{-}p}$ = 200mV Input grounded	f = 217Hz		51		dB
			f = 1kHz		63		
		V_{DD} = 3.6V, 4.2V $V_{Ripple\ p\text{-}p}$ = 200mV Input grounded	f = 217Hz		64		
			f = 1kHz		65		

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the SN4990D, see power derating curves for additional information.

Note 3: Guaranteed by design.

Typical Performance Characteristic

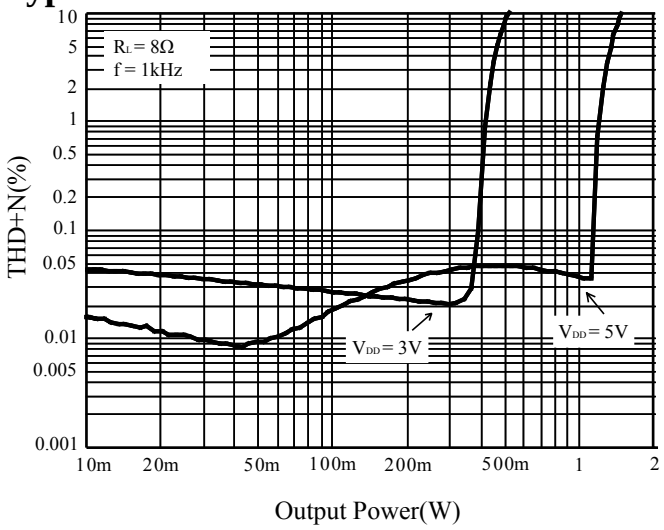


Figure 2 THD+N vs. Output Power

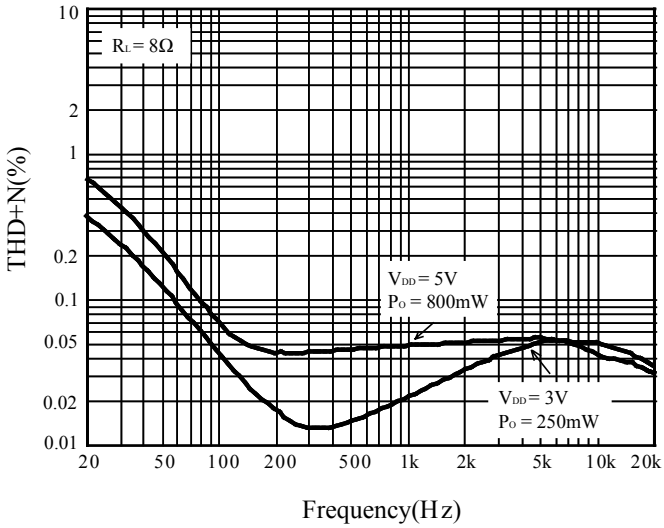


Figure 3 THD+N vs. Frequency

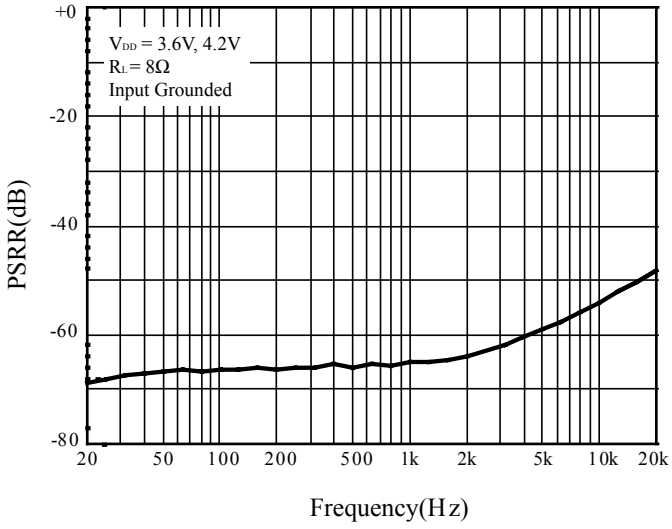


Figure 4 PSRR vs. Frequency

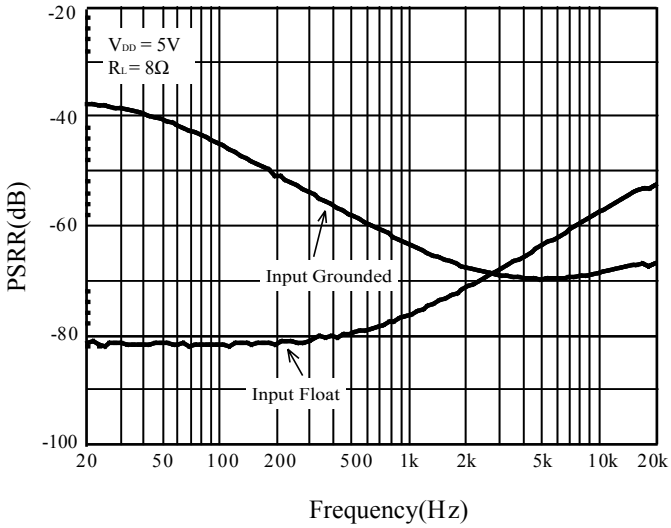


Figure 5 PSRR vs. Frequency

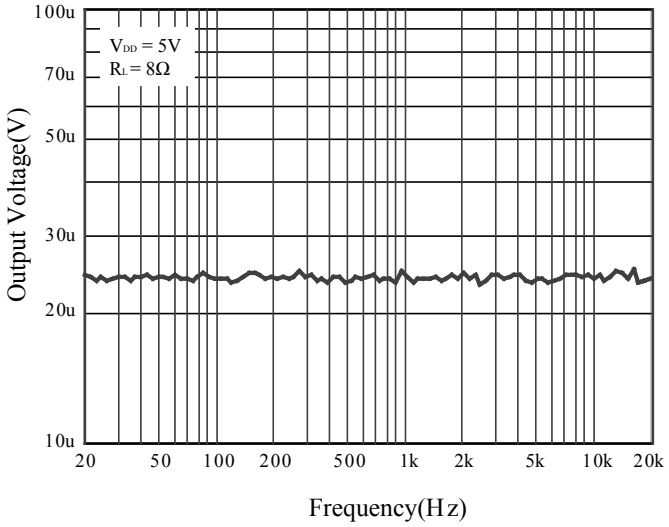


Figure 6 Noise Floor

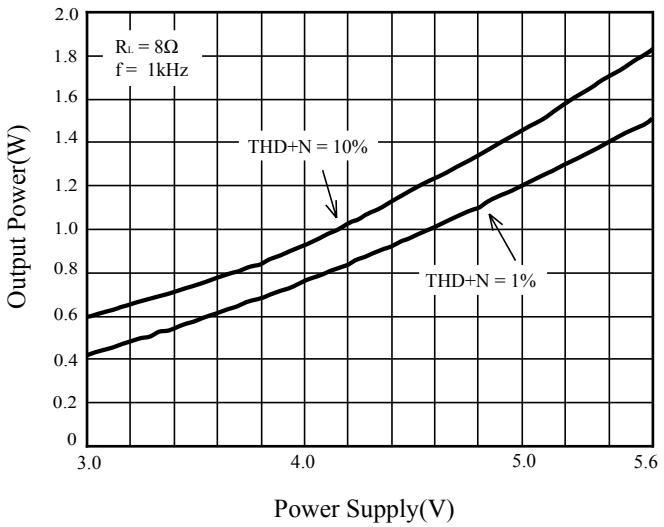


Figure 7 Output Power vs. Power Supply

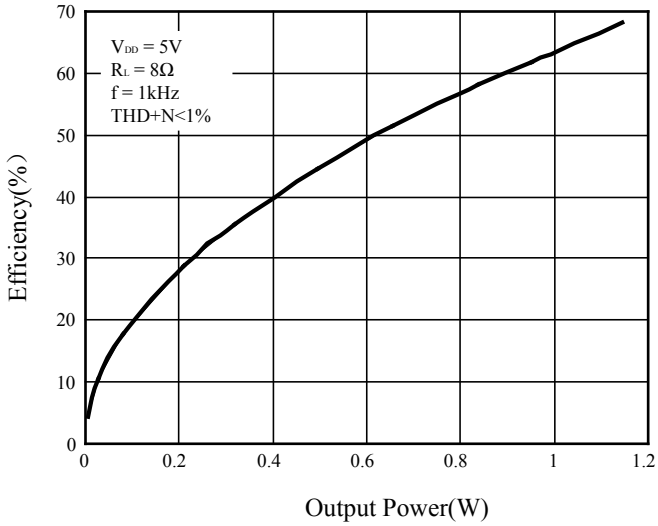


Figure 8 Efficiency vs. Output Power

Application Information

BTL Configuration Principle

The SN4990D is a monolithic power amplifier with a BTL output type. BTL (bridge tied load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single-ended output 1 = $V_{OUT+} = V_{OUT}$ (V)

Single ended output 2 = $V_{OUT-} = -V_{OUT}$ (V)

and $V_{OUT+} - V_{OUT-} = 2V_{OUT}$ (V)

The output power is:

$$P_{OUT} = \frac{(2V_{OUT\ RMS})^2}{R_L}$$

For the same power supply voltage, the output power in BTL configuration is four times higher than the output power in single ended configuration.

Gain in A Typical Application Schematic

The typical application schematic is shown in Figure 1 on page 1.

In the flat region (no C_{IN} effect), the output voltage of the first stage is (in Volts):

$$V_{OUT-} = (-V_{IN})\frac{R_F}{R_{IN}}$$

For the second stage: $V_{OUT+} = -V_{OUT-}$ (V)

The differential output voltage is (in Volts):

$$V_{OUT+} - V_{OUT-} = 2V_{IN}\frac{R_F}{R_{IN}}$$

The differential gain named gain (G_v) for more convenient usage is:

$$G_v = \frac{V_{OUT+} - V_{OUT-}}{V_{IN}} = 2V_{IN}\frac{R_F}{R_{IN}}$$

V_{OUT+} is in phase with V_{IN} and V_{OUT-} is phased 180° with V_{IN}. This means that the positive terminal of the loudspeaker should be connected to V_{OUT+} and the negative to V_{OUT-}.

Low and High Frequency Response

In the low frequency region, C_{IN} starts to have an effect. C_{IN} forms with R_{IN} a high-pass filter with a −3dB cut-off frequency. F_{CL} is in Hz.

$$F_{CL} = \frac{1}{2\pi R_{IN} C_{IN}}$$

In the high frequency region, you can limit the bandwidth by adding a capacitor (C_F) in parallel with R_F. It forms a low-pass filter with a −3dB cut-off frequency. F_{CH} is in Hz.

$$F_{CH} = \frac{1}{2\pi R_F C_F}$$

Decoupling of The Circuit

Two capacitors are needed to correctly bypass the SN4990D: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_{BYPASS}.

C_S has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1µF, you can expect THD+N levels similar to those shown in the datasheet.

In the high frequency region, if C_S is lower than 1µF, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is higher than 1µF, those disturbances on the power supply rail are more filtered.

C_{BYPASS} has an influence on THD+N at lower frequencies, but its function is critical to the final result of PSRR (with input grounded and in the lower frequency region).

If C_{BYPASS} is lower than 1µF, THD+N increases at lower frequencies and PSRR worsens.

If C_{BYPASS} is higher than 1µF, the benefit on THD+N at lower frequencies is small, but the benefit to PSRR is substantial.

Note that C_{IN} has a non-negligible effect on PSRR at lower frequencies. The lower the value of C_{IN}, the higher the PSRR is.

Wake-up Time (t_{WU})

When the SDB pin is released to put the device ON, the bypass capacitor C_{BYPASS} will not be charged immediately. As C_{BYPASS} is directly linked to the bias of the amplifier, the bias will not work properly until the C_{BYPASS} voltage is correct. The time to reach this voltage is called wake-up time or t_{WU} and specified in the electrical characteristics table with C_{BYPASS} = 1µF.

Pop Performance

Pop performance is intimately linked with the size of the input capacitor C_{IN} and the bias voltage bypass capacitor C_{BYPASS}.

The size of C_{IN} is dependent on the lower cut-off frequency and PSRR values requested. The size of C_{BYPASS} is dependent on THD+N and PSRR values requested at lower frequencies.

Moreover, C_{BYPASS} determines the speed with which the amplifier turns ON.

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

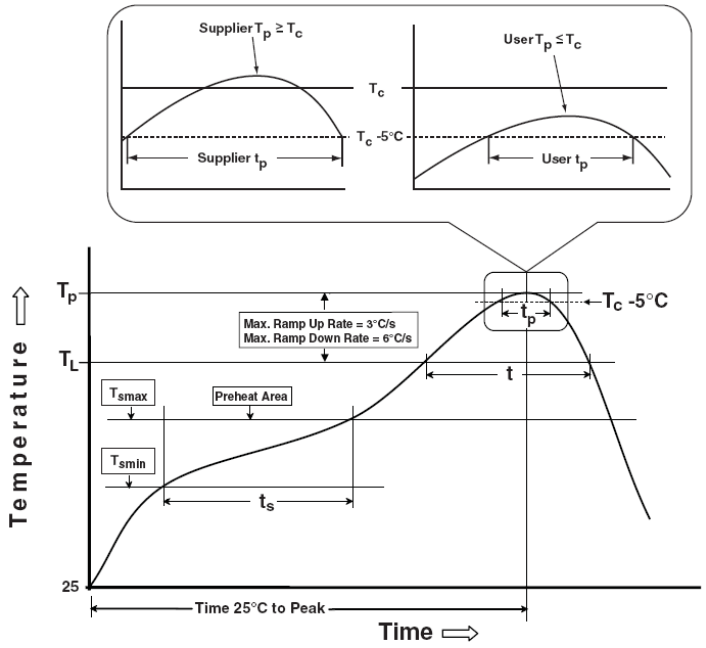
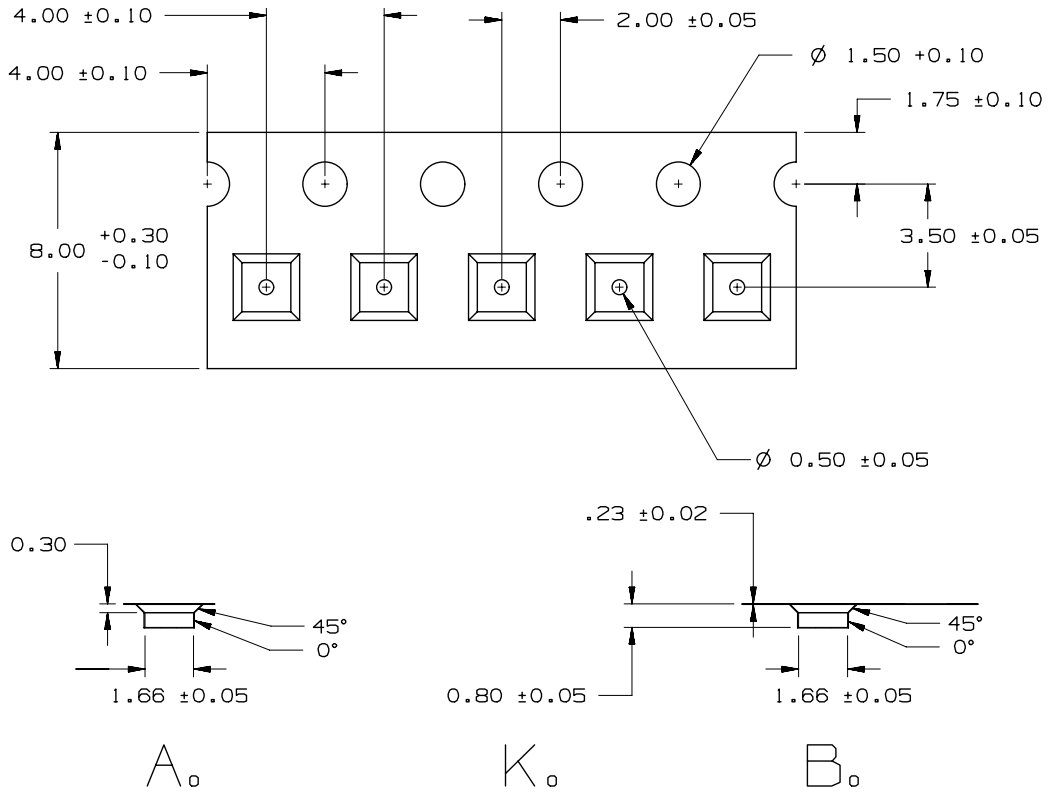
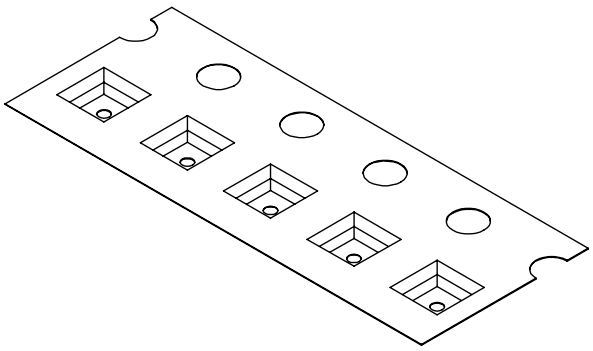


Figure 9 Classification Profile

Tape and Reel Information



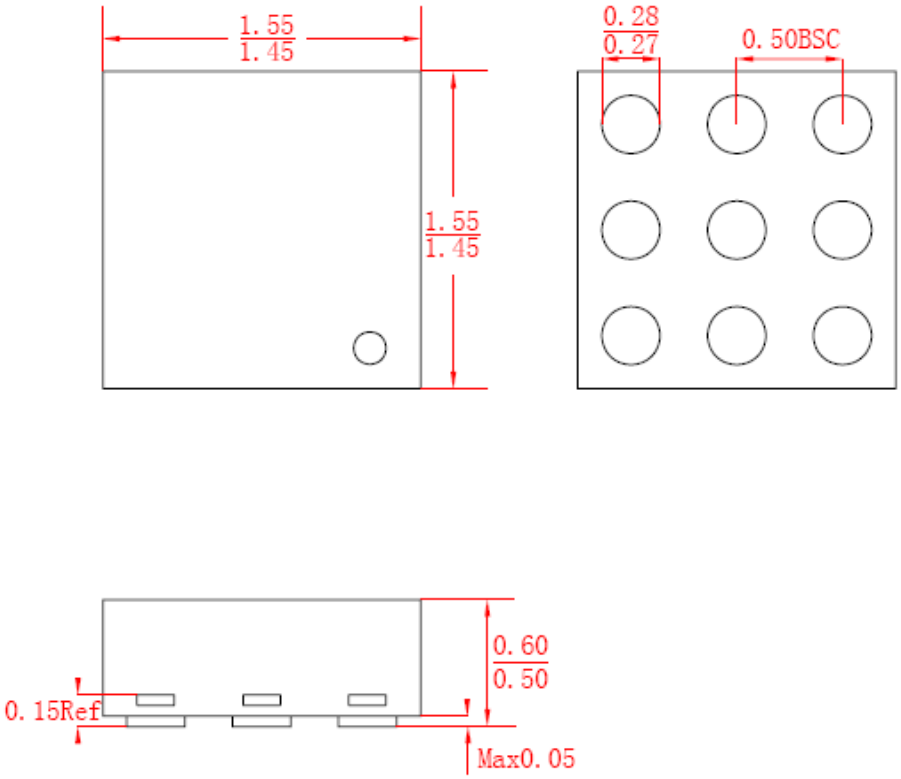


THE DIMENSIONS SHOWN ON THIS PROPOSED DRAWING ARE FOR ILLUSTRATIVE PURPOSE. DIMENSIONS FROM ACTUAL CARRIER MAY VARY SLIGHTLY.

Note: All dimensions in millimeters unless otherwise stated.

Packaging Information

UTQFN-9



Note: All dimensions in millimeters unless otherwise stated.

SI-EN 专利 UTQFN 封装 1.5mm × 1.5mm_9L SMT 贴片指导说明 Rev 4.0

超薄四方扁平及管脚微缩结构（UTQFN，Ultra Thickness Quad Flat Non-leaded）封装的 Audio PA 是矽恩微电子（SI-EN Technology Ltd）推出的可完全替代市场上所有玻璃封装（WLCSP，Wafer Level Chip Scale Package），并具有专利保护的（专利号：200920137165.8）的新产品。

为了让您更深入了解并顺利导入此产品，主要从以下 2 个方面提供此产品的使用说明：

一、产品介绍

对比 UTQFN 和 WLCSP，UTQFN 有明显的优势如下：

1. 成本更有优势
由于采用了更先进的工艺和制程，降低了芯片的面积成本，从而使得整体产品成本更有优势。

2. 交货周期更短
一般的生产周期为 4 天，与一般 QFN 产品的工艺流程基本相同，UTQFN 交货更有保障，可迅速适应大规模突发交货需求。

3. 品质更稳定
由于芯片不直接裸露在外面，所以避免了传统 WCSP 封装产品贴片使用的过程中容易崩缺、掉球等不良现象。

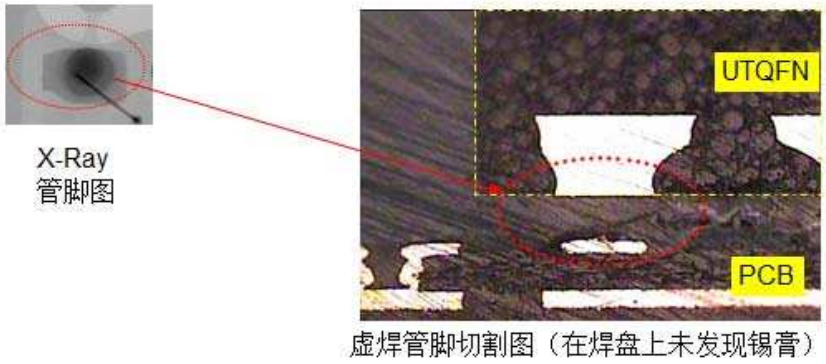
二、SMT 生产使用注意点

由于 UTQFN 的管脚结构与 QFN 类似为平面（2D）结构，与 WLCSP 的管脚的三维球（3D）结构不同，这使得贴片前需要：

1. 调整贴片机的 UTQFN 影像辨识设定

UTQFN	WLCSP
侧光为辅 垂直光为主	侧光为主 垂直光为辅

2. 注意生产过程中锡膏印刷质量的管控
WLCSP 的管脚是可塌落的焊锡球，在 reflow 过程中可以补充锡膏印刷过程中锡膏不足的问题，所以目前生产过程中一些锡膏印刷质量不好的问题并没有曝露出来，而 UTQFN 是 2D 的平面结构，会受到锡膏不足问题的影响，而表现为虚焊，如下图，某客户曾经反映 0.1%的初期量产虚焊问题，经过确认，为焊盘上没有锡膏所至，该客户通过过加强贴片厂的印刷流程品质管控后，问题得以解决。



虚焊管脚的切割图

正常产品的切割图

所以在 SMT 生产中应特别注意:

（1）印刷后的品质抽检，注意锡膏不足和印刷偏移问题。
（2）钢网的清理频率。
（3）锡膏的使用寿命，不可以超时使用（锡膏的粘稠度会显著增高）。

矽恩微电子品保工程部
2011 年 1 月

如果您对 SMT 生产有技术疑问，请发邮件到 qa@si-en.com，或者请致电：13625277602 曹先生