

# Dual 2.6W Stereo Audio Amplifier

## General Description

The SN4088D is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.6W to a 4Ω load.

The SN4088D features a low-power consumption shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce “clicks-and-pop” during device turn-on.

## Applications

- Cell phones, PDA, MP4,PMP
- Portable and desktop computers
- Desktops audio system
- Multimedia monitors

## Key Specifications

- $P_O$  at 1% THD+N,  $V_{DD} = 5V$   
 $R_L = 4\Omega$  ----- 2.1W (Typ.)  
 $R_L = 8\Omega$ ----- 1.3W (Typ.)
- $P_O$  at 10% THD+N,  $V_{DD} = 5V$   
 $R_L = 4\Omega$  ----- 2.6W (Typ.)  
 $R_L = 8\Omega$  ----- 1.6W (Typ.)
- $P_O$  at 1% THD+N,  $V_{DD} = 4V$   
 $R_L = 4\Omega$  ----- 1.4W (Typ.)  
 $R_L = 8\Omega$  ----- 0.81W (Typ.)
- Shutdown current ----- 0.04μA (Typ.)
- Supply voltage range ----- 2.7V ~ 5.5V
- QFN-16 (4mm × 4mm) package

## Features

- Suppress “click-and-pop”
- Thermal shutdown protection circuitry
- Micro power shutdown mode

## Typical Application Circuit

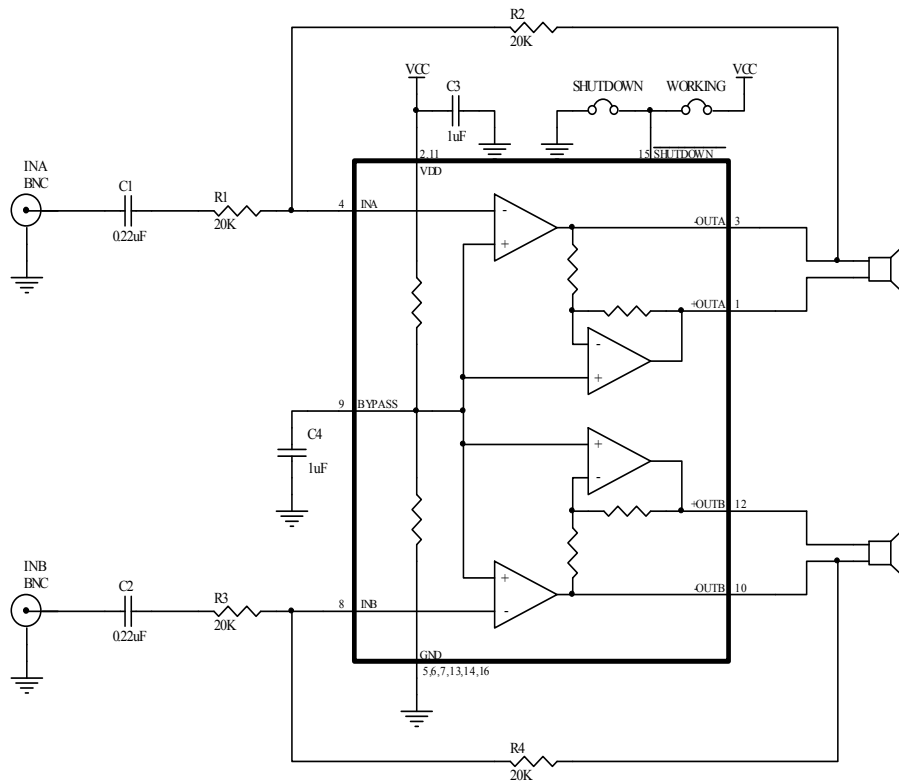
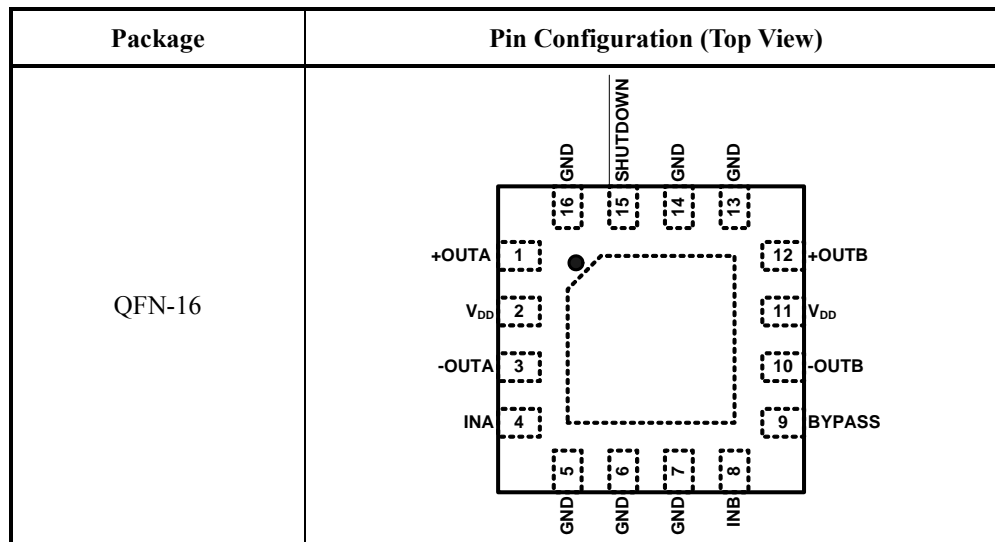


Figure 1 Typical Audio Amplifier Application Circuit

## Pin Configuration

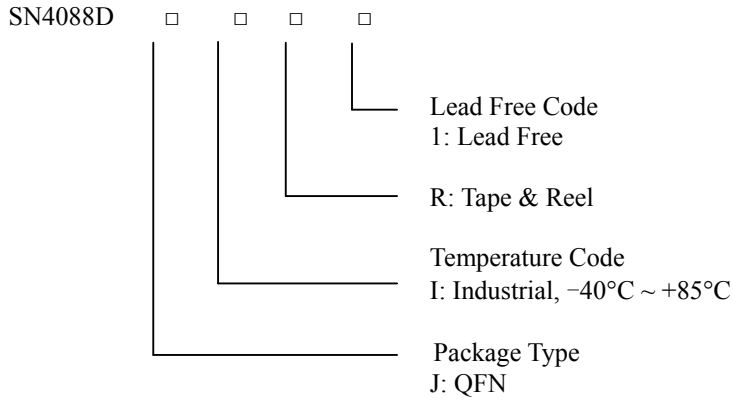


## Pin Description

No.	Pin	I/O	Description
1	+OUTA	O	Left channel +output.
2,11	V <sub>DD</sub>	-	Supply voltage.
3	-OUTA	O	Left channel -output.
4	INA	I	Left channel input.
5~7,13,14,16	GND	-	Ground.
8	INB	I	Right channel input.
9	Bypass	I	Bypass capacitor which provides the common mode voltage.
10	-OUTB	O	Right channel -output.
12	+OUTB	O	Right channel +output.
15	Shutdown	I	Shut down control, hold low for shutdown mode.
	Thermal Pad	-	Connect to GND.

Ordering Information

Order Number	Package Type	QTY/Reel	Operating Temperature Range
SN4088DJIR1	QFN-16	2500	-40°C ~ +85°C



## Absolute Maximum Ratings

Supply voltage, $V_{DD}$ -----	-0.3V ~ +6.0V
Solder information, Vapor Phase (60s) -----	215°C
Infrared (15s) -----	220°C
Storage temperature range -----	-65°C ~ +150°C
Input voltage -----	-0.3V ~ $V_{DD}+0.3V$
Junction temperature -----	150°C
Operating temperature range -----	-40°C ~ +85°C

*Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

The following specifications apply for  $V_{DD} = 5V$ , unless otherwise noted. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Typ.	Limit	Unit
$V_{DD}$	Supply voltage			2.7	V (Min.)
				5.5	V (Max.)
$I_{DD}$	Quiescent power supply current	$V_{IN} = 0V, I_o = 0A$	4.5	10.5	mA (Max.)
$I_{SD}$	Shutdown current	GND applied to the shutdown pin	0.1	1	$\mu A$ (Max.)
$V_{IH}$	Shutdown input voltage high			1.4	V (Min.)
$V_{IL}$	Shutdown input voltage low			0.4	V (Max.)
$T_{WU}$	Turn on time	1 $\mu F$ bypass cap(C4)	120		ms

## Electrical Characteristics Operation

The following specifications apply for  $V_{DD} = 5V$ , unless otherwise noted. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Typ.	Limit	Unit
$V_{os}$	Output offset voltage	$V_{IN} = 0V$	5	25	mV (Max.)
$P_o$	Output power	THD+N = 1%, $f = 1kHz, R_L = 8\Omega$	1.3	1.15	W (Min.)
		THD+N = 10%, $f = 1kHz, R_L = 8\Omega$	1.6	1.45	W (Min.)
		THD+N = 1%, $f = 1kHz, R_L = 4\Omega$	2.1	1.95	W (Min.)
		THD+N = 10%, $f = 1kHz, R_L = 4\Omega$	2.6	2.45	W (Min.)
THD+N	Total harmonic distortion +noise	1kHz, $A_{vd} = 2, R_L = 8\Omega, P_o = 1W$	0.1		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	80		dB
		Input floating 1kHz, $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	70		dB
		Input GND 217Hz, $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	60		dB
		Input GND 1kHz $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	60		dB
$X_{talk}$	Channel separation	$f = 1kHz, C4 = 1\mu F$	-100		dB
$V_{NO}$	Output noise voltage	1kHz, A-weighted	7		$\mu V$

## Electrical Characteristics

The following specifications apply for  $V_{DD} = 3V$ , unless otherwise noted. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Typ.	Limit	Unit
$I_{DD}$	Quiescent power supply current	$V_{IN} = 0V, I_O = 0A$	3.8		mA
$I_{SD}$	Shutdown current	GND applied to the shutdown pin	0.1		$\mu A$
$V_{IH}$	Shutdown input voltage high			1.1	V (Min.)
$V_{IL}$	Shutdown input voltage low			0.4	V (Max.)
$T_{WU}$	Turn on time	1 $\mu F$ bypass cap(C4)	110		ms

## Electrical Characteristics Operation

The following specifications apply for  $V_{DD} = 3V$ , unless otherwise noted. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Condition	Typ.	Limit	Unit
$V_{os}$	Output offset voltage	$V_{IN} = 0V$	2.5		mV
$P_o$	Output power	THD+N = 1%, $f = 1kHz, R_L = 8\Omega$	0.45		W
		THD+N = 10%, $f = 1kHz, R_L = 8\Omega$	0.56		W
		THD+N = 1%, $f = 1kHz, R_L = 4\Omega$	0.74		W
		THD+N = 10%, $f = 1kHz, R_L = 4\Omega$	0.9		W
THD+N	Total harmonic distortion+noise	1kHz, $A_{vd} = 2, R_L = 8\Omega, P_o = 0.3W$	0.18		%
PSRR	Power supply rejection ratio	Input floating, 217Hz, $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	75		dB
		Input floating 1kHz, $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	70		dB
		Input GND 217Hz, $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	60		dB
		Input GND 1kHz $V_{ripple} = 200mV_{p-p}$ C4 = 1 $\mu F, R_L = 8\Omega$	62		dB
$X_{talk}$	Channel separation	$f = 1kHz, C4 = 1\mu F$	-100		dB
$V_{NO}$	Output noise voltage	1kHz, A-weighted	7		$\mu V$

Typical Performance Characteristics

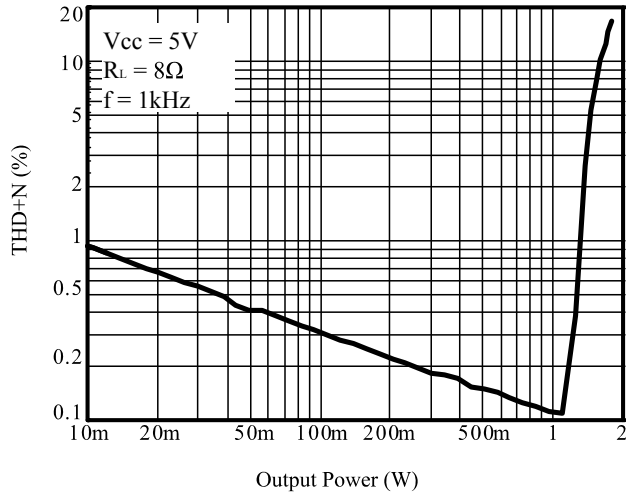


Figure 2 THD+N vs. Output Power

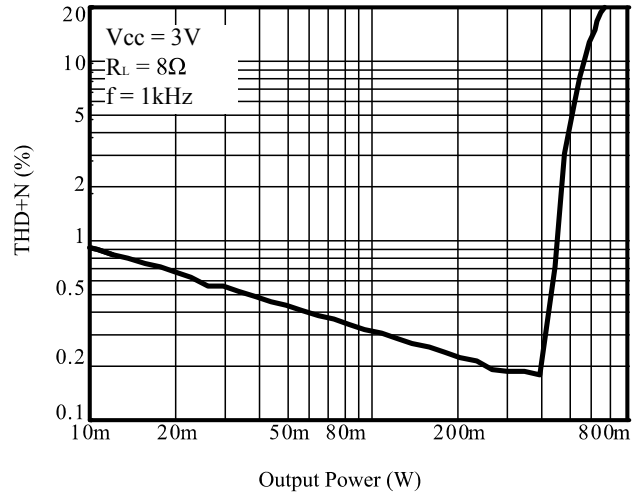


Figure 3 THD+N vs. Output Power

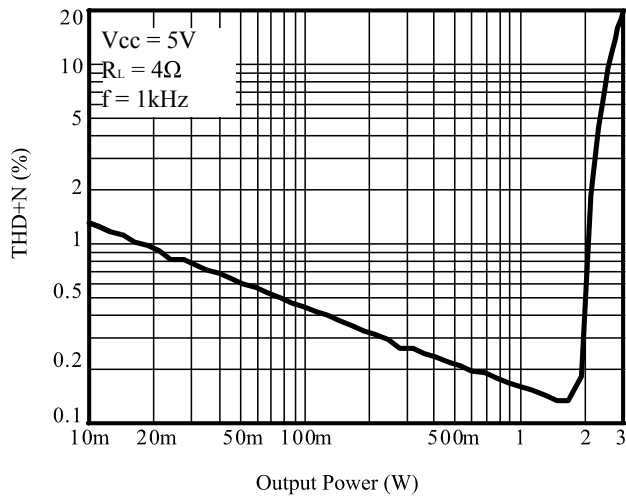


Figure 4 THD+N vs. Output Power

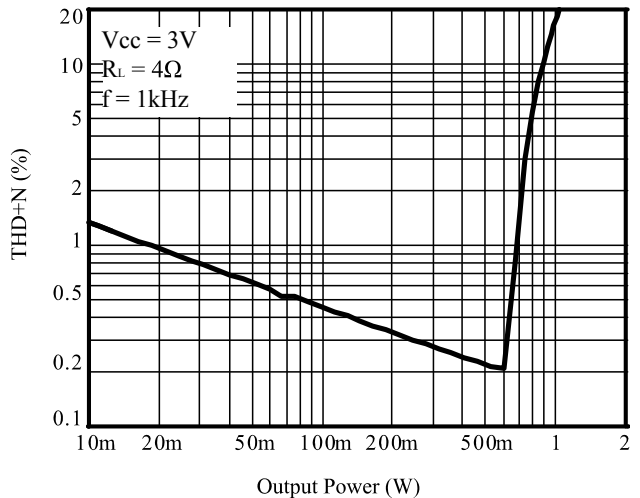


Figure 5 THD+N vs. Output Power

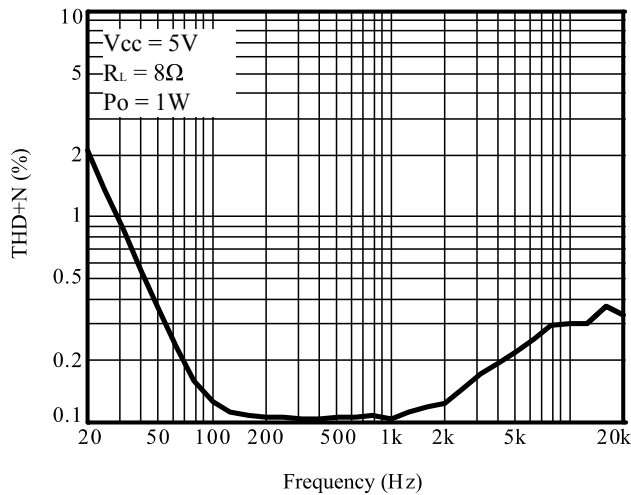


Figure 6 THD+N vs. Frequency

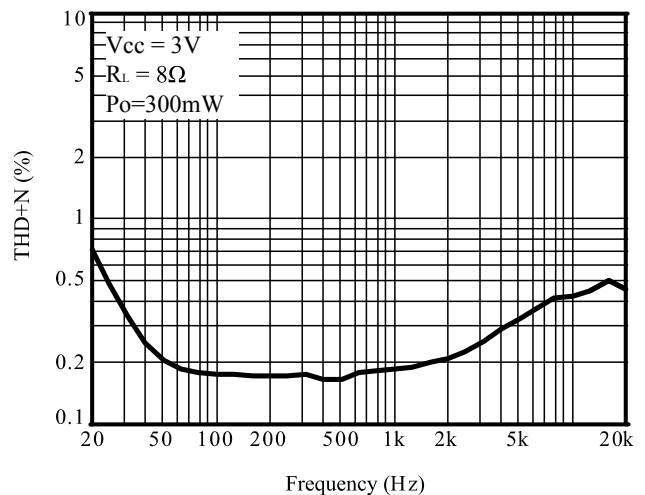


Figure 7 THD+N vs. Frequency

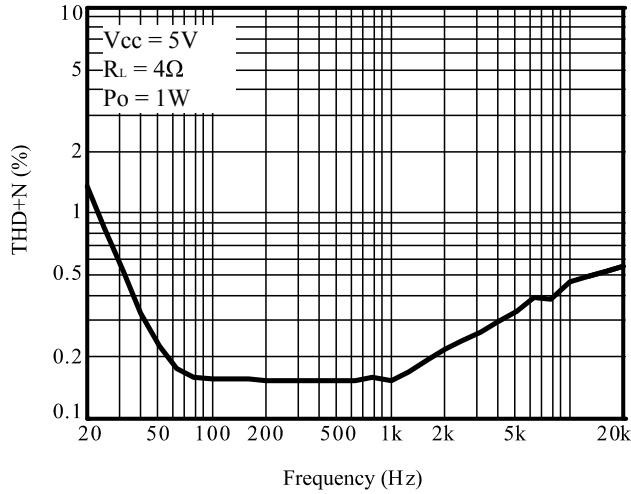


Figure 8 THD+N vs. Frequency

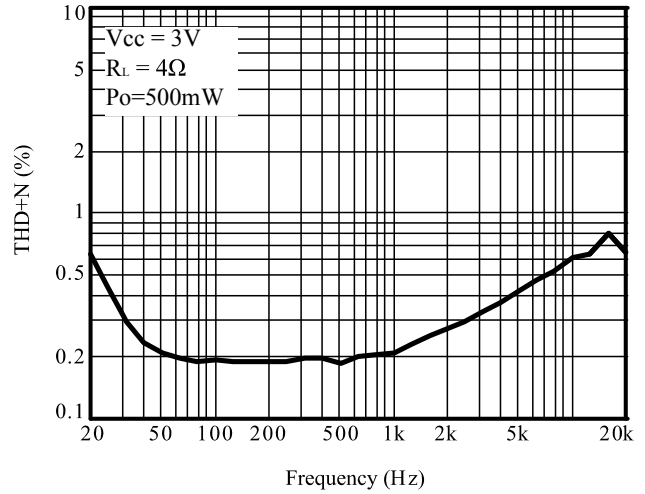


Figure 9 THD+N vs. Frequency

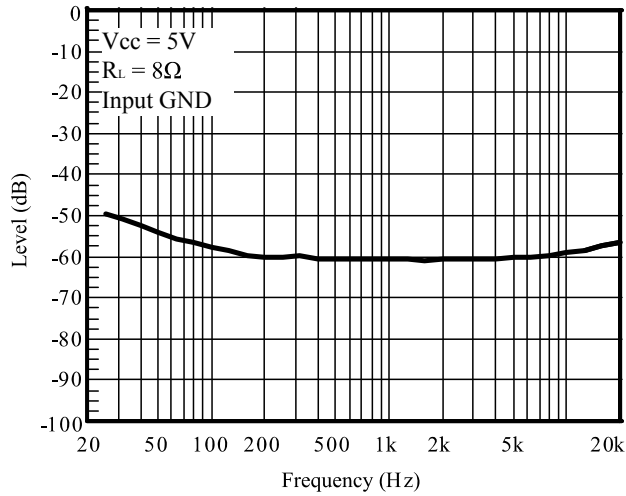


Figure 10 PSRR vs. Frequency

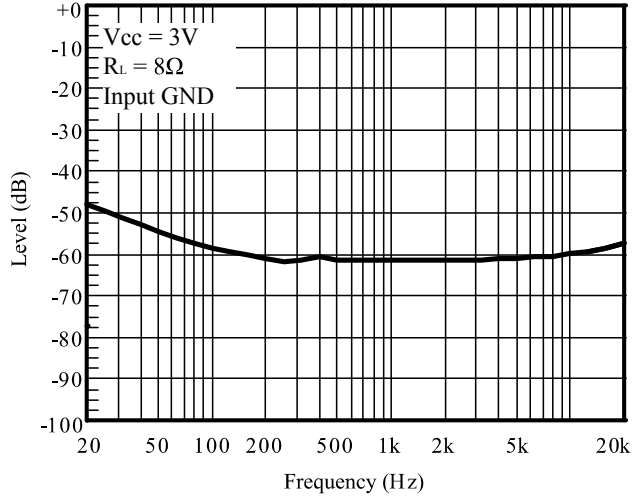


Figure 11 PSRR vs. Frequency

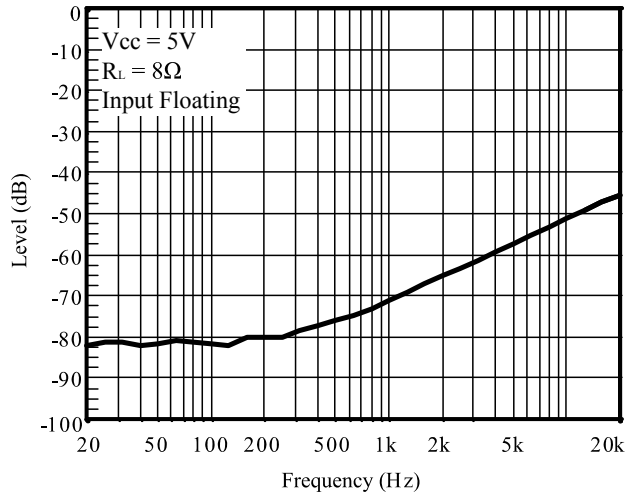


Figure 12 PSRR vs. Frequency

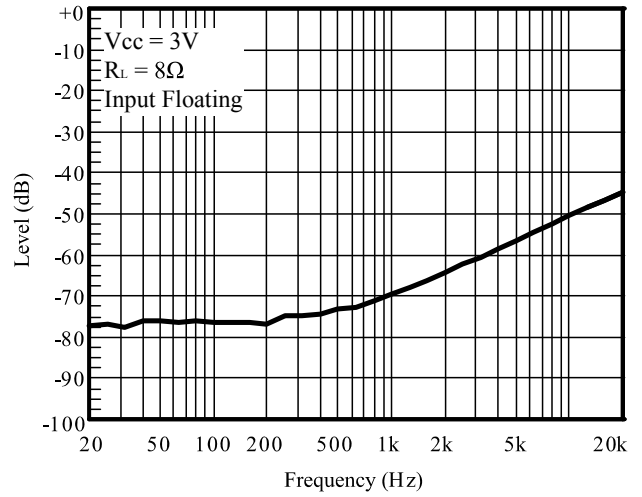


Figure 13 PSRR vs. Frequency

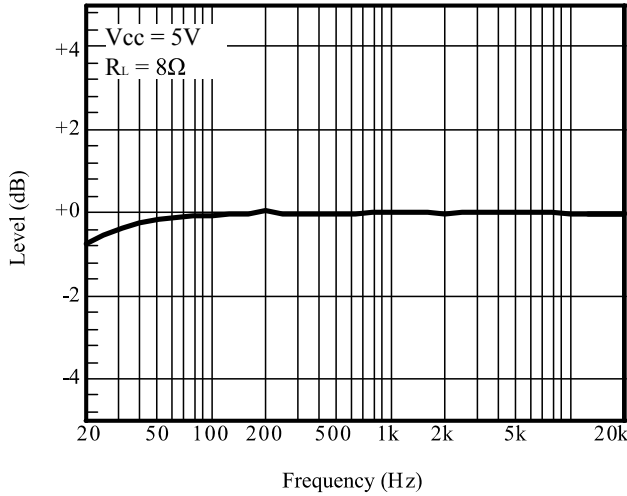


Figure 14 Frequency Response

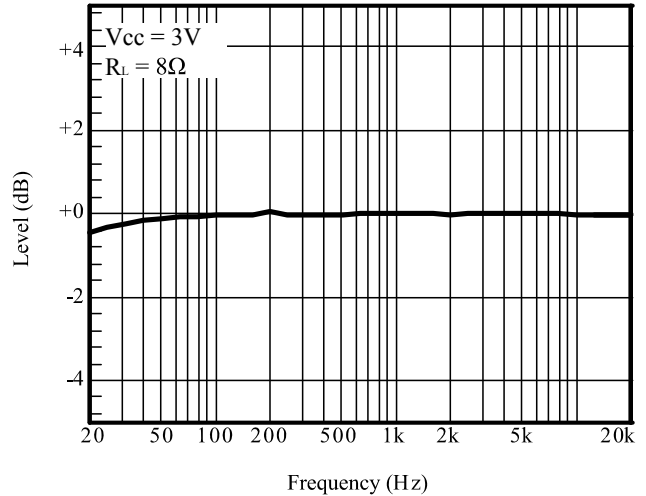


Figure 15 Frequency Response

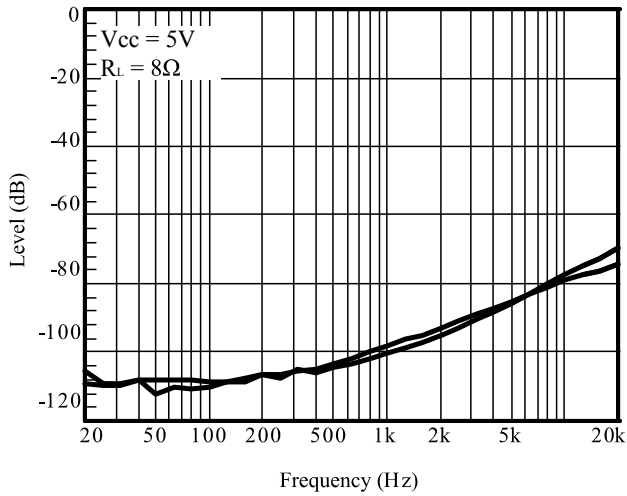


Figure 16 Crosstalk vs. Frequency

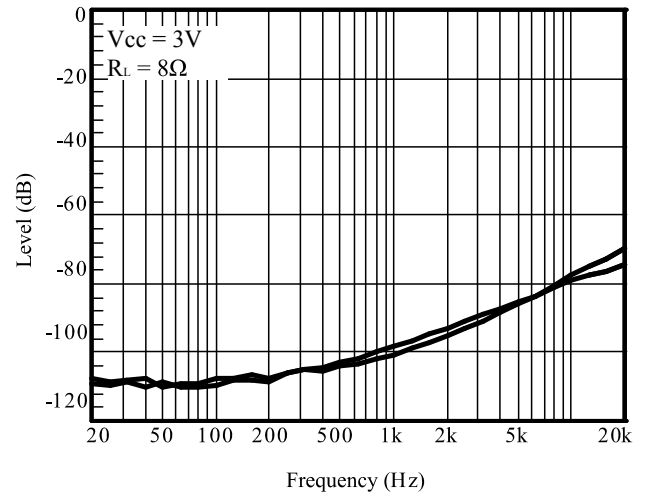


Figure 17 Crosstalk vs. Frequency

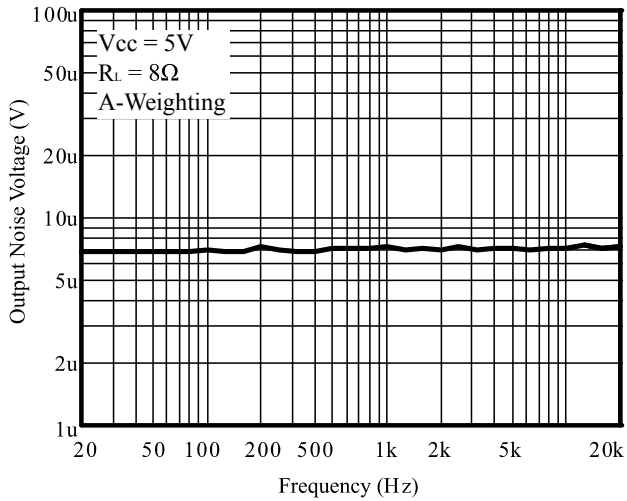


Figure 18 Noise Floor

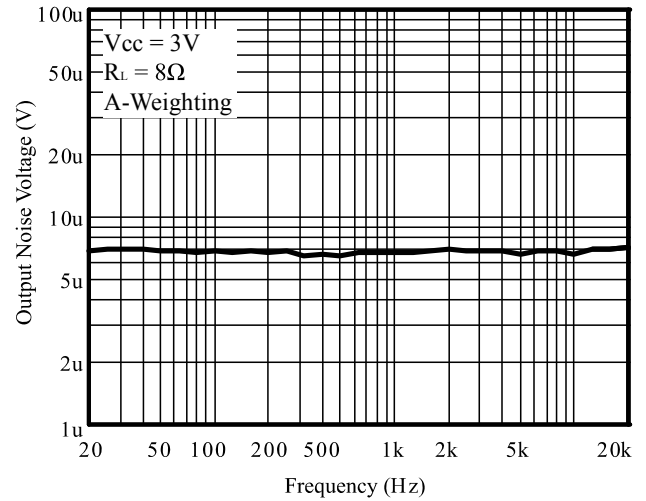


Figure 19 Noise Floor

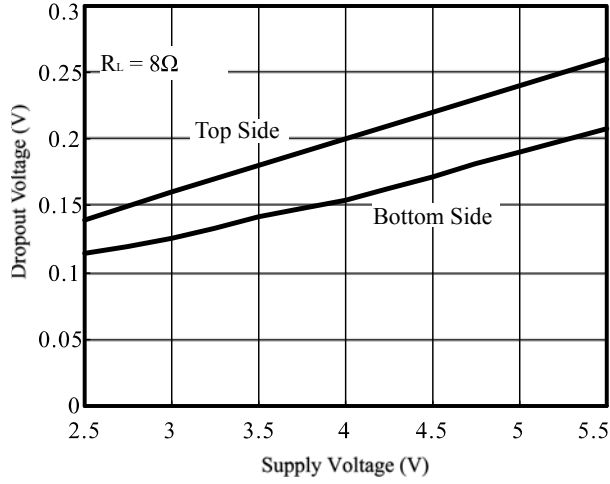


Figure 20 Dropout Voltage vs. Supply Voltage

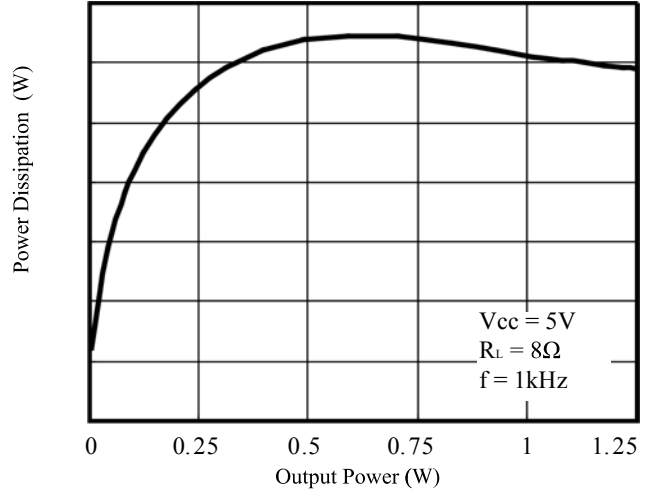


Figure 21 Power Dissipation vs. Output Power

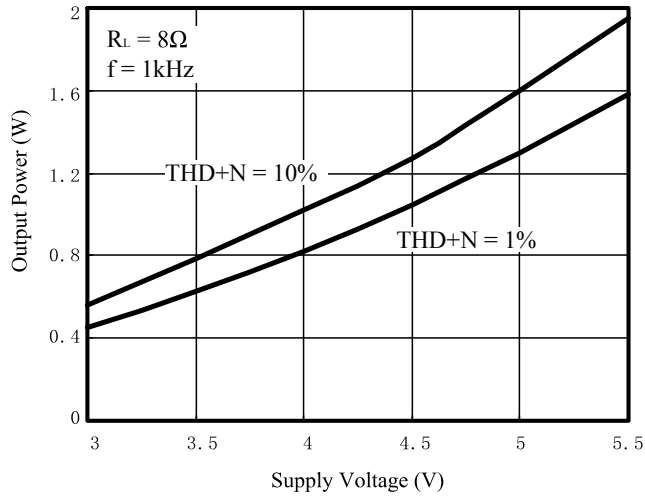


Figure 22 Output Power vs. Supply Voltage

## Application Information

### Exposed-Dap Package PCB Mounting Considerations

The SN4088D's QFN (die attach paddle) package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air.

The QFN package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers.

### Bridge Configuration Explanation

As shown in Figure 2, the SN4088D consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors  $R_2$ ,  $R_4$  and input resistors  $R_1$  and  $R_3$  set the closed-loop gain of Amp A (-out) and Amp B (-out) whereas two internal 20k $\Omega$  resistors set Amp A's (+out) and Amp B's (+out) gain at 1. The SN4088D drives a load, such speaker, connected between the two amplifier outputs, -OUTA and +OUTA.

Figure 2 shows that Amp A's (-out) output serves as Amp A's (+out) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between -OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 \times (R_f/R_i) \quad (1)$$

or

$$A_{VD} = 2 \times (R_2/R_1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply

amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

### Power Dissipation

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a single ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The SN4088D has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and an 8 $\Omega$  load, the maximum single channel power dissipation is 0.63W or 1.26W for stereo operation.

$$P_{DMAX} = 4 \times (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \quad (3)$$

The SN4088D's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The SN4088D's  $T_{JMAX} = 150^\circ\text{C}$ . In the QFN package soldered to a DAP pad that expands to a copper area of 5in<sup>2</sup> on a PCB, the SN4088D's  $\theta_{JA}$  is 20°C/W. At any given ambient temperature  $T_A$ , use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting  $P_{DMAX}$  for  $P_{DMAX}'$  results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the SN4088D's maximum junction temperature.

$$T_A = T_{JMAX} - 2 \times P_{DMAX} \theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and a 4 $\Omega$  load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the QFN package.

$$T_{JMAX} = P_{DMAX} \theta_{JA} + T_A \quad (6)$$

Equation (6) gives the maximum junction temperature  $T_{JMAX}$ . If the result violates the SN4088D's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce  $\theta_{JA}$ . The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. The  $\theta_{JA}$  is the sum of  $\theta_{JC}$ ,  $\theta_{CS}$ , and  $\theta_{SA}$ . ( $\theta_{JC}$  is the junction-to-case thermal impedance,  $\theta_{CS}$  is the case-to-sink thermal impedance, and  $\theta_{SA}$  is the sink-to-ambient thermal impedance.)

### Power Supply Bypassing

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 $\mu$ F in parallel with a 0.1 $\mu$ F filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 $\mu$ F tantalum bypass capacitance connected between the SN4088D's supply pins and ground. Keep the length of leads and traces that connect capacitors between the SN4088D's power supply pin and ground as short as possible.

### Micro-Power Shutdown

The voltage applied to the SHUTDOWN pin controls the SN4088D's shutdown function. Activate micro-power shutdown by applying GND to the SHUTDOWN pin. When active, the SN4088D's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.04 $\mu$ A typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the SHUTDOWN pin.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When use a switch, connect an external 100k $\Omega$  resistor between the SHUTDOWN pin and GND. Select normal amplifier operation by closing the switch. Opening the switch sets the SHUTDOWN pin to ground through the 100k $\Omega$  resistor, which activates the micro power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

### Selecting Proper External Components

Optimizing the SN4088D's performance requires properly selecting external components. Though the SN4088D operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The SN4088D is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of 1VRMS (2.83V<sub>P-P</sub>). Please refer to the **Audio Power Amplifier Design** section for more information on selecting the proper gain.

### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors ( $C_1$  and  $C_2$ ) in Figure 2. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size,  $C_1$  and  $C_2$  have an effect on the SN4088D's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually  $V_{DD}/2$ ) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors,  $R_2$  and  $R_4$ . Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired  $-3$ dB frequency.

As shown in Figure 2, the input resistors ( $R_1$  and  $R_3$ ) and the input capacitors ( $C_1$  and  $C_2$ ) produce a  $-3$ dB high pass filter cutoff frequency that is found using Equation (7).

$$f_{-3dB} = 1/2\pi R_{in} C_{in} = 1/2\pi R_1 C_1 \quad (7)$$

As an example when using a speaker with a low frequency limit of 150Hz,  $C_1$ , using Equation (7) is 0.053 $\mu$ F. The 0.33 $\mu$ F  $C_1$  shown in Figure 2 allows the SN4088D to drive high efficiency, full range speaker whose response extends below 30Hz.

## Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C4, the capacitor connected to the BYPASS pin. Since C4 determines how fast the SN4088D settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the SN4088D's outputs ramp to their quiescent DC voltage (nominally 1/2 V<sub>DD</sub>), the smaller the turn-on pop. Choosing C4 equal to 1.0μF along with a small value of C1 (in the range of 0.1μF to 0.39μF), produces a click-less and pop-less shutdown function. As discussed above, choosing C1 no larger than necessary for the desired band with helps minimize clicks and pops. Connecting a 1μF capacitor, C4, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR.

## Optimizing Click and Pop Reduction Performance

The SN4088D contains circuitry that minimizes turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V<sub>DD</sub>. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C4 alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C4 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C4 increases, the turn-on time increases. There is a linear relationship between the size of C4 and the turn-on time. Here are some typical turn-on times for various values of C4 (all tested at V<sub>DD</sub> = 5V).

C <sub>4</sub>	T <sub>ON</sub>
0.01μF	13ms
0.1μF	26ms
0.22μF	44ms
0.47μF	68ms
1.0μF	120 ms

In order eliminate "click-and-pop"; all capacitors must be discharged before turn-on. Rapidly switching V<sub>DD</sub> on and off may not allow the capacitors to fully discharge, which may cause "click-and-pop".

## Audio Power Amplifier Design

### Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	1W <sub>RMS</sub>
Load Impedance:	8Ω
Input Level:	1V <sub>RMS</sub>
Input Impedance:	20kΩ

Bandwidth: 100Hz~20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs. Supply Voltage curve in the **Typical Performance Characteristics** section. Another way, using Equation (8), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs. Supply Voltage in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (8). The result is in Equation (9).

$$V_{\text{OUTPEAK}} = \sqrt{2R_L P_O} \quad (8)$$

$$V_{DD} \geq V_{\text{OUTPEAK}} + (V_{\text{ODTOP}} + V_{\text{ODBOT}}) \quad (9)$$

The Output Power vs. Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.35V for a 1W output at 1% THD+N. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the SN4088D to produce peak output power in excess of 1.2W at 5V of V<sub>DD</sub> and 1% THD+N without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the **Power Dissipation** section.

After satisfying the SN4088D's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation (10).

$$A_{VD} = \sqrt{P_O R_L} / V_{IN} = V_{\text{orms}} / V_{\text{inrms}} \quad (10)$$

Thus, a minimum gain of 2.83 allows the SN4088D's to reach full output swing and maintain low noise and THD+N performance. For this example, let A<sub>VD</sub> = 3.

The amplifier's overall gain is set using the input (R<sub>1</sub> and R<sub>3</sub>) and feedback resistors R<sub>2</sub> and R<sub>4</sub>. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_2 / R_1 = A_{VD} / 2 \quad (11)$$

The value of R<sub>f</sub> is 30kΩ.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency

response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the  $\pm 0.25$ dB desired limit. The results are an

$$f_L = 100\text{Hz}/5 = 20\text{Hz}$$

and an

$$f_H = 20\text{kHz} \times 5 = 100\text{kHz}.$$

As mentioned in the **External Components** section,  $R_1$  and  $C_1$  create a high pass filter that sets the amplifier's lower band pass frequency limit. Find the coupling capacitor's value using Equation (12).

$$C_1 \geq 1/(2\pi R_1 f_L) \quad (12)$$

The result is

$$1/(2\pi \times 20\text{k}\Omega \times 20\text{Hz}) = 0.398\mu\text{F}$$

Use a  $0.39\mu\text{F}$  capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain,  $A_{VD}$ , determines the upper pass band response limit. With  $A_{VD} = 3$  and  $f_H = 100\text{kHz}$ , the closed-loop gain bandwidth product (GBWP) is 300kHz. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b>	
Temperature min (T <sub>smin</sub> )	150°C
Temperature max (T <sub>smax</sub> )	200°C
Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> )	217°C
Time at liquidous (t <sub>L</sub> )	60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

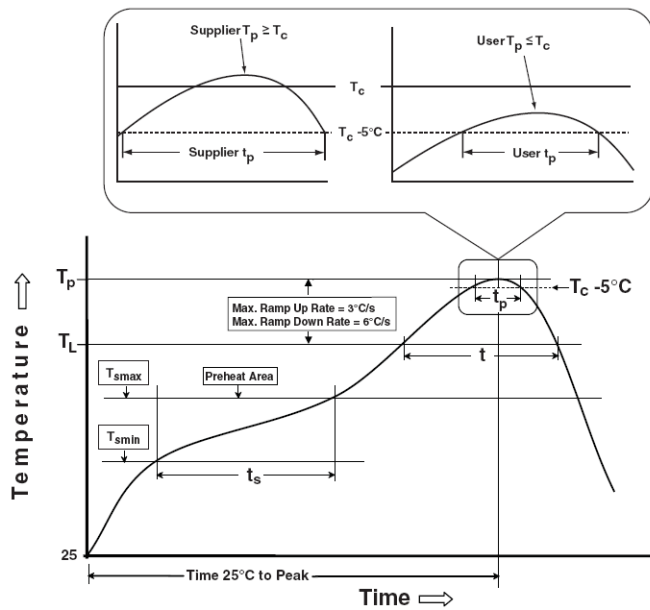
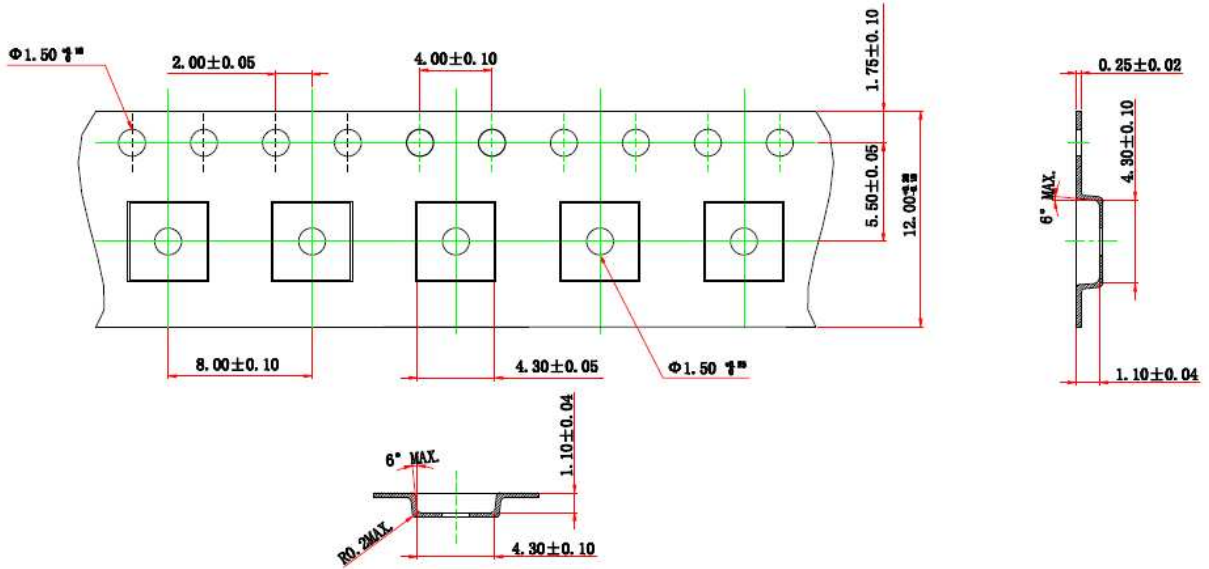


Figure 23 Classification Profile

Tape and Reel Information

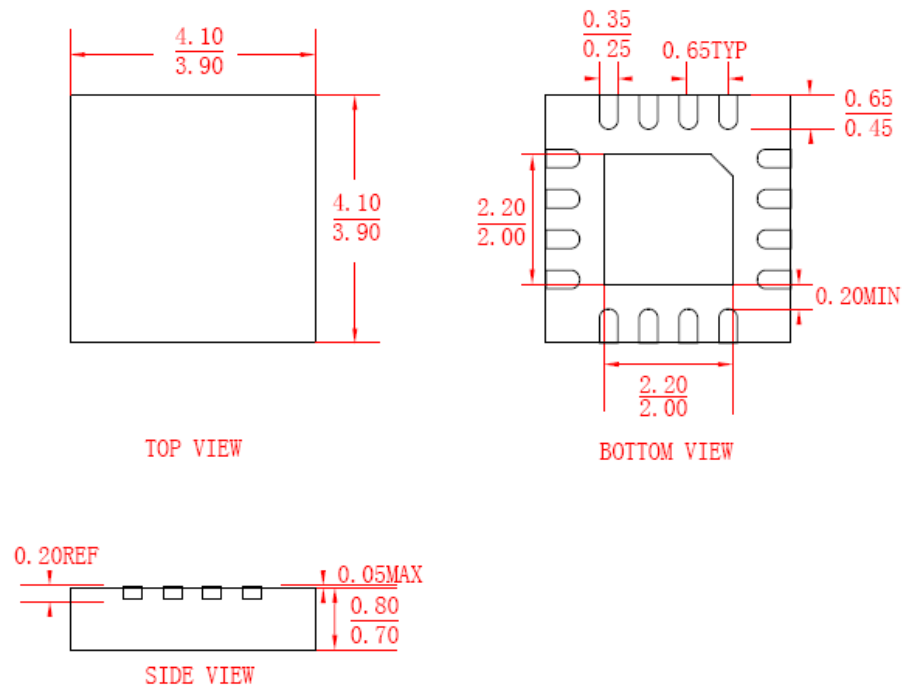


NOTES:[技术要求]:

- 1.CARRIER TAPE COLOR:BLACK[载带颜色为黑色]
- 2.COVER TAPE WIDTH:9.50±0.10 [配套9.5±0.10宽盖带]
- 3.COVER TAPE COLOR:TRANSPARENT[盖带颜色无色透明]
4. ANTISTATIC COATED 10<sup>10</sup>~10<sup>11</sup> OHMS/SQ.[单位面积表面阻抗为10<sup>10</sup>Ω/□~10<sup>11</sup>Ω/□]
- 5.10 BPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.  
[10个传送位孔间距累积公差0.20MAX.]
- 6.SUPPLIER-3M[供应商3M]
- 7.MOLD# WBRP(4×4×0.75/0.85)[载带模治WBRP(4×4×0.75/0.85)]
- 8.ALL DIMS IN mm.[所有单位为mm]
- 9.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.  
[禁止使用长电科技规定的一级环境管理物质]
- 10.THE DIRECTION OF VIEW: . [视图方向:
- 11.SPECIAL FOR CUSTOMER SI-EN [矽基客户专用]

## Package Information

## QFN-16



*Note: All dimensions in millimeters unless otherwise stated.*

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