

3W@5.0V Mono Filter-less Class-D Audio Power Amplifier

General Description

The SN2010B is a high efficiency, 3W@5.0V mono filter-less class-D audio power amplifier. A low noise, filter-less PWM architecture eliminates the output filter, reduces external component count, system cost, and simplifying design.

Operating in a single 5.0V supply, SN2010B is capable of driving 4Ω speaker load at a continuous average output of 3W@10% THD+N. The SN2010B has high efficiency with speaker load compared to a typical class-AB amplifier.

In cellular handsets, the earpiece, speaker phone, and melody ringer speaker can each be driven by the SN2010B. The gain of SN2010B is externally configurable which allows independent gain control from multiple sources by summing signals from each function. SN2010B is available in UTQFN-9 packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

Features

- 5.0V supply at THD+N = 10%
– 3W into 4Ω (Typ.)
– 1.68W into 8Ω (Typ.)
- Efficiency at 5.0V
– 85% at 400mW with a 4Ω speaker
– 88% at 400mW with a 8Ω speaker
- Less than 1μA shutdown current
- Optimized PWM output stage eliminates LC output filter
- Fully differential design reduces RF rectification and eliminates bypass capacitor
- Improved CMRR eliminates two input coupling capacitors
- Integrated click-and-pop suppression circuitry
- UTQFN-9 package
- RoHS compliant and 100% lead(Pb)-free

Applications

- Wireless or cellular handsets and PDAs
- Portable DVD player
- Notebook PC
- Portable radio
- Educational toys
- Portable gaming

Typical Application Circuit

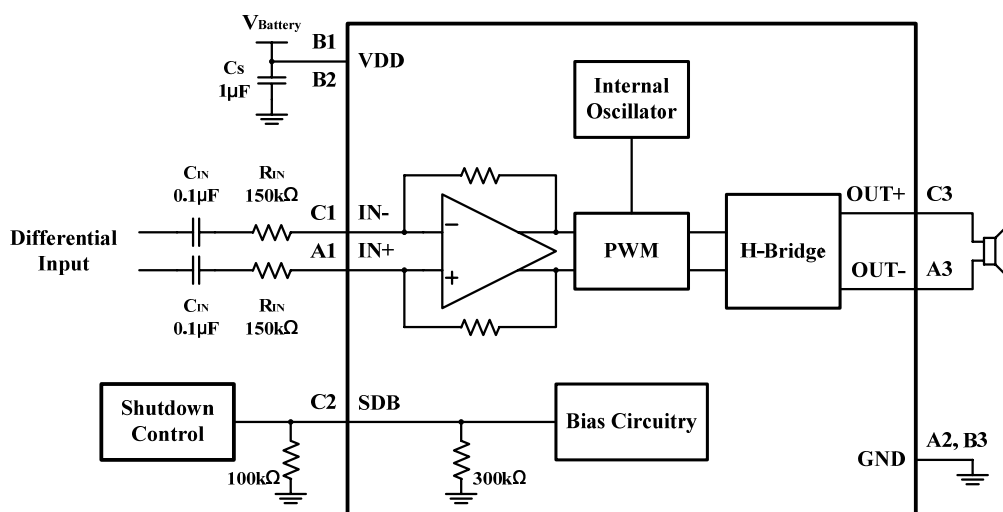


Figure 1 Typical Application Circuit

Pin Configuration

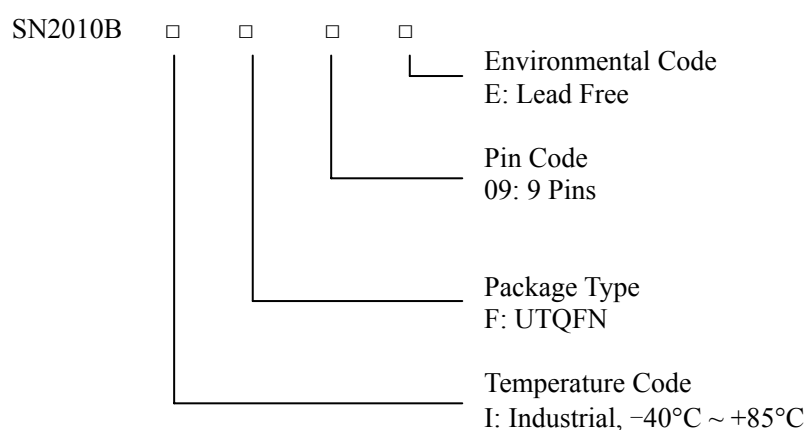
Package	Pin Configuration (Top View)
UTQFN-9	

Pin Description

No.	Pin	I/O	Description
A1	IN+	I	Positive audio input.
A2, B3	GND	-	Connect to ground.
A3	OUT-	O	Negative audio output.
B1, B2	VDD	-	Power supply.
C1	IN-	I	Negative audio input.
C2	SDB	I	Enter in shutdown mode when active low.
C3	OUT+	O	Positive audio output.

Ordering Information

Order Number	Package Type	QTY/Reel	Operating Temperature Range
SN2010BIF09E	UTQFN-9	3000	-40°C ~ +85°C



Absolute Maximum Ratings (Note 1)

Supply voltage, V_{DD} -----	-0.3V ~ +5.5V
Voltage at any input pin -----	-0.3V ~ $V_{DD} + 0.3V$
Junction temperature, T_{JMAX} -----	-40°C ~ +150°C
Storage temperature rang, T_{stg} -----	-65°C ~ +150°C
Lead temperature 1.6mm(1/16 inch) from case for 10s -----	260°C
Thermal resistance θ_{JA} (UTQFN) -----	70°C/W
ESD (HBM) -----	6kV

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

$V_{DD} = 2.7V \sim 5.5V$, $T_A = 25^\circ C$, unless otherwise noted. (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.7		5.5	V
$ V_{OS} $	Output offset voltage (measured differentially)	$V_{SDB} = 0V$, $A_V = 2V/V$		10		mV
I_{DD}	Quiescent current	$V_{DD} = 5.5V$, no load		2.6		mA
		$V_{DD} = 2.7V$, no load		1.2		
I_{SD}	Shutdown current	$V_{SDB} = 0.4V$			1	μA
f_{sw}	Switching frequency			250		kHz
R_{IN}	Input resistor	Gain $\leq 20V/V$	15			k Ω
Gain		$R_{IN} = 150k\Omega$		2		V/V
V_{IH}	High-level input voltage		1.4		V_{DD}	V
V_{IL}	Low-level input voltage		0		0.4	V

Electrical Characteristics

$T_A = 25^\circ\text{C}$, Gain = 2V/V, $C_{IN} = 2\mu\text{F}$, unless otherwise noted. (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
P_O	Output power	THD+N = 10% $f = 1\text{kHz}$, $R_L = 8\Omega$	$V_{DD} = 5.0\text{V}$		1.68		W
			$V_{DD} = 4.2\text{V}$		1.2		
			$V_{DD} = 3.6\text{V}$		0.88		
		THD+N = 10% $f = 1\text{kHz}$, $R_L = 4\Omega$	$V_{DD} = 5.0\text{V}$		3.0		W
			$V_{DD} = 4.2\text{V}$		2.0		
			$V_{DD} = 3.6\text{V}$		1.5		
		THD+N = 1% $f = 1\text{kHz}$, $R_L = 8\Omega$	$V_{DD} = 5.0\text{V}$		1.4		W
			$V_{DD} = 4.2\text{V}$		1.0		
			$V_{DD} = 3.6\text{V}$		0.7		
		THD+N = 1% $f = 1\text{kHz}$, $R_L = 4\Omega$	$V_{DD} = 5.0\text{V}$		2.4		W
			$V_{DD} = 4.2\text{V}$		1.68		
			$V_{DD} = 3.6\text{V}$		1.2		
THD+N	Total harmonic distortion plus noise	$V_{DD} = 4.2\text{V}$, $P_O = 0.6\text{W}$, $R_L = 8\Omega$, $f = 1\text{kHz}$		0.18		%	
		$V_{DD} = 4.2\text{V}$, $P_O = 1.1\text{W}$, $R_L = 4\Omega$, $f = 1\text{kHz}$		0.22			
V_{NO}	Output voltage noise	$V_{DD} = 4.2\text{V}$, $f = 20\text{Hz}$ to 20kHz Inputs AC-grounded		80		μV_{rms}	
T_{WU}	Wake-up time from shutdown	$V_{DD} = 3.6\text{V}$		32		ms	
SNR	Signal-to-noise ratio	$P_O = 1.0\text{W}$, $R_L = 8\Omega$, $V_{DD} = 4.2\text{V}$		91		dB	
PSRR	Power supply rejection ratio	$f = 217\text{Hz}$, $R_L = 8\Omega$ Input grounded	$V_{DD} = 5.0\text{V}$		-75	dB	
			$V_{DD} = 4.2\text{V}$		-70		
			$V_{DD} = 3.6\text{V}$		-66		

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: All parts are production tested at $T_A = 25^\circ\text{C}$. Other temperature limits are guaranteed by design.

Note 3: Guaranteed by design.

Typical Performance Characteristic

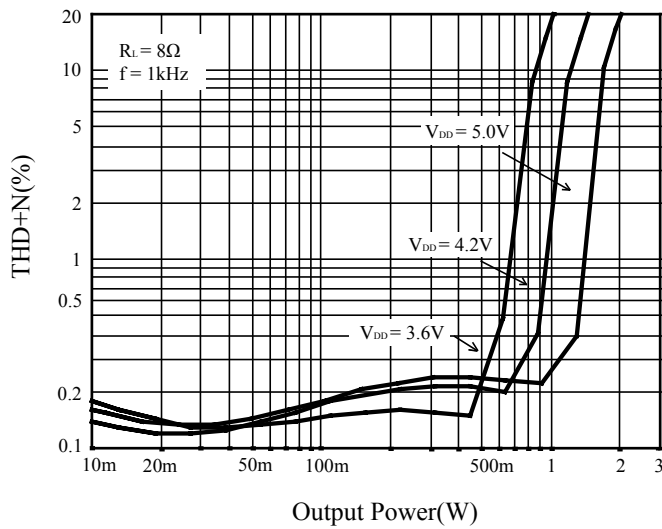


Figure 2 THD+N vs. Output Power

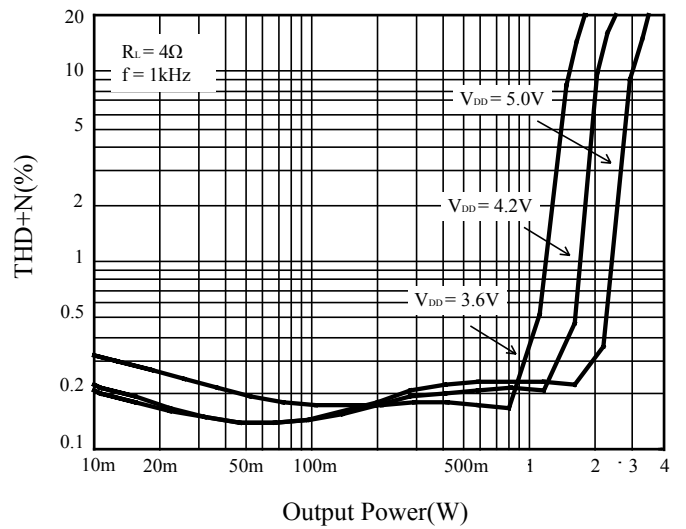


Figure 3 THD+N vs. Output Power

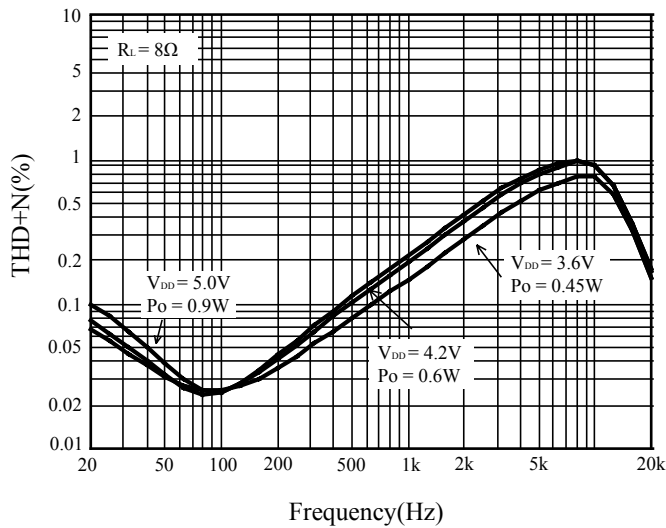


Figure 4 THD+N vs. Frequency

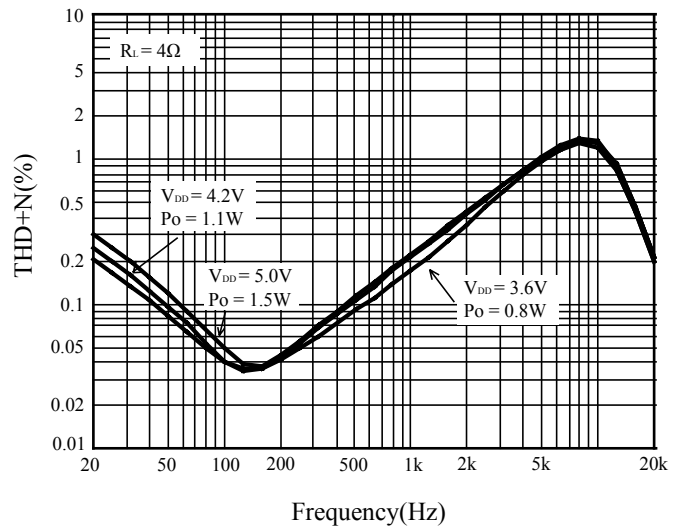


Figure 5 THD+N vs. Frequency

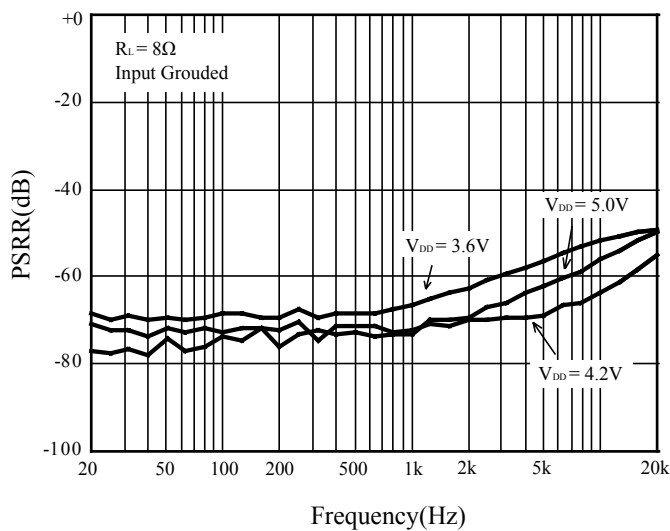


Figure 6 PSRR vs. Frequency

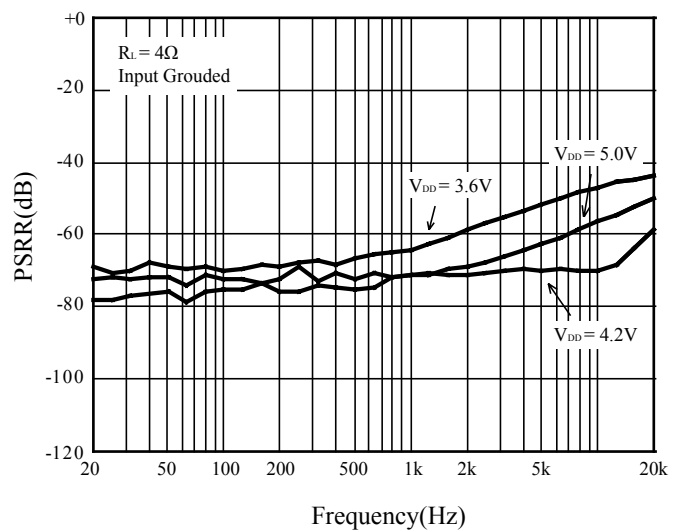


Figure 7 PSRR vs. Frequency

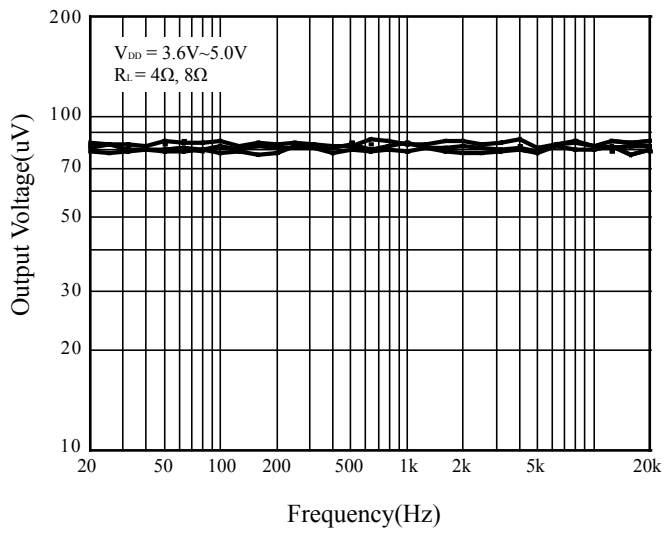


Figure 8 Noise

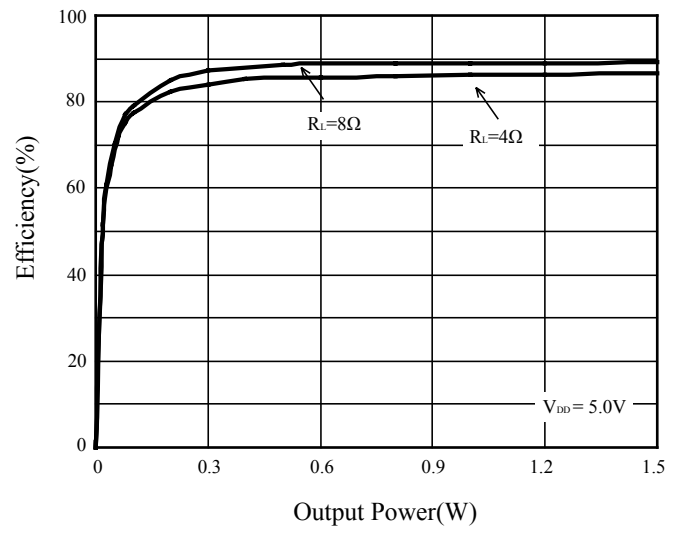


Figure 9 Efficiency

Application Information

Fully Differential Amplifier

The SN2010B is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential SN2010B can still be used with a single-ended input; however, the SN2010B should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output.

GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

Component Selection

Figure 10 shows the SN2010B with differential inputs and input capacitors, and Figure 11 shows the SN2010B with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

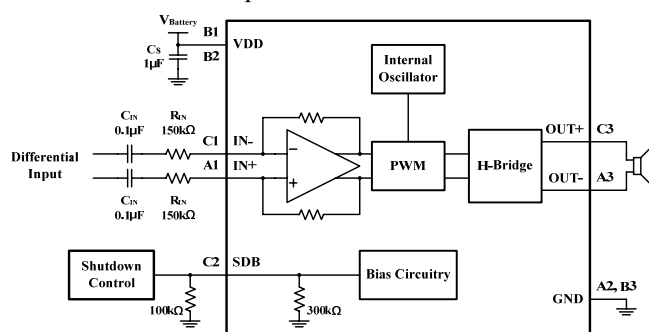


Figure 10 Differential Input

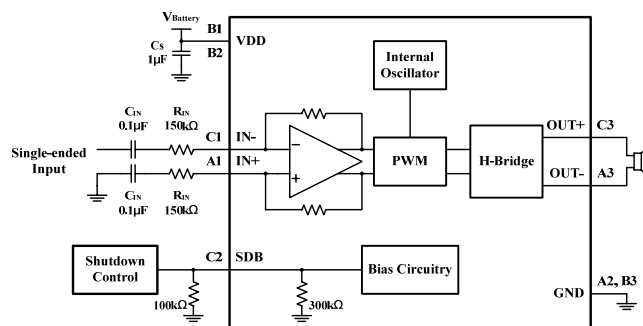


Figure 11 Single-Ended Input

Input Resistors (R_{IN})

The input resistors (R_{IN}) set the gain of the amplifier according to Equation (1).

$$Gain = \frac{2 \times 150k\Omega}{R_{IN}} \left(\frac{V}{V} \right) \quad (1)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the SN2010B to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2V/V or lower. Lower gain allows the SN2010B to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Decoupling Capacitor (C_S)

The SN2010B is a high performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the SN2010B is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications

because of the high PSRR of this device

Input Capacitors (C_{IN})

The input capacitors and input resistors form a high pass filter with the corner frequency, f_c , determined in Equation (2).

$$f_c = \frac{1}{(2\pi R_{IN} C_{IN})} \quad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_{IN} = \frac{1}{(2\pi R_{IN} f_c)} \quad (3)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of $\pm 10\%$ or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low frequency response, use large input coupling capacitors ($1\mu F$). However, in a GSM phone the ground signal is fluctuating at 217Hz, but the signal from the codec does not have the same 217Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217Hz hum.

Summing Input Signals

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The SN2010B makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see Equations (4) and (5) and Figure 12).

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{IN1}} \left(\frac{V}{V} \right) \quad (4)$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{IN2}} \left(\frac{V}{V} \right) \quad (5)$$

If summing left and right inputs with a gain of 1V/V, use $R_{IN1} = R_{IN2} = 300k\Omega$.

If summing a ring tone and a phone signal, set the ring-tone gain to $Gain2 = 2V/V$, and the phone gain to $Gain1 = 0.1V/V$. The resistor values would be

$$R_{IN1} = 3M\Omega, R_{IN2} = 150k\Omega$$

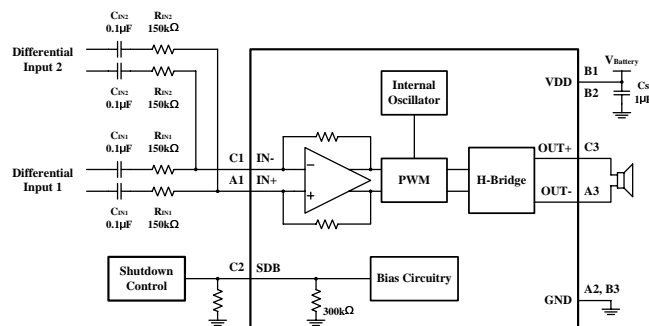


Figure 12 Summing Two Differential Inputs

Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 13 shows how to sum a differential input signal and a single-ended input signal. Ground noise may couple in through IN- with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{IN2} , shown in Equation (8). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{IN1}} \left(\frac{V}{V} \right) \quad (6)$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{IN2}} \left(\frac{V}{V} \right) \quad (7)$$

$$C_{IN2} = \frac{1}{(2\pi R_{IN2} f_{c2})} \quad (8)$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at $Gain1 = 0.1V/V$, and the ring-tone gain is set to $Gain2 = 2V/V$, the resistor values would be

$$R_{IN1} = 3M\Omega, R_{IN2} = 150k\Omega$$

The high pass corner frequency of the single-ended input is set by C_{IN2} . If the desired corner frequency is less than 20Hz.

$$C_{IN2} > \frac{1}{(2\pi 150k\Omega \times 20Hz)} \quad (9)$$

$$C_{IN2} > 53pF \quad (10)$$

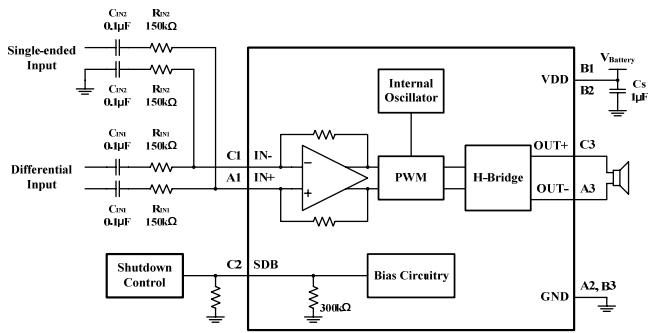


Figure 13 Summing Differential Input and Single-Ended Input Signals

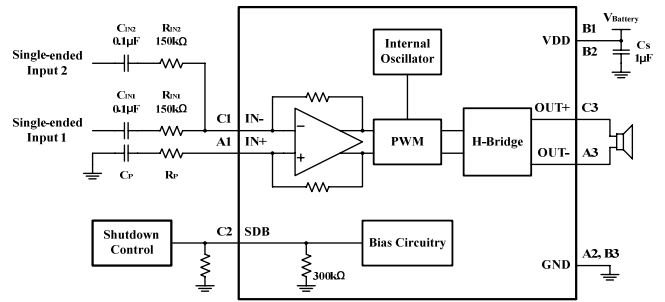


Figure 14 Summing Two Single-Ended Inputs

Summing Two Single-Ended Input Signals

The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see Equations (11) through (14) and Figure 14). Resistor, R_P , and capacitor, C_P , are needed on the IN^- terminal to match the impedance on the IN^+ terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{IN1}} \left(\frac{V}{V} \right) \quad (11)$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{IN2}} \left(\frac{V}{V} \right) \quad (12)$$

$$C_{IN1} = \frac{1}{(2\pi R_{IN1} f_{c1})} \quad (13)$$

$$C_{IN2} = \frac{1}{(2\pi R_{IN2} f_{c2})} \quad (14)$$

$$C_P = C_{IN1} + C_{IN2} \quad (15)$$

$$R_P = \frac{R_{IN1} \times R_{IN2}}{(R_{IN1} + R_{IN2})} \quad (16)$$

EMI Evaluation Result

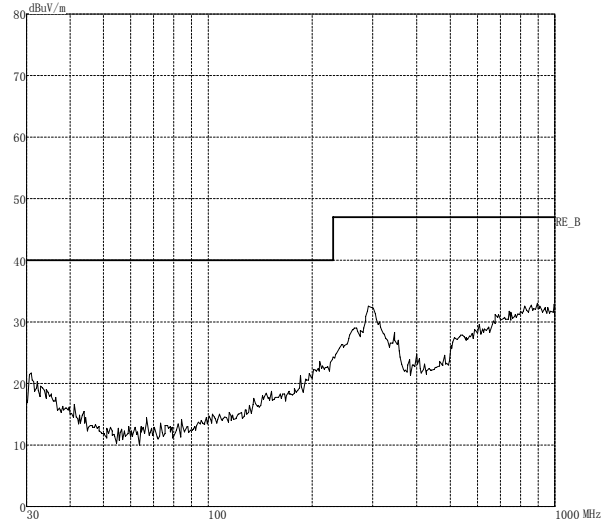


Figure 15 EMI Evaluation Result

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

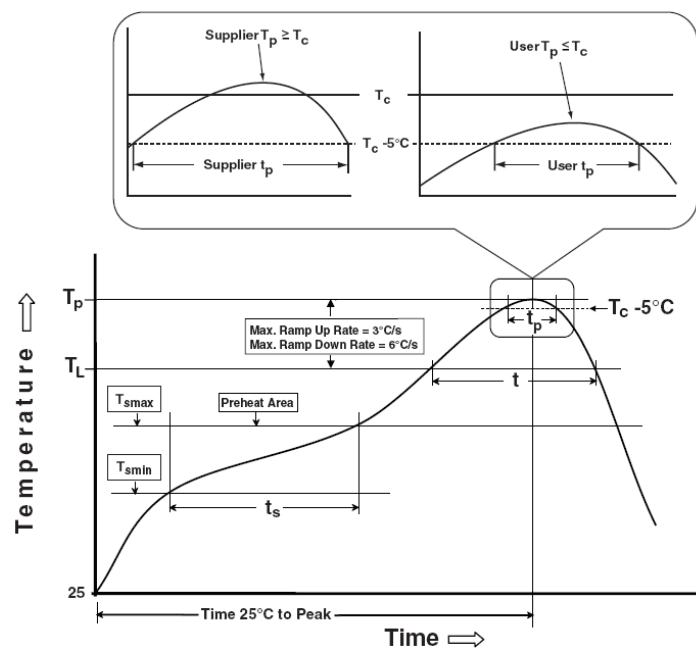
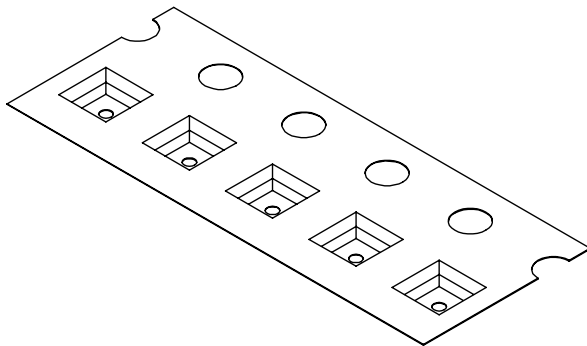
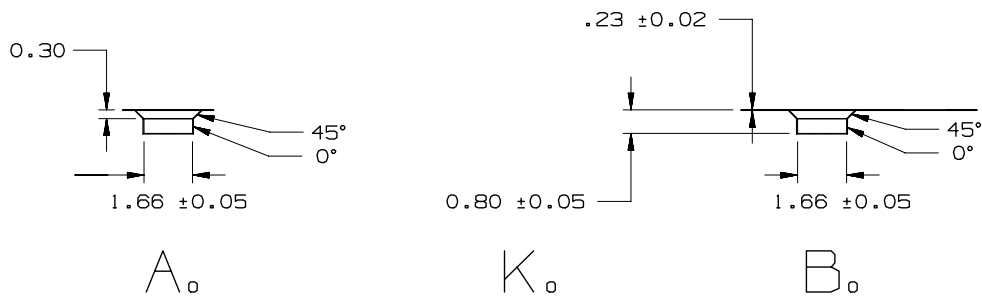
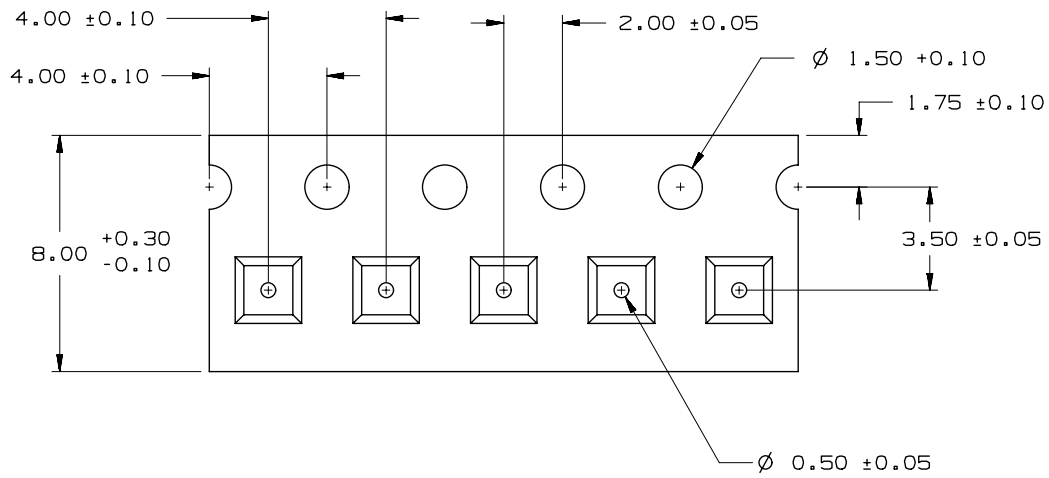


Figure 16 Classification Profile

Tape and Reel Information

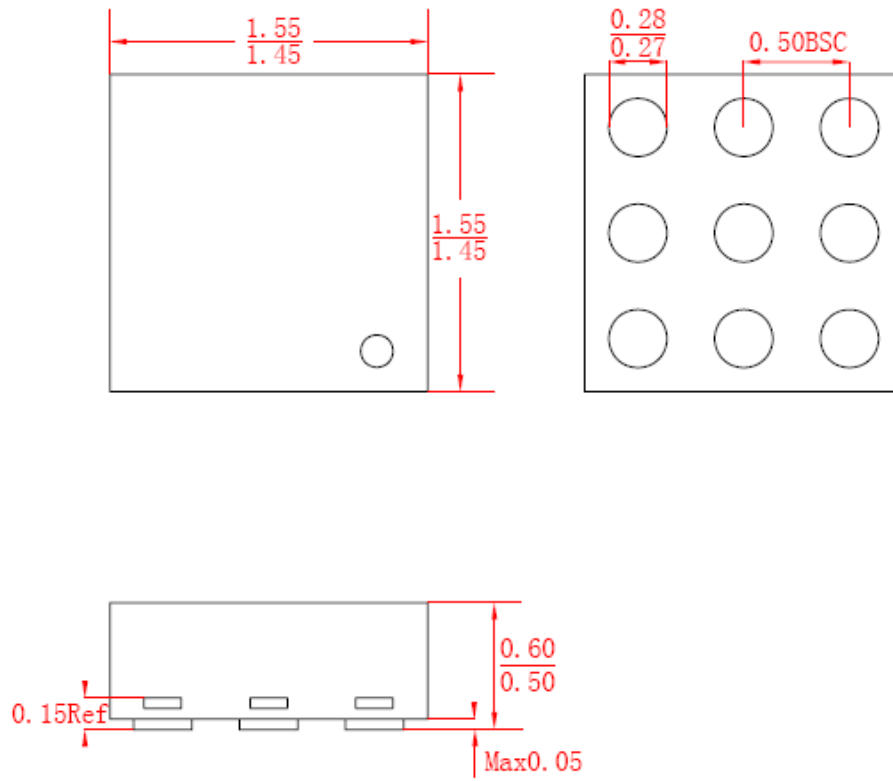


THE DIMENSIONS SHOWN ON THIS PROPOSED DRAWING ARE FOR ILLUSTRATIVE PURPOSE. DIMENSIONS FROM ACTUAL CARRIER MAY VARY SLIGHTLY.

Note: All dimensions in millimeters unless otherwise stated.

Packaging Information

UTQFN-9



Note: All dimensions in millimeters unless otherwise stated.

SI-EN 专利 UTQFN 封装 1.5mm × 1.5mm_9L SMT 贴片指导说明 Rev 4.0

超薄四方扁平及管脚微缩结构（UTQFN, Ultra Thickness Quad Flat Non-leded）封装的 Audio PA 是矽恩微电子（SI-EN Technology Ltd）推出的可完全替代市场上所有玻璃封装（WLCSP, Wafer Level Chip Scale Package），并具有专利保护的（专利号：200920137165.8）的新产品。

为了让您更深入地了解并顺利导入此产品，主要从以下 2 个方面提供此产品的使用说明：

一、产品介绍

对比 UTQFN 和 WLCSP，UTQFN 有明显的优势如下：

1. 成本更有优势

由于采用了更先进的工艺和制程，降低了芯片的面积成本，从而使得整体产品成本更有优势。

2. 交货周期更短

一般的生产周期为 4 天，与一般 QFN 产品的工艺流程基本相同，UTQFN 交货更有保障，可迅速适应大规模突发交货需求。

3. 品质更稳定

由于芯片不直接裸露在外面，所以避免了传统 WCSP 封装产品贴片使用的过程中容易崩缺、掉球等不良现象。

二、SMT 生产使用注意点

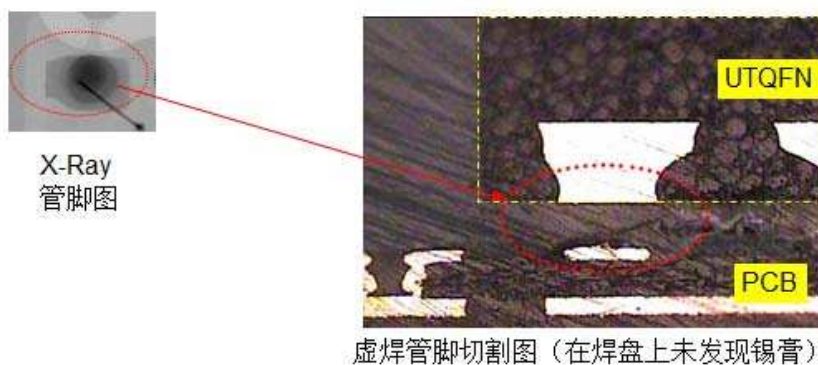
由于 UTQFN 的管脚结构与 QFN 类似为平面（2D）结构，与 WLCSP 的管脚的三维球（3D）结构不同，这使得贴片前需要：

1. 调整贴片机的 UTQFN 影像辨识设定

UTQFN	WLCSP
侧光为辅 垂直光为主	侧光为主 垂直光为辅

2. 注意生产过程中锡膏印刷质量的管控

WLCSP 的管脚是可塌落的焊锡球，在 reflow 过程中可以补充锡膏印刷过程中锡膏不足的问题，所以目前生产过程中一些锡膏印刷质量不好的问题并没有曝露出来，而 UTQFN 是 2D 的平面结构，会受到锡膏不足问题的影响，而表现为虚焊，如下图，某客户曾经反映 0.1% 的初期量产虚焊问题，经过确认，为焊盘上没有锡膏所至，该客户通过过加强贴片厂的印刷流程品质管控后，问题得以解决。



虚焊管脚的切割图



所以在 SMT 生产中应特别注意:

- (1) 印刷后的品质抽检, 注意锡膏不足和印刷偏移问题。
- (2) 钢网的清理频率。
- (3) 锡膏的使用寿命, 不可以超时使用 (锡膏的粘稠度会显著增高)。

矽恩微电子品保工程部
2011 年 1 月

如果您对 SMT 生产有技术疑问, 请发邮件到 qa@si-en.com, 或者请致电: 13625277602 曹先生

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