

## 2.7W Mono Filter-less Class-D Audio Power Amplifier

### General Description

The SN2005 is a high efficiency, 2.7W mono class-D audio power amplifier. A low noise, filter-less PWM architecture eliminates the output filter, reducing external component count, system cost, and simplifying design.

Operating in a single 5V supply, SN2005 is capable of driving 4Ω speaker load at a continuous average output of 2.7W with 10% THD+N. The SN2005 has high efficiency with speaker load compared to a typical class AB amplifier.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the SN2005. The gain of SN2005 is externally configurable which allows independent gain control from multiple sources by summing signals from each function.

The SN2005 is available in DFN and MSOP packages.

### Applications

- Wireless or Cellular Handsets and PDAs
- Portable DVD Player
- Notebook PC
- Portable Radio
- Educational Toys
- USB Speakers
- Portable Gaming

### Features

- 5 V Supply at THD = 10%
  - ◇ 2.7 W Into 4Ω (Typ)
  - ◇ 1.6 W Into 8Ω (Typ)
- Efficiency at 5V:
  - ◇ 83% at 400 mW with a 4Ω speaker
  - ◇ 89% at 400 mW with a 8Ω speaker
- Low Quiescent Current (3mA) and less than 0.1μA Shutdown Current from a 5.5V supply
- Improved PSRR (-63 dB) and 2.5V to 5.5V Wide Supply Voltage Eliminates Need for a Voltage Regulator
- Optimized PWM Output Stage Eliminates LC Output Filter
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Integrated Pop and Click Suppression Circuitry
- 3mm × 3mm DFN-8 and MSOP-8package
- RoHS compliant and 100% lead(Pb)-free

### Typical Application Circuit

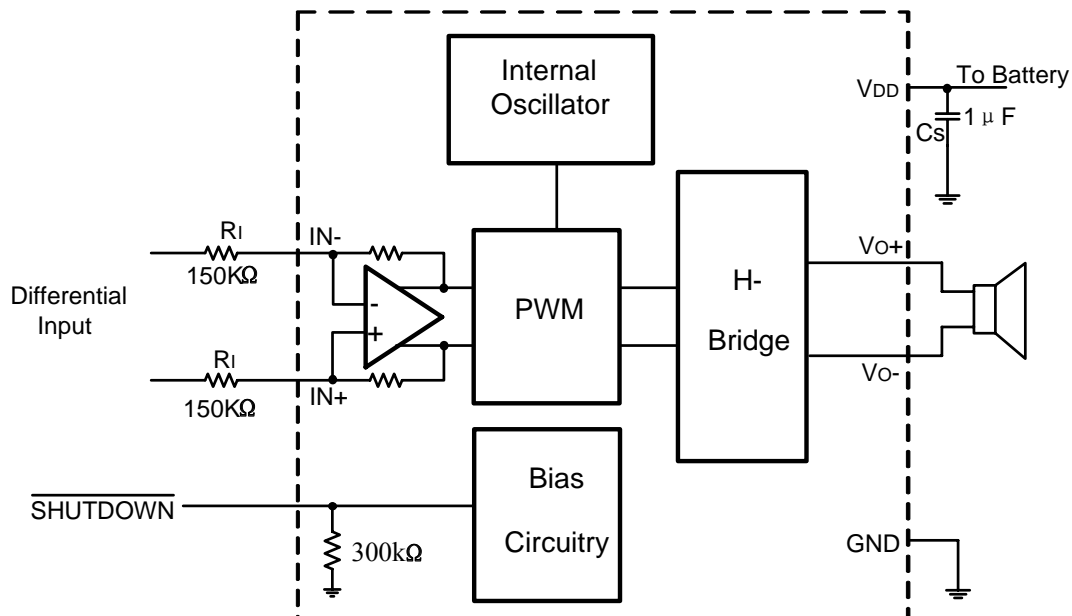


Figure 1 Typical SN2005 Application Schematic with Differential Input without Input Capacitors

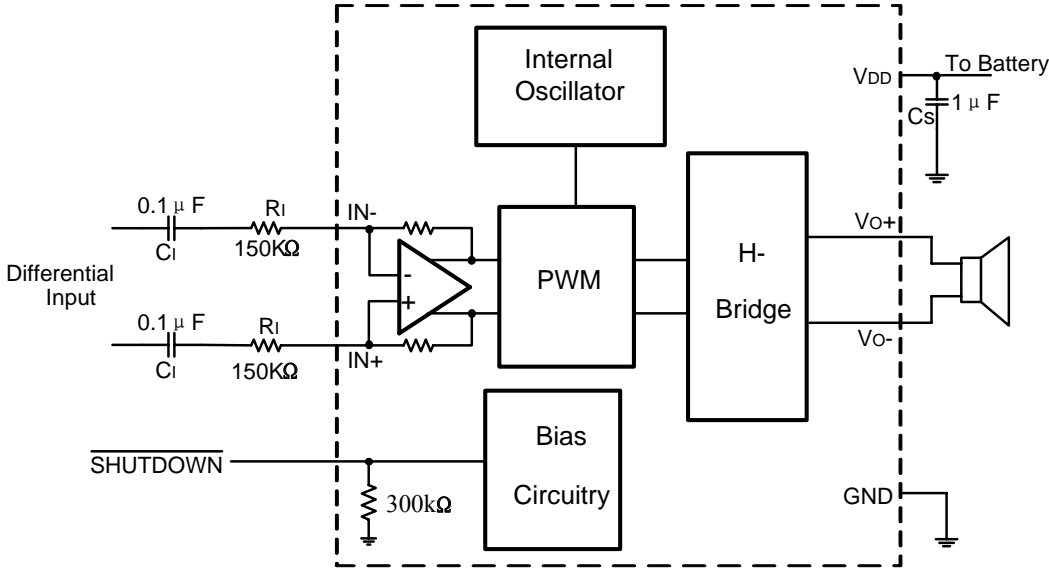


Figure 2 Typical SN2005 Application Schematic with Differential Input and Input Capacitors

Pin Configurations

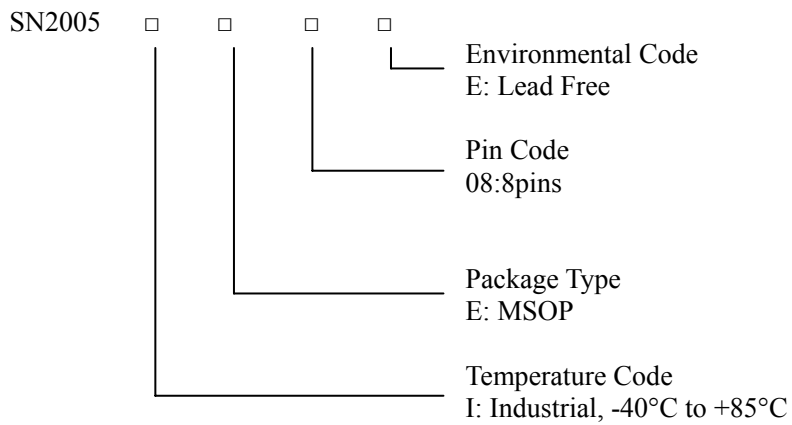
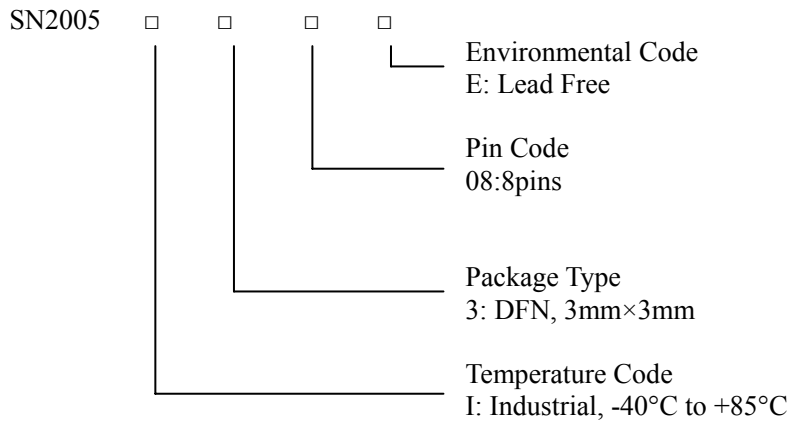
Package	Pin Configurations (Top view)
DFN-8	
MSOP-8	

Pin Description

Pin	DFN-8	MSOP-8	I/O	Description
SHUTDOWN	1	1	I	Shutdown terminal (active low logic)
NC	2	2		No internal connection
IN+	3	3	I	Positive differential input
IN-	4	4	I	Negative differential input
Vo+	5	5	O	Positive BTL output
VDD	6	6	I	Power supply
GND	7	7	I	High-current ground
Vo-	8	8	O	Negative BTL output
Thermal Pad	Yes	No		Connect to GND

## Ordering Information

Order Number	Package Type	Operating Temperature range
SN2005I308E	DFN-8	-40 °C to 85°C
SN2005IE08E	MSOP-8	-40 °C to 85°C



**Absolute Maximum Ratings (Note 1)**

- Supply Voltage,  $V_{DD}$ .....-0.3 V to 6V
- Voltage at Any Input Pin.....-0.3 V to  $V_{DD} + 0.3V$
- Junction Temperature,  $T_{JMAX}$ .....-40°C to 150°C
- Storage Temperature Rang,  $T_{stg}$ ...-65°C to 150°C
- ESD Susceptibility.....4kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds.....260°C
- Thermal Resistance  $\theta_{JA}$  (DFN) .....47°C/W

**Recommended Operating Conditions**

Parameter		Min.	Max.	Unit
Supply voltage, $V_{DD}$		2.5	5.5	V
High-level input voltage, $V_{IH}$	$\overline{SHUTDOWN}$	1.4	$V_{DD}$	V
Low-level input voltage, $V_{IL}$	$\overline{SHUTDOWN}$	0	0.4	V
Input resistor, $R_I$	Gain $\leq 20V/V$ (26dB)	15		k $\Omega$
Common mode input voltage range, $V_{IC}$	$V_{DD} = 2.5 V, 5.5 V$	0.5	$V_{DD}-0.8$	V
Operating free-air temperature, $T_A$		-40	85	°C

**Electrical Characteristics  $T_A = 25^\circ C$  (Note 2)**

Symbol	Parameter	Conditions	SN2005			Unit
			Min.	Typ.	Max.	
$ V_{OS} $	Output offset voltage (measured differentially)	$V_I = 0V, A_V = 2 V/V, V_{DD} = 2.5V \text{ to } 5.5V$		1	25	mV
$ I_{IH} $	High-level input current	$V_{DD} = 5.5V, V_I = 5.8V$			35	$\mu A$
$ I_{IL} $	Low-level input current	$V_{DD} = 5.5V, V_I = -0.3V$			2	$\mu A$
$I_Q$	Quiescent current	$V_{DD} = 5.5V, \text{ no load}$		3	4.5	mA
		$V_{DD} = 2.5V, \text{ no load}$		2	3.2	
$I_{SD}$	Shutdown current	$V_{\overline{SHUTDOWN}} = 0.4V, V_{DD} = 2.5V \text{ to } 5.5V$		0.1	1	$\mu A$
fsw	Switching frequency	$V_{DD} = 2.5V \text{ to } 5.5V$		300		kHz
Gain		$V_{DD} = 2.5V \text{ to } 5.5V, R_I = 150K\Omega$		2		

Electrical Characteristics  $T_A = 25^\circ\text{C}$ , Gain= 2V/V, (Note 3)

Symbol	Parameter	Conditions		SN2005			Unit
				Min.	Typ.	Max.	
$P_O$	Output power	THD+N=10%, f=1kHz, $R_L=8\Omega$	$V_{DD}= 5.0\text{V}$		1.61		W
			$V_{DD}= 3.6\text{V}$		0.85		
			$V_{DD}= 2.5\text{V}$		0.40		
		THD+N=10%, f=1kHz, $R_L=4\Omega$	$V_{DD}= 5.0\text{V}$		2.69		W
			$V_{DD}= 3.6\text{V}$		1.45		
			$V_{DD}= 2.5\text{V}$		0.61		
		THD+N=1%, f=1kHz, $R_L=8\Omega$	$V_{DD}= 5.0\text{V}$		1.34		W
			$V_{DD}= 3.6\text{V}$		0.71		
			$V_{DD}= 2.5\text{V}$		0.32		
		THD+N=1%, f=1kHz, $R_L=4\Omega$	$V_{DD}= 5.0\text{V}$		1.94		W
			$V_{DD}= 3.6\text{V}$		1.15		
			$V_{DD}= 2.5\text{V}$		0.50		
THD+N	Total harmonic distortion plus noise	$V_{DD}= 5.0\text{V}, P_O=1.0\text{W}, R_L=8\Omega, f=1\text{kHz}$			0.17		%
		$V_{DD}= 5.0\text{V}, P_O=1.2\text{W}, R_L=4\Omega, f=1\text{kHz}$			0.20		
$V_N$	Output voltage noise	$V_{DD}= 5\text{V}, f=20\text{Hz to } 20\text{kHz}$ , Inputs ac-grounded with $C_I= 1\mu\text{F}$ A-Weighting			54		$\mu\text{Vrms}$
$T_{WU}$	Wake-up time from shutdown	$V_{DD}= 3.6\text{V}$			3.5		ms
SNR	Signal-to-noise ratio	$P_O=1.0\text{W}, R_L=8\Omega, V_{DD}= 5.0\text{V}$			94		dB
PSRR	Power supply rejection ratio	$V_{DD}= 2.5\text{V to } 5.5\text{V}$			-63		dB

**Note1:** Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Note 2:** All parts are production tested at  $T_A = 25^\circ\text{C}$ . Other temperature limits are guaranteed by design

**Note3.** Guaranteed by design

Typical Performance Characteristics

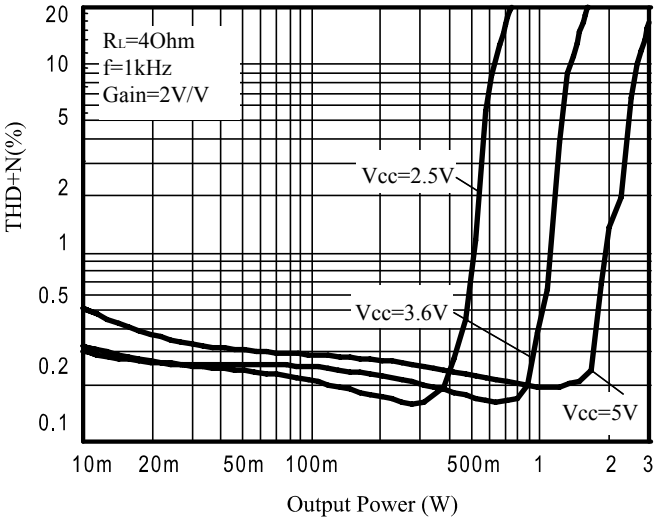


Figure 3. THD+N vs. Output Power

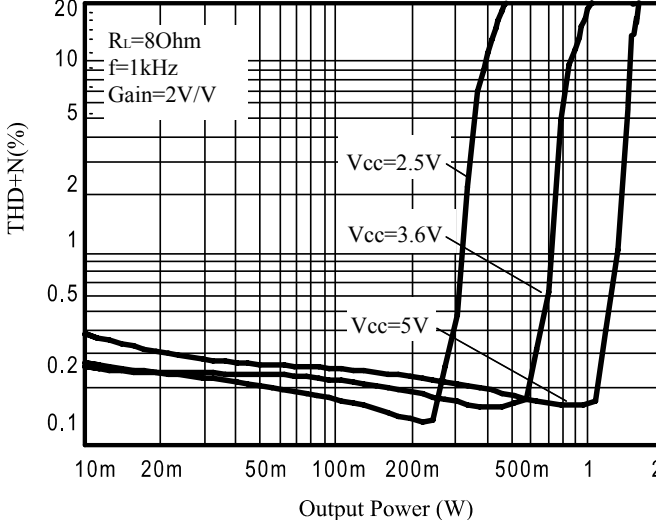


Figure 4. THD+N vs. Output Power

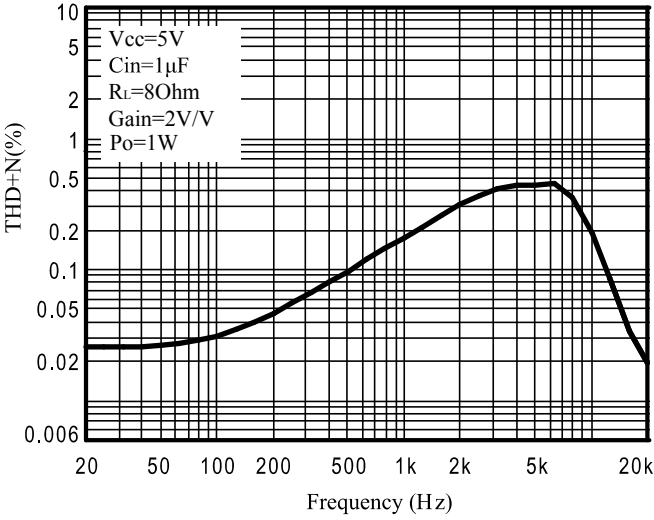


Figure 5. THD+N vs. Frequency

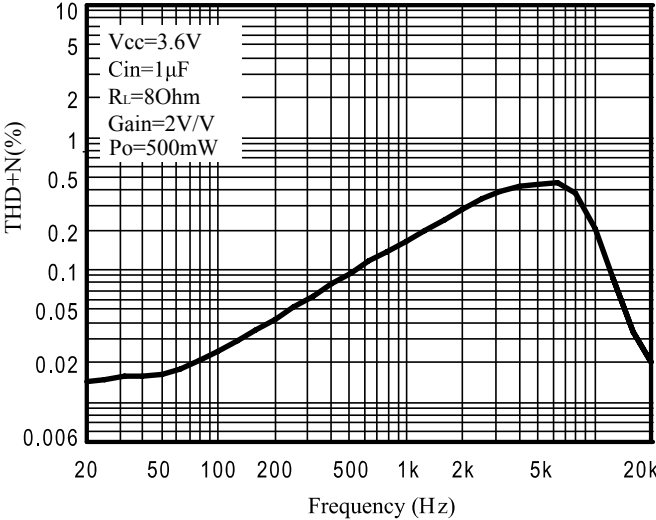


Figure 6. THD+N vs. Frequency

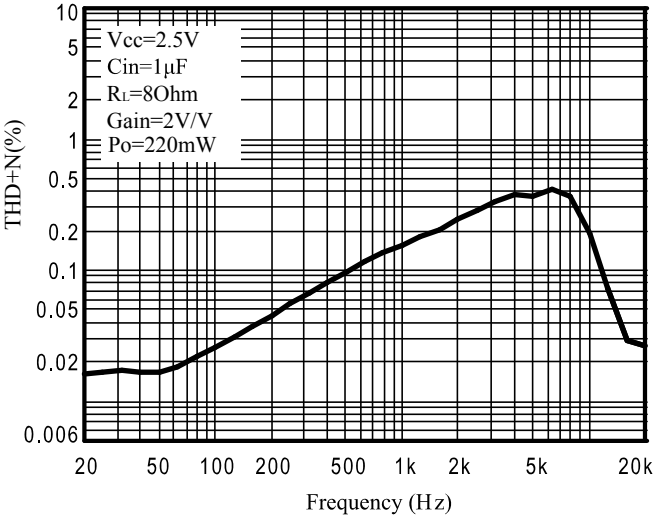


Figure 7. THD+N vs. Frequency

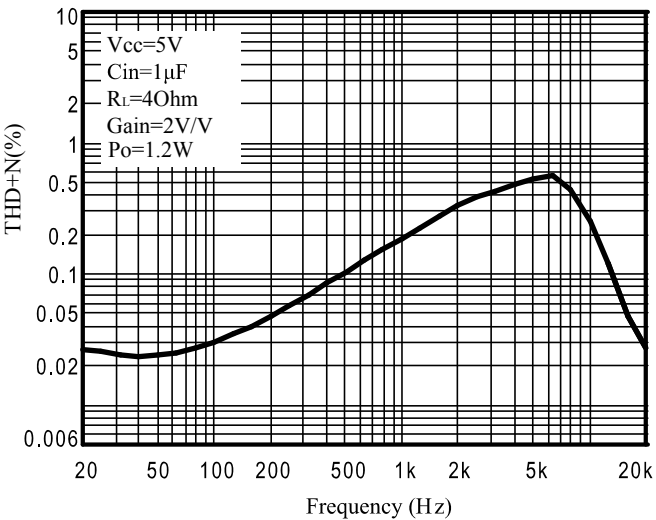


Figure 8. THD+N vs. Frequency

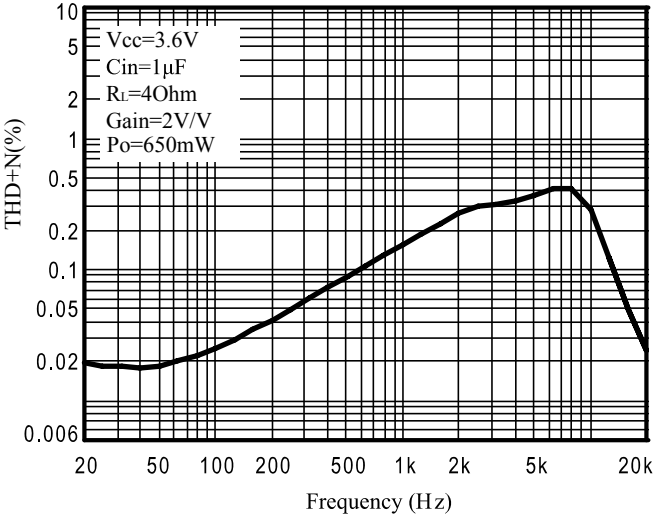


Figure 9. THD+N vs. Frequency

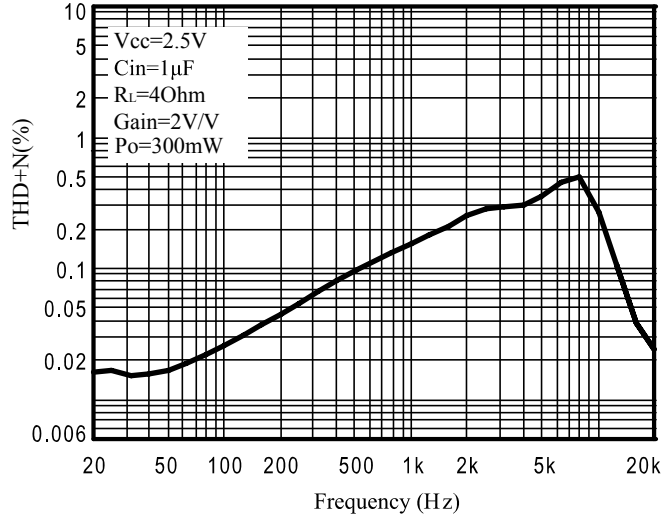


Figure 10. THD+N vs. Frequency

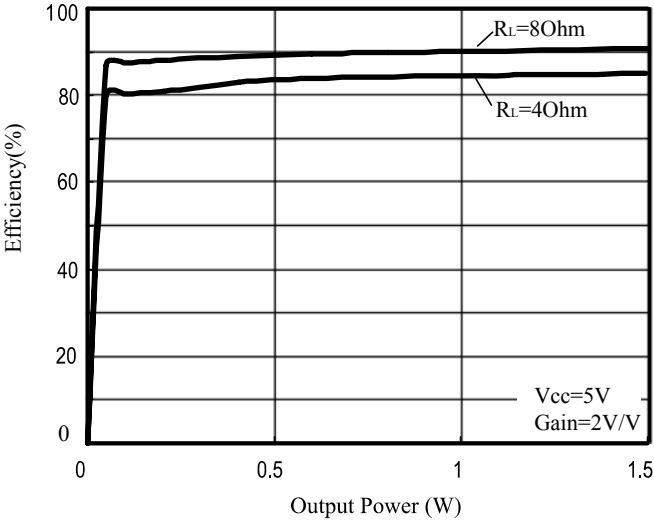


Figure 11. Efficiency vs. Output Power

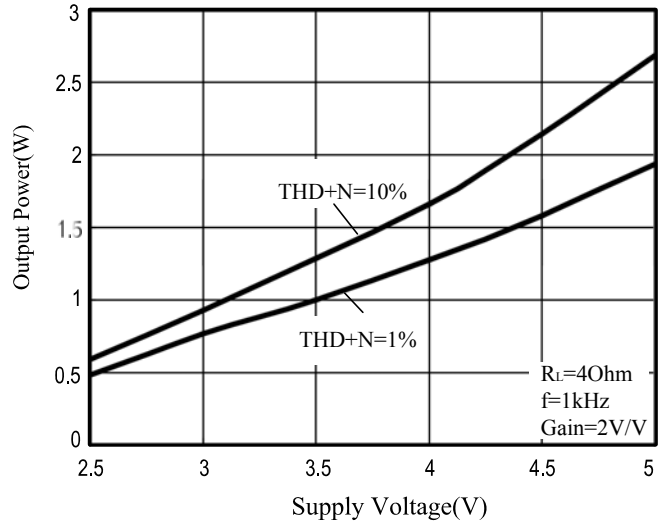


Figure 12. Output Power vs. Supply Voltage

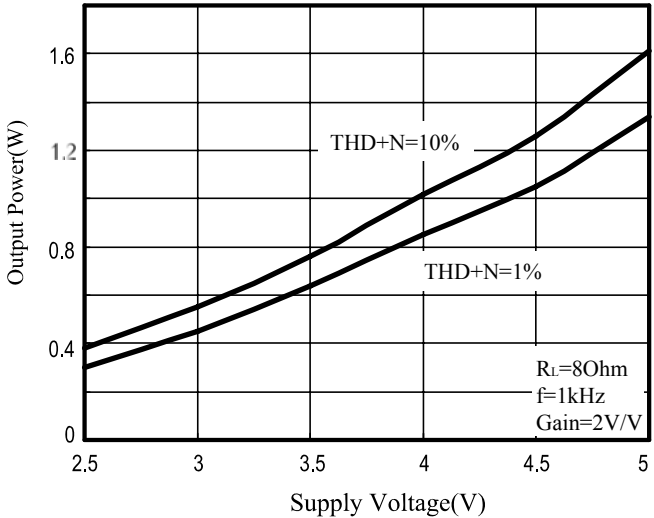


Figure 13. Output Power vs. Supply Voltage

## Application Information

### Fully Differential Amplifier

The SN2005 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around  $V_{DD}/2$  regardless of the common-mode voltage at the input. The fully differential SN2005 can still be used with a single-ended input; however, the SN2005 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

### Advantages of Fully Differential Amplifiers

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.

GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

### Component Selection

Figure 14 shows the SN2005 with differential inputs and optional input capacitors. Input capacitors are used when the common mode input voltage range specs can not be guaranteed or high pass filter is considered.

Figure 15 shows the SN2005 with single-ended inputs. The input capacitors have to be used in the single ended case because it is much more susceptible to noise in this case.

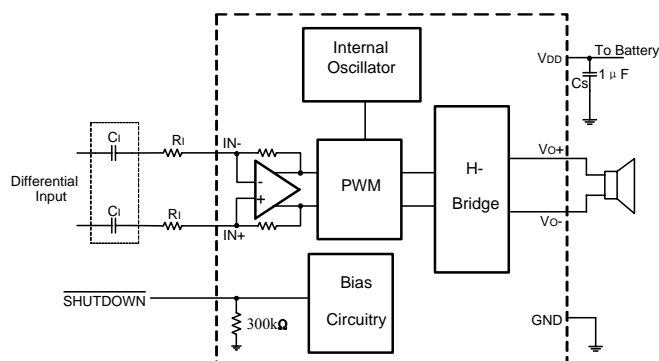


Figure 14. Typical Application Schematic with Differential Input

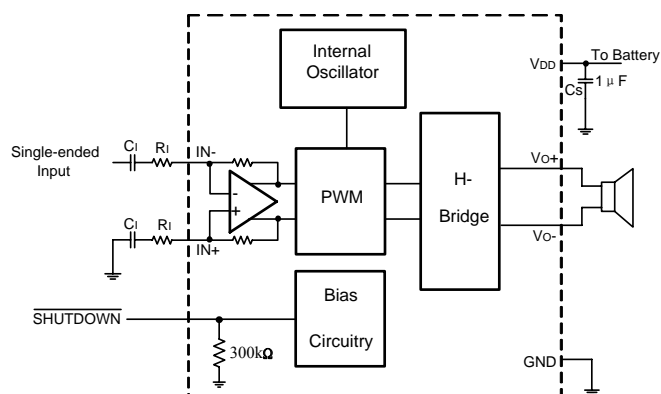


Figure 15. Typical Application Schematic with Single-Ended Input

### Input Resistors ( $R_I$ )

The input resistors ( $R_I$ ) set the gain of the amplifier according to equation (1).

$$\text{Gain} = \frac{2 \times 150\text{k}\Omega}{R_I} \left( \frac{V}{V} \right) \quad (1)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% accuracy resistors or better to keep the performance optimized. Matching is more important than overall accuracy.

Place the input resistors close to the SN2005 to reduce noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the SN2005 to operate at its best, and keeps a high V voltage at the input making the inputs less susceptible to noise.

### Decoupling Capacitor ( $C_S$ )

The SN2005 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure high efficiency and low total harmonic distortion (THD). For higher frequency transients, spikes, or digital noises on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically  $1\mu\text{F}$ , placed as close as possible to the device  $V_{DD}$  pin works best. Placing this decoupling capacitor close to the SN2005 is also important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a  $10\mu\text{F}$  or greater capacitor placed near the audio power amplifier would also be helpful, but it is not required in most applications because of better PSRR of this device.

### Input Capacitors (C<sub>I</sub>)

The input capacitors and input resistors form a high-pass filter with the corner frequency,  $f_c$ , determined in equation (2).

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad (3)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of  $\pm 10\%$  or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1 $\mu$ F). However, in a GSM phone the ground signal is fluctuating at 217Hz, but the signal from the codec does not have the same 217Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217Hz hum.

### Summing Input Signals

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The SN2005 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

### Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals. The gain for each input source can be set independently (see equations (4) and (5), and Figure 16).

$$Gain1 = \frac{V_o}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left( \frac{V}{V} \right) \quad (4)$$

$$Gain2 = \frac{V_o}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left( \frac{V}{V} \right) \quad (5)$$

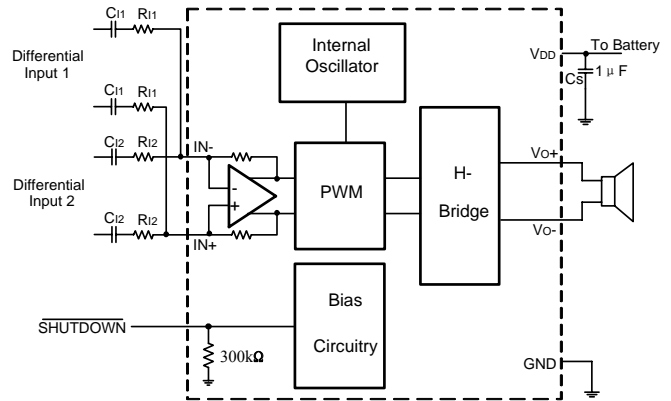


Figure 16 Application Schematic with SN2005 Summing Two Differential Inputs

If summing left and right inputs with a gain of 1V/V, use  $R_{I1} = R_{I2} = 300k\Omega$ .

If summing a ring tone and a phone signal, set the ring-tone gain to  $Gain\ 2 = 2V/V$ , and the phone gain to  $Gain\ 1 = 0.1\ V/V$ . The resistor values would be.

$R_{I1} = 3M\Omega$ , and  $R_{I2} = 150k\Omega$

### Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 17 shows how to sum a differential input signal and a single-ended input signal. Ground noise may couple in through IN- with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by  $C_{I2}$ , shown in equation (8). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$Gain1 = \frac{V_o}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left( \frac{V}{V} \right) \quad (6)$$

$$Gain2 = \frac{V_o}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left( \frac{V}{V} \right) \quad (7)$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \quad (8)$$

If summing a ring tone and phone signals, the phone signals should use the differential inputs while the ring tone should use the single-ended input. The phone gain is set at  $gain\ 1 = 0.1V/V$ , and the ring-tone gain is set to  $gain\ 2 = 2V/V$ , the resistor values would be

$R_{I1} = 3M\Omega$ , and  $R_{I2} = 150k\Omega$

The high pass corner frequency of the single-ended input is set by  $C_{I2}$ . If the desired corner frequency is less than 20 Hz.

$$C_{I2} > \frac{1}{(2\pi 150k\Omega \times 20\text{Hz})} \quad (9)$$

$$C_{I2} > 53\text{pF} \quad (10)$$

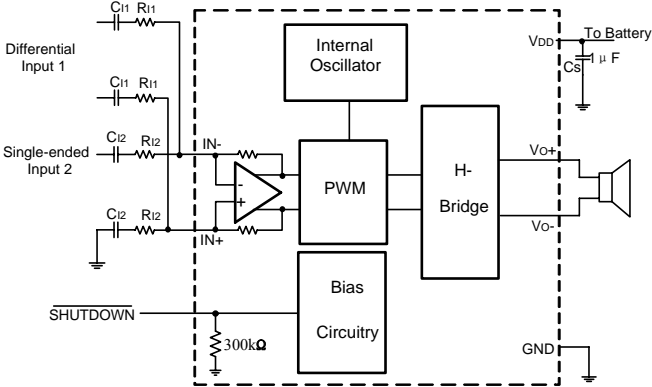


Figure 17. Application Schematic with SN2005 Summing Differential Input and Single-Ended Input Signals

**Summing Two Single-Ended Input Signals**

The gain and corner frequencies ( $f_{c1}$  and  $f_{c2}$ ) for each input source can be set independently (see equations (11) through (14), and Figure 18). Resistor,  $R_p$ , and capacitor,  $C_p$ , are needed on the IN- terminal to match the impedance on the IN+ terminal.

The single-ended inputs must be driven by low impedance sources.

$$Gain1 = \frac{V_o}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left( \frac{V}{V} \right) \tag{11}$$

$$Gain2 = \frac{V_o}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left( \frac{V}{V} \right) \tag{12}$$

$$C_{I1} = \frac{1}{(2\pi R_{I1} f_{c1})} \tag{13}$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \tag{14}$$

$$C_p = C_{I1} + C_{I2} \tag{15}$$

$$R_p = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \tag{16}$$

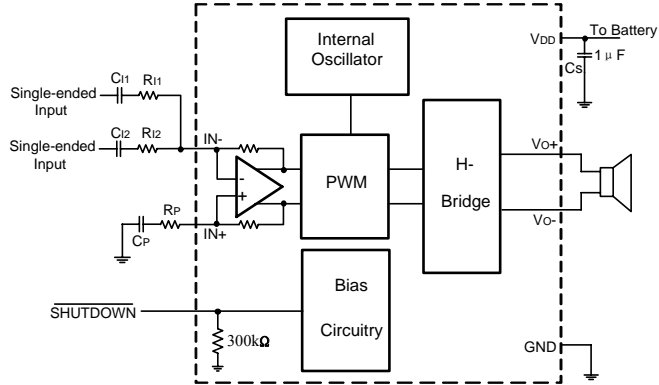
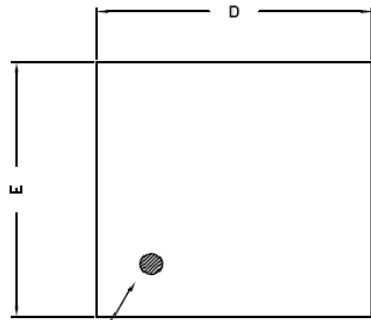


Figure 18. Application Schematic with SN2005 Summing Two Single-Ended Inputs

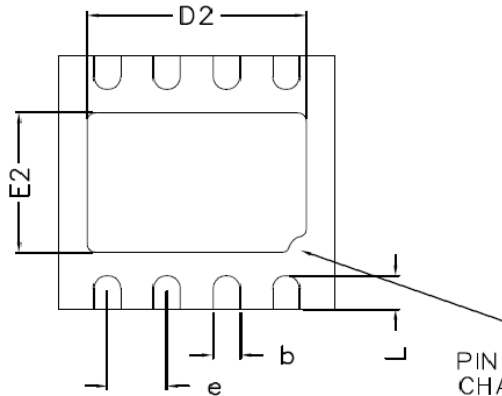
Packaging Information

DFN-8



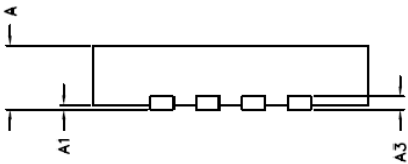
PIN 1 DOT BY MARKING

TOP VIEW



PIN #1 IDENTIF CHAMFER

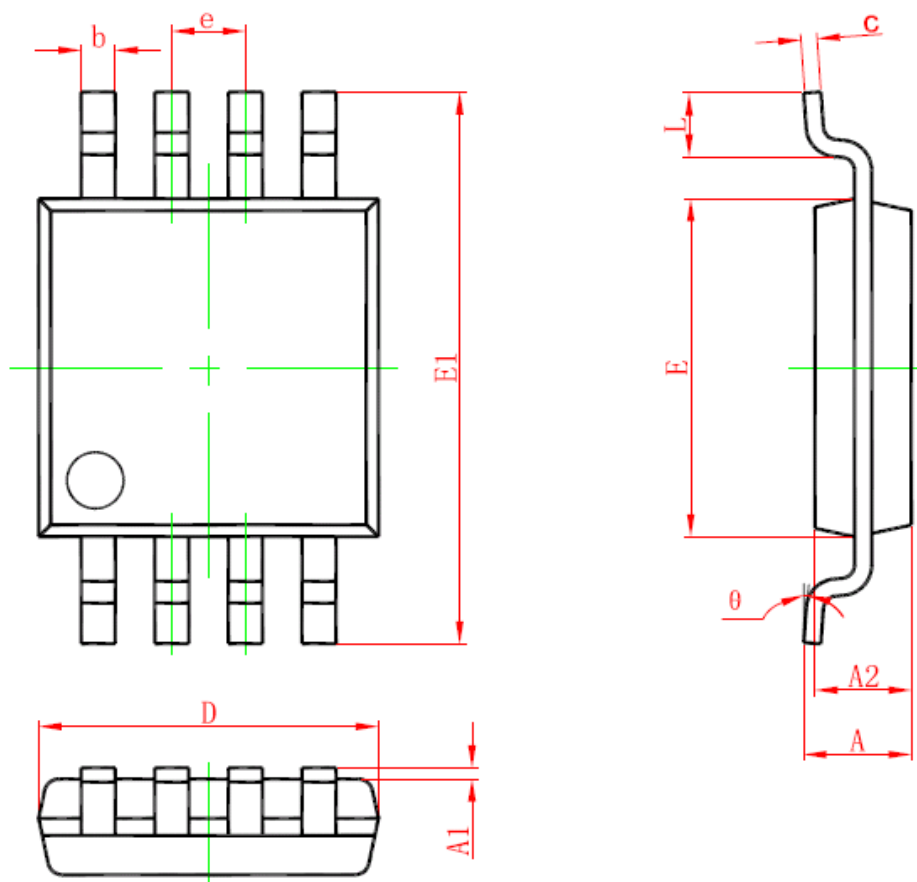
BOTTOM VIEW



SIDE VIEW

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	PKG.	VERY VERY THIN	
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.20 REF.		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
b	0.18	0.30	0.35
L	0.30	0.40	0.58
D2	1.95	2.39	2.49
E2	1.40	1.651	1.75
e	0.65 BSC.		

## MSOP-8



Symbol	Dimension (mm)		
	MIN	TYP	MAX
A	0.82	1.02	1.10
A1	0.02	—	0.15
A2	0.75	0.85	0.95
b	0.25	0.32	0.38
c	0.09	0.16	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.75	4.90	5.05
e	—	0.65	—
L	0.40	0.60	0.80
θ	0	3	6

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