

TMS320DM6437
Evaluation Module

*Technical
Reference*

TMS320DM6437 Evaluation Module Technical Reference

509105-0001 Rev. C
December 2006

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About This Manual

This document describes the board level operations of the DM6437 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM6437 Processor.

The DM6437 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM6437 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM6437 Evaluation Module will sometimes be referred to as the DM6437 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding this device can be found at the following Texas Instruments website:

<http://www.ti.com>

Table 1: Manual History

| Revision | History |
|----------|---------------|
| A | Alpha Release |
| B | Beta Release |

Table 2: Board History

| Revision | History |
|----------|---------------|
| A | Alpha Release |
| B | Beta Release |

Chapter 1

Introduction to the DM6437 EVM

Chapter One provides a description of the DM6437 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM6437 EVM is a PCI based or standalone development platform that enables users to evaluate and develop applications for the TI DaVinci™ processor family. Schematics, list of materials, and application notes are available to ease hardware development and reduce time to market.

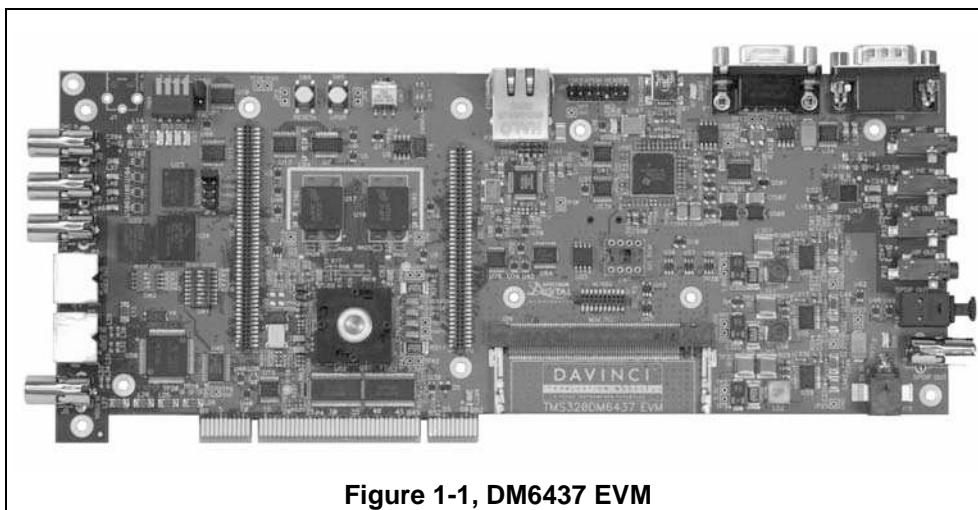


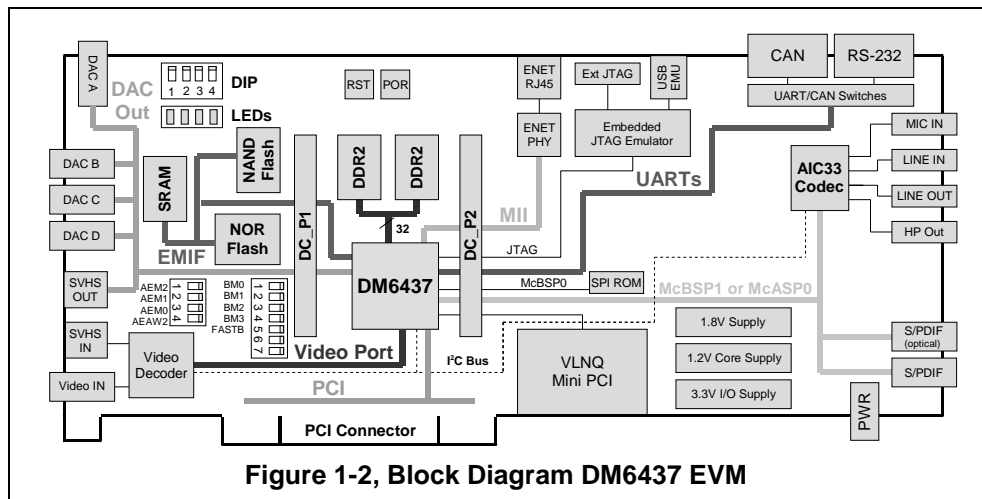
Figure 1-1, DM6437 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM6437 processor operating up to 600 Mhz.
- 1 TVP5146M2 video decoder, supports composite or S video
- 4 video DAC outputs - component, RGB, composite (3 populated)
- 128 Mbytes of DDR2 DRAM
- UART, CAN I/O Interfaces
- 16 Mbytes of non-volatile Flash memory, 64 Mbytes NAND Flash, 2 Mbytes SRAM
- AIC33 stereo codec
- I²C Interface with onboard eeprom and expanders
- 10/100 MBS Ethernet Interface
- Configurable boot load options
- Embedded JTAG emulation interface
- 4 user LEDs and 4 position user switch

- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- VLYNQ Interface
- S/PDIF Interface, analog, and optical

1.2 Functional Overview of the DM6437 EVM



The DM6437 on the EVM interfaces to on-board peripherals through integrated device interfaces and a 8-bit wide EMIF bus. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is jumper selectable to be connected to the Flash, SRAM, NAND, and daughter card expansion connectors which are used for add-on boards.

On board video decoder and on chip encoders interface video streams to the DM6437 processor. One TVP5146M2 decoder and 4 on chip DAC channels are standard on the EVM (only 3 output connectors are populated so that the board can fit in a PCI slot). On screen display functions are implemented in software on the DM6437 processor.

An on-board AIC33 codec allows the DSP to transmit and receive analog audio signals. The I²C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, line output, and headphone outputs.

The EVM includes 4 user LEDs, and 4 position user DIP switch which can be used to provide the user with interactive feedback. These interfaces are implemented via I²C expanders.

VLYNQ, and ethernet MAC interfaces are integrated peripherals on the DM6437 processor exploiting its system on a chip architecture. VLYNQ is available when the PCI is not used.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V DDR2 memory. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the EVM through an embedded emulator or via the 14 pin external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development. Code Composer communicates with the board through the embedded emulator or an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DaVinci family of processors have a large byte addressable address space, some limitations to byte addressing are determined by peripheral interconnection to the DM6437 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a DM6437 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The Flash, NAND Flash, or SRAM are mapped into CS2 space and selectable via JP2. When CS2 is used for daughter card interfacing JP2 must be set appropriately.

| Address | DM6437 EVM |
|------------|------------|
| 0x10800000 | Cache/RAM |
| 0x42000000 | CS2 |
| 0x44000000 | CS3 |
| 0x46000000 | CS4 |
| 0x48000000 | CS5 |
| 0x4C000000 | VLNQ |
| 0x80000000 | DDR |

Figure 1-3, Memory Map, DM6437 EVM

1.5 Configuration Switch Settings

The EVM has a two configuration switches that allow users to control the operational state of the processor when it is released from reset. The configuration switches are labeled SW1 and SW2 on the EVM board.

Switch SW1 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to EMIF boot (out of 8-bit Flash). The DM6437 EVM only supports little endian mode and is not configurable. Refer to section 3.5.1 for the boot load options using switch SW1.

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J16), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM6437 DDR2 interface, and DDR2 memory.

There are three power test points on the EVM; TP23, TP34, and TP38. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 1: Power Test Points

| Test Point | Voltage | Voltage Use |
|------------|---------|---------------------------------|
| TP23 | +1.2 V | DM6437 Core |
| TP34 | +3.3V | DSP I/O and logic |
| TP38 | +1.8 V | DDR2 Memory, DSP I/O, and logic |

1.7 Power Measurement

The EVM supports power test points to allow measurement of the various power rails on the DM6437 device. Series resistors are used in the device's power domains thereby measuring the voltage across these resistors. The current can be calculated via $V = I * R$.

Refer to the test point section in chapter 3 for detailed information on measuring current on the DM6437 device.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM6437 EVM.

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2.1 EMIF Interfaces

A separate 8 bit EMIF with multiple chip selects divide up the address space and allow for asynchronous accesses on the EVM. On board the CS2 is used for Flash, NAND Flash, or SRAM.

2.1.1 DDR2 Memory Interface

The DM6437 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two 512 megabit 16 bit wide memories on this bus, for a total of 128 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM6437 internal DDR controller.

2.1.2 Flash, NAND Flash, SRAM Memory Interface

The DM6437 has 16 megabytes of NOR Flash, or 64 megabytes of NAND Flash, or 2 megabyte of SRAM memory mapped into the CS2 space. This NOR Flash memory, and NAND Flash memory are used primarily for boot loading. SRAM is used for debugging application code. The CS2 space is configured as 8 bits wide on the DM6437 EVM for NOR Flash, SRAM, or NAND flash usage.

2.2 Peripheral Interfaces

The DM6437 has several peripheral interfaces which allow the user to interface to external devices. These interfaces are outlined in the following sections.

2.2.1 VLYNQ Interface

The DM6437 brings its internal VLYNQ interface out to a mini PCI connector J20 and small 20 pin connector DC_P3. The VLYNQ interface is multiplexed on the PCI/EM bus and this bus must be reconfigured after boot up to support VLYNQ. A multiplexer is used to minimize board layout stubs and allow as direct as possible interface for the VLYNQ signals. VLYNQ is not operational if the board is used in a PCI slot.

2.2.2 UART Interface

The internal UART0 on the DM6437 device is driven to connector P8. The UART's interface is routed to a Texas Instruments MAX3221 RS-232 line driver prior to being brought out to a male DB-9 connector, P8. The on board UART signals can be disabled by pulling the RS232_ENABLEn signal high via the daughter card connectors.

2.2.3 CAN Interface

The internal CAN controller on the DM6437 device is driven to connector P7. The controller is routed to a Texas Instruments SN65HVD235 CAN controller prior to being routed to female DB-9 connector, P7. The on board CAN signals can be disabled by pulling CAN_ENABLEn high via the daughter card connector.

2.3 Video Interfaces

The DM6437 EVM has video input and output ports to support a variety of user applications. These are discussed in the two sections below.

2.3.1 Input Video Port Interfaces

The DM6437 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146M2 is used to decode composite video or S-video inputs into the device. P2 is used for the S-video inputs and J5 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC_P1 when the on board CBTs are disabled by driving control TVP5146_ENABLEn signal high on DC_P1.

2.3.2 On Chip Video Output DACs

The DM6437 incorporates 4 output DACs to interface to various output standards. The DACs are buffered via opamps and driven to four RCA jacks, J1-J4. The outputs of the DACs are programmable to support composite video, component video, or RGB.

S-video output is available from connector P1. This connector is driven by video DACs B and C from the DM6437. Video DAC B is the chroma and video DAC C is the luma.

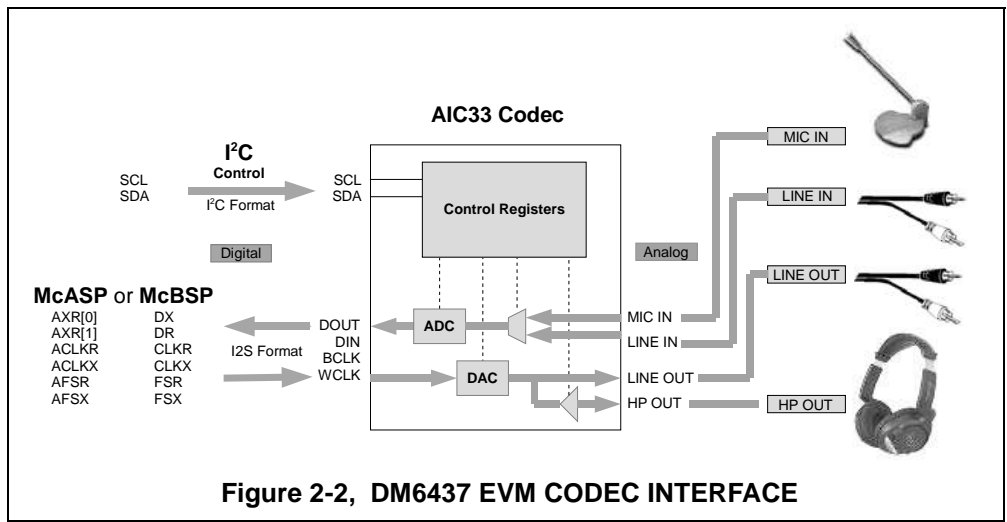
2.4 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec’s internal configuration registers and one to send and receive digital audio samples. The I²C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The default configuration is to use the McBSP is used as the bi-directional data channel. However, optionally the McASP can be used to drive the data channel. Data channel selection is controller via an on board I²C expander. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec has a programmable clock from a PLL1705 PLL device. The default system clock is 18.432 Mhz. The internal sample rate generate subdivides the 18.432 MHz clock to generate common frequencies such as 48KHz and 8KHz. The sample rate is set by a codec register. The figure below shows the codec interface on the DM6437 EVM.



2.4.1 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM6437 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

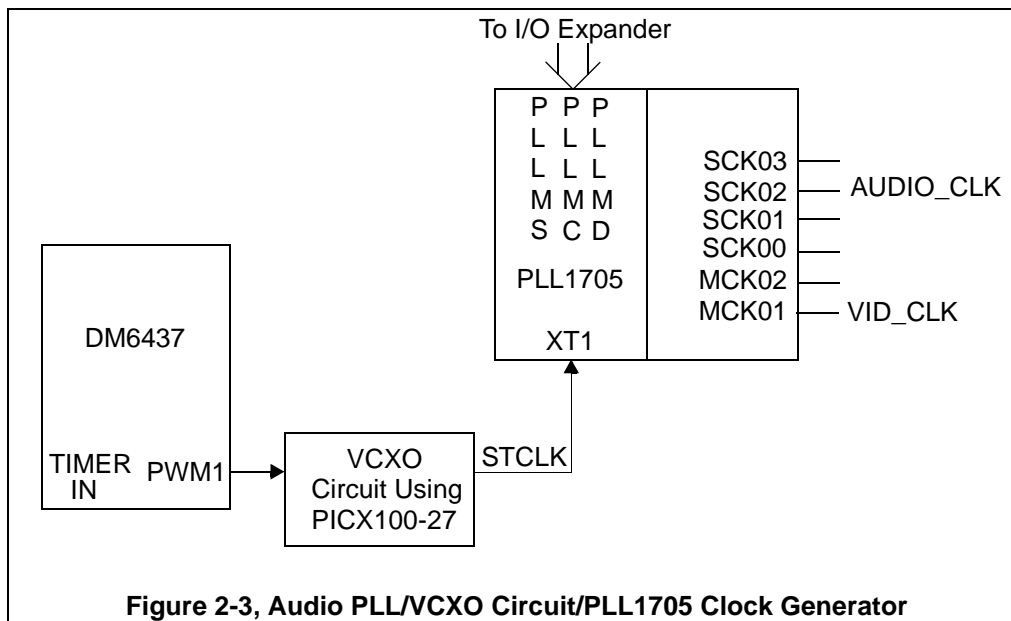
In streaming video applications the audio and video sequences can lose synchronization. The DM6437 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM1 and timer inputs on DM6437 are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I²C and Expander U13. Software sequencing on the I/O expander is required to interface correctly to the PLL1705's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.



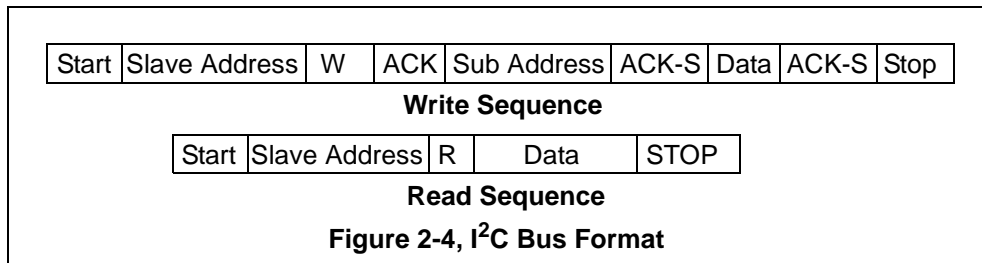
2.5 Ethernet Interface

The DM6437 integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Micrel KS8001L PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P3. The PHY directly interfaces to the DM6437. The ethernet address is stored in the I²C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.6 I²C Interface

The I²C bus on the DM6437 is ideal for interfacing to the control registers of many devices. On the DM6437 EVM the I²C bus is used to configure the video decoder, stereo Codec, I/O expanders. An I²C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.



The addresses of the on board peripherals are shown in the table below.

Table 1: I²C Memory Map

| Device | Address | R/W | Device | Function |
|-------------|---------|-----|--------|-------------------------|
| TVP5146M2 | 0x5D | R/W | U50 | Video Decoder |
| PCF 8574A | 0x38 | R/W | U10 | User Input |
| PCF 8574A | 0x39 | R/W | U11 | User LEDs |
| PCF 8574A | 0x3A | R/W | U13 | PLL, User I/O |
| PCF8574A | 0x3B | R/W | U64 | User I/O |
| TLV320AIC33 | 0x1B | R/W | U43 | CODEC |
| 24WC256 | 0x50 | R/W | U25 | I ² C EEPROM |

2.6.1 I/O Expanders

The DM6437 EVM uses four I²C expanders to handle various bit I/O functions. Each of these is an 8 bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 2: U10 I/O Expander

| Pin Number | Function | Description |
|------------|---------------------|-------------------------------------|
| P0 | JP1 NTSC/PAL Select | Read only video mode, 1=NTSC, 0=PAL |
| P1 | SW7 Slide Switch | Read only slide switch |
| P2 | Reserved | None |
| P3 | Reserved | None |
| P4 | SW4-1 | Read only user switch |
| P5 | SW4-2 | Read only user switch |
| P6 | SW4-3 | Read only user switch |
| P7 | SW4-4 | Read only user switch |

Table 3: U11 I/O Expander

| Pin Number | Function | Description |
|------------|----------------|----------------------------------|
| P0 | User LED DS1 | 0=Turns LED on, 1=Turns LED off |
| P1 | User LED DS2 | 0=Turns LED on, 1=Turns LED off |
| P2 | User LED DS3 | 0=Turns LED on, 1=Turns LED off |
| P3 | User LED DS4 | 0=Turns LED on, 1=Turns LED off |
| P4 | VLYNQ Reset | 0=Removes Reset, 1=Applies Reset |
| P5 | Reserved | None |
| P6 | User I/O DC_P2 | To daughter card, DC_P2 Pin 81 |
| P7 | User I/O DC_P2 | To daughter card, DC_P2 Pin 82 |

Table 4: U13 I/O Expander

| Pin Number | Function | Mode | Description |
|------------|-----------|------|-----------------------------|
| P0 | User I/O | RW | Daughter Card, DC_P2 Pin 87 |
| P1 | User I/O | RW | Daughter Card, DC_P2 Pin 88 |
| P2 | User I/O | RW | Daughter Card, DC_P2 Pin 85 |
| P3 | User I/O | RW | Daughter Card, DC_P2 Pin 84 |
| P4 | PLL -SR | W | Write PLL1705 SR Pin |
| P5 | PLL - FS2 | W | Write PLL1705 FS2 Pin |
| P6 | PLL - FS1 | W | Write PLL1705 FS1 Pin |
| P7 | PLL-CSEL | W | Write PLL1705 CSEL Pin |

Table 5: U64 I/O Expander

| Pin Number | Function | Description |
|------------|-----------------------|-----------------------------|
| P0 | McBSP_Enable to AIC23 | * 1=Enable, 0=Disable |
| P1 | McASP_Enable to AIC23 | * 0=Enable, 1=Disable |
| P2 | SPDIF Enable | * 0=Enable, 1=Disable |
| P3 | Reserved | None |
| P4 | Reserved | None |
| P5 | Reserved | None |
| P6 | Reserved | None |
| P7 | Core Voltage Select | 0 = 1.05 Volt, 1 = 1.2 Volt |

* only one should be enabled at a time

2.6.2 I²C EEPROM

The DM7436 EVM incorporates an I²C eeprom that can be used for booting or general purpose storage.

This eeprom is also used to store the ethernet MAC address and the board's revision. The MAC address is also labeled on the board. Care should be taken not to erase these items when user information is stored in the eeprom. Spectrum Digital uses addresses 0x7F00 to 0x7FFF for manufacturing information. This information is shown in the table below.

Table 6: DM6437 MAC Addresses

| Address | Contents |
|---------|--------------------------------------|
| 0x7F00 | EMAC Address 0 (most significant) |
| 0x7F01 | EMAC Address 1 |
| 0x7F02 | EMAC Address 2 |
| 0x7F03 | EMAC Address 3 |
| 0x7F04 | EMAC Address 4 |
| 0x7F05 | EMAC Address 5 |
| 0x7F06 | Reserved |
| 0x7F07 | Board Revision |

2.7 S/PDIF Analog, and Optical Interfaces

The McBSP's FSR pin on the DM6437 can be configured to operate as a S/PDIF transmitter. The DM6437 EVM supports both analog and optical interfaces. The analog S/PDIF output pin is routed to a driver and filter circuit before being output on J10. I²C Expander U64 output P2 is used to enable the S/PDIF interface. When S/PDIF is selected on the expander (P2=0), the McASP enable should be disabled and the McBSP enable should be disabled. Another driver is used to interface the optical transmitter P14. When the S/PDIF interface is enabled the TLV320AIC33 codec is disabled, the WCLK should be disabled prior to enabling the S/PDIF output.

The McBSP interface can be disabled for daughter card use by pulling the AIC_ENABLEn signal high from the daughter card connector.

2.8 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

The pin outs for this interface are documented in Section 3.

The connectors provide access to the DSP's EMIF signals to interface with memories and memory mapped devices. The video capture port is brought out to the daughter card interface.

Several signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 7: Daughter Card Interface

| Signal | Function |
|--------------------|--|
| AIC33_ENABLEn | Disconnects CPU from on board codec |
| CI_EMA_ENABLEn | Disables CI0 to CI7 from upper on board EMIF address lines |
| MEM_EMD7-0_ENABLEn | Disables CPU from on board data bus |
| VIC_TINPOL_ENABLEn | Disable CPU TINPOL pin from on board use |
| ENET_ENABLEn | Disconnects CPU from on board ethernet PHY |
| CAN_ENABLEn | Disconnects CPU from on board CAN |
| RS232_ENABLEn | Disconnects CPU from on board UART |
| TVP5146_ENABLEn | Disconnects CPU from on board video decoder |

Other than the buffering, most daughter card signals are not modified on the board.

2.9 DM6437 Core CPU Clock

The DM6437 EVM uses a 27 Megahertz crystal to generate the input clock. The DM6437 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM6437 device.

2.10 DM6437 Core Voltage Select

The DM6437 EVM has the ability to adjust the core voltage between 1.2 volts and 1.05 volts. an I/O expander is used to control this I²C feature.

Chapter 3

Physical Description

This chapter describes the physical layout of the DM6437 EVM and its interfaces.

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3.1 Board Layout

The DM6437 EVM is a 8.75 x 4.5 inch (210 x 115 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the DM6437 EVM.

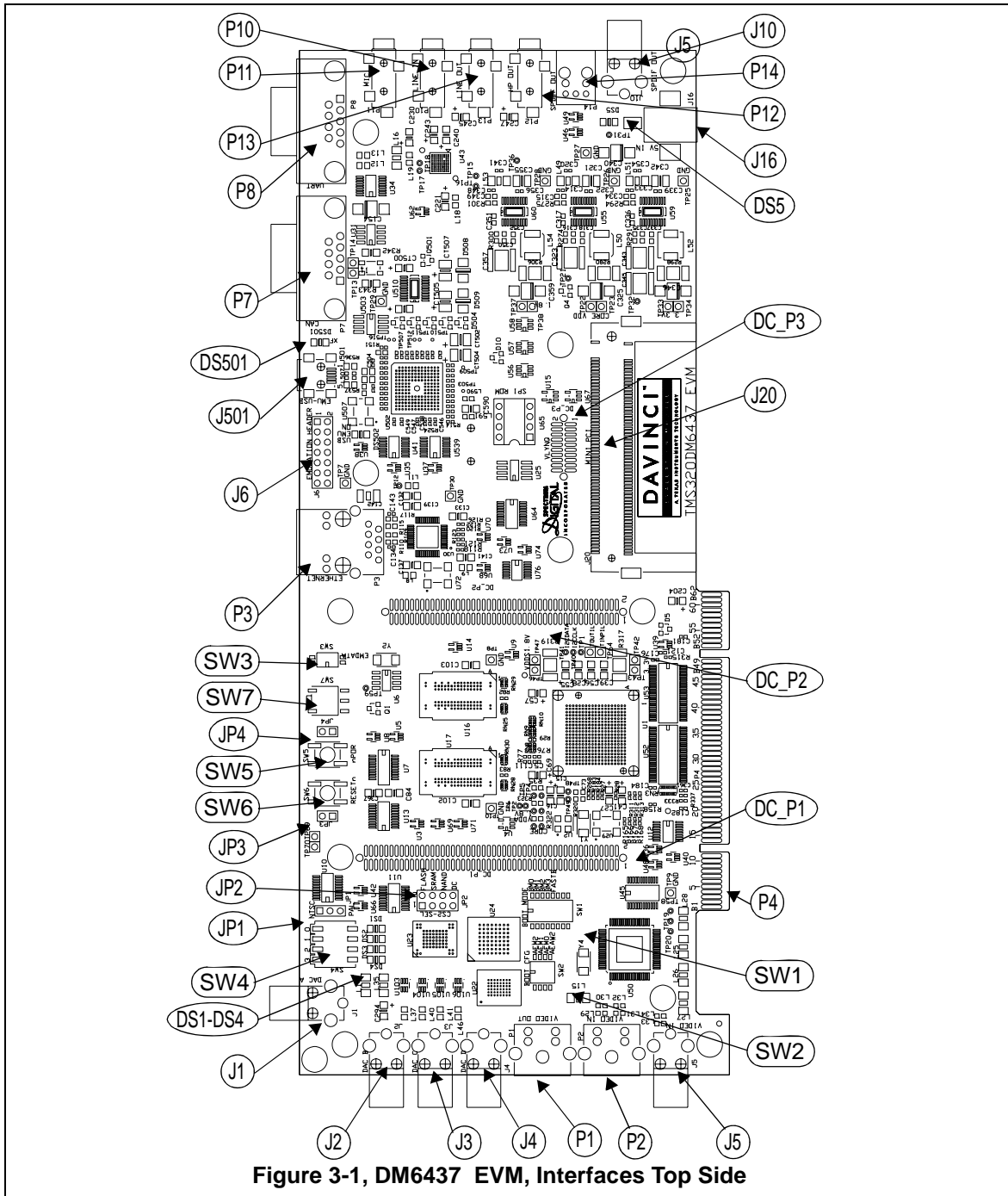


Figure 3-1, DM6437 EVM, Interfaces Top Side

3.2 Connectors

The EVM has twenty three (23) connectors providing interfaces to various peripherals. These connectors are described in the following sections.

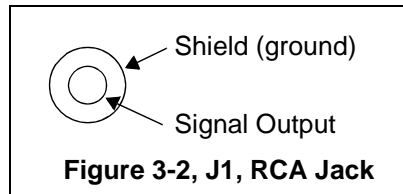
Table 1: Connectors

| Connector | Size | Function |
|-----------|-------------|----------------------------------|
| J1 | RCA | DAC A * |
| J2 | RCA | DAC B |
| J3 | RCA | DAC C |
| J4 | RCA | DAC D |
| J5 | RCA | Video In |
| J6 | 14 | External Emulation Header |
| J10 | RCA | S/PDIF Out |
| J16 | 2.5 mm | +5V In |
| J20 | 2 x 62 | Mini PCI Interface |
| J501 | Mini USB | Embedded USB Emulation Interface |
| P1 | 4 Pin DIN | S-Video Out |
| P2 | 4 Pin DIN | S-Video In |
| P3 | RJ-45 | Ethernet |
| P4 | PCI | PCI |
| P7 | 9 Pin D-sub | CAN |
| P8 | 9 Pin D-sub | RS-232 UART |
| P10 | 3.5 mm | Stereo Line In |
| P11 | 3.5 mm | Microphone In |
| P12 | 3.5 mm | Headphone Out |
| P13 | 3.5 mm | Stereo Line Out |
| P14 | Optical | S/PDIF Out |
| DC_P1 | 2x50 | Expansion |
| DC_P2 | 2x45 | Expansion |
| DC_P3 | 2x10 | Expansion |

* Not populated

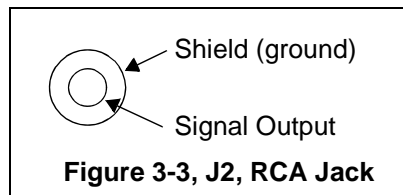
3.2.1 J1, DAC A Video Out

J1 is an RCA jack used to interface to DAC A of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.



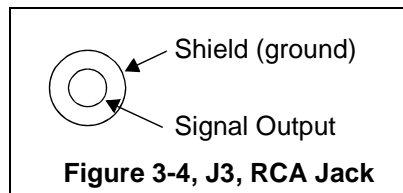
3.2.2 J2, DAC B Video Out

J2 is an RCA jack used to interface to DAC B of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.



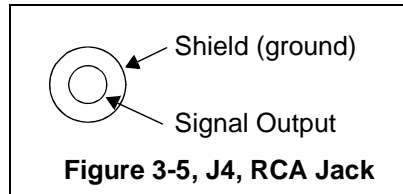
3.2.3 J3, DAC C Video Out

J3 is an RCA jack used to interface to DAC C of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.



3.2.4 J4, DAC D Video Out

J1 is an RCA jack used to interface to DAC D of the DM6437 to a video device. This connector is driven directly by the VPSS back end via an opamp. This connector is not installed for clearance reasons when using the PCI bus. The pinout of this connector is shown below.



3.2.5 J5, Video In

J5 is an RCA jack used as a video input to the TVP5146M2 video decoder. This connector brings in a video signal to the TVP5146M2. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

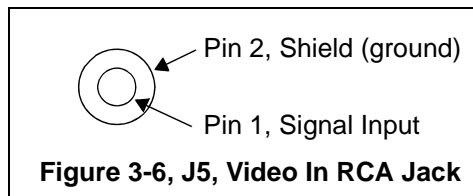


Table 2: J5, Video In, RCA Jack

| Pin # | Signal Name |
|-------|------------------|
| 1 | Pin 8, TVP5146M2 |
| 2 | GND |

3.2.6 J10, S/PDIF Out

J10 is an RCA jack used as an analog output from the McBSP FSR signal on the DSP. This connector brings out the SPDIF signal. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

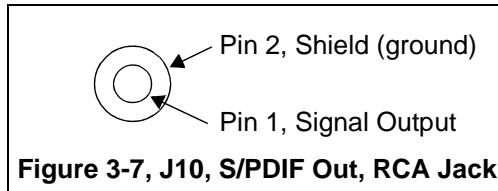
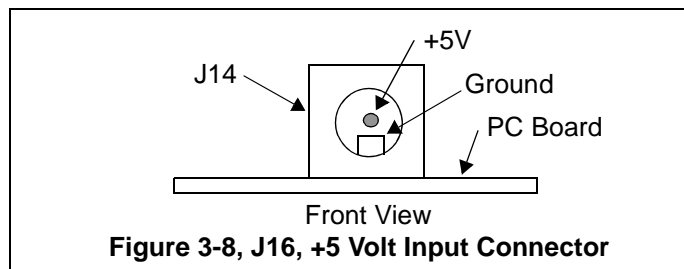


Table 3: J10, S/PDIF, RCA Jack

| Pin # | Signal Name |
|-------|----------------------|
| 1 | S/PDIF Analog output |
| 2 | GND |

3.2.7 J16, +5V Input

Connector J16 is the input power connector. This connector bring in +5 volts to the EVM. This is a 2.5 mm. jack. The figure below shows this connector as viewed from the card edge.



3.2.8 J20, Mini PCI Interface

Connector J20 provides a mini-PCI on the DM6437 EVM. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector.

Table 4: J16, VLYNQ Card Interface

| Pin # | Signal |
|--|-------------|
| 2,3,4,5,6,7,8,10,11, 12,13,15,17,18,29, 30,38,39,47,49,51, 53,55,57,71,73,75, 77,80,82,84,86,93, 98,100,104,105, 106,107,108,109, 113,115,116,117, 118,120,122,123, 124 | NC |
| 9,14,20,23,25,27 32,33,34,35,37,41, 42,44,45,46,48,50, 52,54,56,58,60,62, 64,66,68,69,72,74, 76,78,79,81,83,85, 87,90,91,92,94,95, 96,99,101,102, 110,114,119 | GND |
| 111 | VCC_1.8V |
| 1,19,28,31,40,63, 70,88,89 | VCC_3.3V |
| 97,103 | VCC_5V |
| 16 | VLYNQ_CLK |
| 21 | VLYNQ_RXD0 |
| 22 | VLYNQ_RXD1 |
| 24 | VLYNQ_SCRUN |
| 26 | VLYNQ_RESET |
| 59 | VLYNQ_RXD2 |
| 61 | VLYNQ_RXD3 |
| 36 | VLYNQ_TXD0 |
| 65 | VLYNQ_TXD2 |
| 67 | VLYNQ_TXD3 |
| 43 | VLYNQ_TXD1 |

3.2.9 J501, Embedded Mini USB Emulation Interface

This connector allows the user to run software development tools and emulation without an external emulator. The signals on this connector are shown in the table below.

Table 5: J501, Embedded Mini USB Emulation Interface

| Pin # | Signal Name |
|-------|---------------|
| 1 | VBUS |
| 2 | D- |
| 3 | D+ |
| 4 | ID (not used) |
| 5 | Ground |

3.2.10 P1, Video Out

Connector P1 is a four pin mini din connector which interfaces to an S-video output display device. This connector brings out the DAC B and DAC C. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

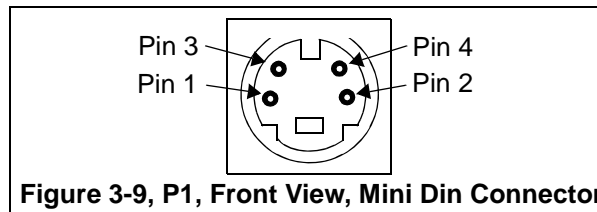


Figure 3-9, P1, Front View, Mini Din Connector

Table 6: P1, Video Out, Mini Din Connector

| Pin # | Signal Name |
|-------|-------------------|
| 1 | Ground |
| 2 | Ground |
| 3 | DAC_IOUTB, Luma |
| 4 | DAC_IOUTC, Chroma |

3.2.11 P2, Video In

Connector P2 is a four pin mini din S-video connector which interfaces to the TVP5146M2 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146M2. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

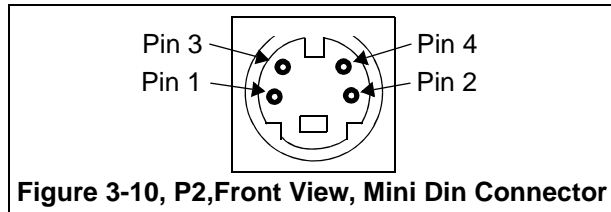


Figure 3-10, P2,Front View, Mini Din Connector

Table 7: J11, Video In, Mini Din Connector

| Pin # | Signal Name |
|-------|-------------|
| 1 | GND |
| 2 | GND |
| 3 | LUMA |
| 4 | Chroma |

3.2.12 P3, Ethernet Interface

The P3 connector is used to provide an 10/100 Mbps Ethernet interface. This is a standard RJ-45 connector. The pinout for the P3 connector is shown in the table below.

Table 8: P3, Ethernet Interface

| Pin # | Signal | Pin # | Signal |
|-------|---------|-------|----------|
| 1 | LXT_TDP | 2 | LXT_TDM |
| 3 | LXT_RDP | 4 | LXT_TDCT |
| 5 | NC | 6 | LXT_RDM |
| 7 | NC | 8 | GND |

Two LEDs are embedded into the connector to report link status.

Table 9: Ethernet LEDs

| LED # | Color |
|-------|--------|
| LED1 | Green |
| LED2 | Yellow |

3.2.13 P4, PCI Connector

The P4 connector is a card edge PCI interface. This connector has an “A” and “B” side. Because of the card seating notches the pin numbers are not contiguous. The “B” side is the top component side. The I/O direction field is referenced from the PCI slot.

Table 10: P4, PCI Connector, “A” Side

| Pin | Signal | I/O | Description | Pin | Signal | I/O | Description |
|-----|------------|-------|-----------------|-----|-----------|-------|------------------------------|
| 1 | TRST- | | Not Used | 2 | +12 Volts | | Not Used |
| 3 | TMS | | Not Used | 4 | TDI | I/O | Tied to TDO |
| 5 | +5 Volts | | +5 Volts Power | 6 | INTA- | O | Interrupt Out |
| 7 | INTC- | O | Interrupt Out | 8 | +5 Volts | | +5 Volts Power |
| 9 | Rsvd.0 | | Not Used | 10 | +V I/O | | Not Used |
| 11 | Rsvd.1 | | Not Used | 12 | Key.1 | | Key |
| 13 | Key.2 | | Key | 14 | +3.3 Vaux | | Not Used |
| 15 | RST- | I | PCI_Resetn | 16 | +V I/O | O | Not Used |
| 17 | GNT- | O | Grant- | 18 | GND | | Ground |
| 19 | PME- | | | 20 | AD30 | I/O/Z | Address/Data 30 |
| 21 | +3.3 Volts | | Not Used | 22 | AD28 | I/O/Z | Address/Data 28 |
| 23 | AD26 | I/O/Z | Address/Data 26 | 24 | GND | | |
| 25 | AD24 | I/O/Z | Address/Data 24 | 26 | IDSEL | I | Initialization Device Select |
| 27 | +3.3 Volts | | Not Used | 28 | AD22 | I/O/Z | Address/Data 22 |
| 29 | AD20 | I/O/Z | Address/Data 20 | 30 | GND | | Ground |
| 31 | AD18 | I/O/Z | Address/Data 18 | 32 | AD16 | I/O/Z | Address/Data 16 |
| 33 | +3.3 Volts | | Not Used | 34 | FRAME- | I | Frame |
| 35 | GND | | Ground | 36 | TRDY- | I/O/Z | Target Ready |
| 37 | GND | | Ground | 38 | STOP- | I/O/Z | Stop Direction |
| 39 | +3.3 Volts | | Not Used | 40 | SDONE | O | Done |
| 41 | SBO- | | | 42 | GND | | Ground |
| 43 | PAR | I/O/Z | Parity | 44 | AD15 | I/O/Z | Address/Data 15 |
| 45 | +3.3 Volts | | Not Used | 46 | AD13 | I/O/Z | Address/Data 13 |
| 47 | AD11 | I/O/Z | Address/Data 11 | 48 | GND | | Ground |
| 49 | AD9 | I/O/Z | Address/Data 9 | 50 | Key.3 | | Key |
| 51 | Key.4 | | Key | 52 | C/BE0 | | Command/Byte Enable0 |
| 53 | +3.3 Volts | | Not Used | 54 | AD6 | I/O/Z | Address/Data 6 |
| 55 | AD4 | I/O/Z | Address/Data 4 | 56 | GND | | Ground |
| 57 | AD2 | I/O/Z | Address/Data 2 | 58 | AD0 | I/O/Z | Address/Data 0 |
| 59 | +V I/O | | Not Used | 60 | REQ64- | | Not Used |
| 61 | +5 Volts | | +5 Volts Power | 62 | +5 Volts | | +5 Volts Power |

The signals on the “B” side of the connector are shown in the table below.

Table 11: P4, PCI Connector, “B” Side

| Pin | Signal | I/O | Description | Pin | Signal | I/O | Description |
|-----|------------|-------|-----------------------|-----|------------|-------|-----------------------|
| 1 | -12 Volts | | Not Used | 2 | TCK | I | Not Used |
| 3 | GND | | Ground | 4 | TDO | I | Tied to TDO |
| 5 | +5 Volts | | +5 Volt Power | 6 | +5 Volts | I | +5 Volt Power |
| 7 | INTB- | | Interrupt OUT | 8 | INTD- | | Interrupt Out |
| 9 | PRSNT1- | O | Power Requirement | 10 | Rsvd.2 | | |
| 11 | PRSNT2- | O | Power Requirement | 12 | Key.5 | | Key |
| 13 | Key.6 | | Key | 14 | Rsvd.3 | | |
| 15 | GND | | Ground | 16 | CLK | | System Clock |
| 17 | GND | | Ground | 18 | REQ- | | |
| 19 | +V I/O | | Not Used | 20 | AD31 | I/O/Z | Address/Data 31 |
| 21 | AD29 | I/O/Z | Address/Data 29 | 22 | GND | | Ground |
| 23 | AD27 | I/O/Z | Address/Data 27 | 24 | AD25 | I/O/Z | Address/Data 25 |
| 25 | +3.3 Volts | | Not Used | 26 | C/BE3 | I/O/Z | Command/Byte Enable 3 |
| 27 | AD23 | I/O/Z | Address/Data 23 | 28 | GND | | Ground |
| 29 | AD21 | I/O/Z | Address/Data 21 | 30 | AD19 | I/O/Z | Address/Data 19 |
| 31 | +3.3 Volts | | Not Used | 32 | AD17 | I/O/Z | Address/Data 17 |
| 33 | C/BE2- | I/O/Z | Command/Byte Enable 2 | 34 | GND | | Ground |
| 35 | IRDY- | I | Initiator Ready | 36 | +3.3 Volts | | Not Used |
| 37 | DEVSEL- | I/O/Z | Device Select | 38 | GND | | Ground |
| 39 | LOCK- | I | Resource Locked | 40 | PERR- | I/O/Z | Parity Error |
| 41 | +3.3 Volts | | Not Used | 42 | SERR- | O | System Error |
| 43 | +3.3 Volts | | Not Used | 44 | C/BE1- | I/O/Z | Command/Byte Enable 1 |
| 45 | AD14 | I/O/Z | Address/Data 14 | 46 | GND | | Ground |
| 47 | AD12 | I/O/Z | Address/Data 12 | 48 | AD10 | I/O/Z | Address/Data 10 |
| 49 | M66EN | O | 66 Mhz Enable | 50 | Key.7 | | Key |
| 51 | Key.8 | | Key | 52 | AD8 | I/O/Z | Address/Data 8 |
| 53 | AD7 | I/O/Z | Address/Data 7 | 54 | +3.3 Volts | | Not Used |
| 55 | AD5 | I/O/Z | Address/Data 5 | 56 | AD3 | I/O/Z | Address/Data 3 |
| 57 | GND | | Ground | 58 | AD1 | I/O/Z | Address/Data 1 |
| 59 | +V I/O | | Not Used | 60 | ACK64- | | Not Used |
| 61 | +5 Volts | | +5 Volt Power | 62 | +5 Volts | | +5 Volt Power |

3.2.14 P7, CAN Connector

The DM6437 EVM has a 9 Pin female D-connector which brings out the CAN transmit and receive signals. This CAN interface uses the SN65HVD235 CAN driver. The pin positions for the P7 connector as viewed from the edge of the printed circuit board are shown below.

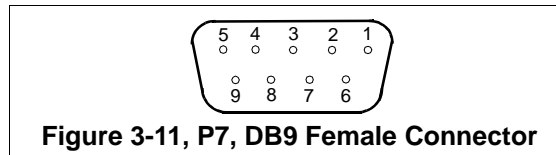


Figure 3-11, P7, DB9 Female Connector

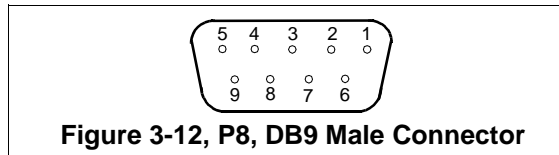
The pin numbers and their corresponding signals are shown in the table below.

Table 12: P7, CANA Pinout

| Pin # | Signal Name |
|-------|-------------|
| 1 | No Connect |
| 2 | CANL |
| 3 | GND |
| 4 | No Connect |
| 5 | No Connect |
| 6 | No Connect |
| 7 | CANH |
| 8 | No Connect |
| 9 | No Connect |

3.2.15 P8, RS-232 UART Connector

The DM6437 EVM has an RS-232 connector which brings out the SCI transmit and receive signals to be used as UART. This UART uses the MAX3221 RS-232 line driver and is routed to a male 9 pin D-connector, P8. The pin positions for the P8 connector as viewed from the edge of the printed circuit board are shown below.



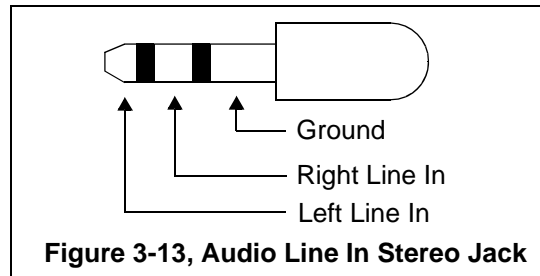
The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 13: P8, RS-232 UART Pinout

| Pin # | Signal Name |
|-------|-------------|
| 1 | No Connect |
| 2 | RXD |
| 3 | TXD |
| 4 | No Connect |
| 5 | GND |
| 6 | No Connect |
| 7 | No Connect |
| 8 | No Connect |
| 9 | No Connect |

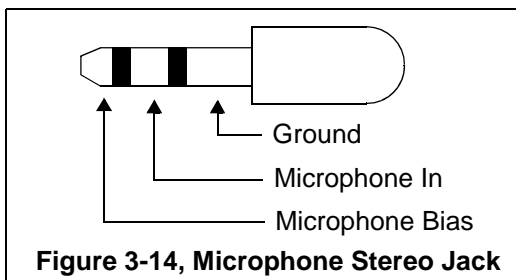
3.2.16 P10, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



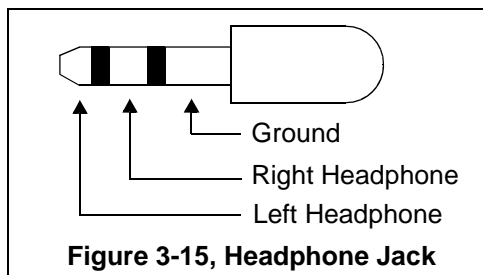
3.2.17 P11, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.



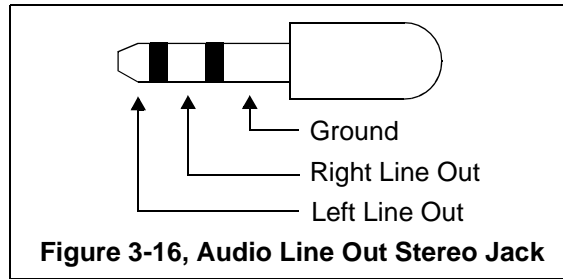
3.2.18 P12, Headphone Connector

Connector P12 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below.



3.2.19 P12, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



3.2.20 P14, S/PDIF Out (Optical)

P14 is an optical transmitter connector used as an output from the McBSP FSR signal on the DM6437 DSP. This connector brings out an optical S/PDIF signal. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

3.2.21 DC_P1, Memory/Video Expansion-

Table 14: DC_P1, Memory/Video Expansion

| Pin | Signal | Conn | Pin | Signal | Conn |
|-----|--------------------------------------|------|-----|--------------------------------------|------|
| 1 | GROUND | | 2 | GROUND | |
| 3 | PCLK_GP[54] | | 4 | Y1_EMD_ENABLEn | |
| 5 | TVP5146_ENABLEn | | 6 | GROUND | |
| 7 | YI3_(CCD3)_GP[39] | | 8 | YI4_(CCD4)_GP[40] | |
| 9 | YI2_(CCD2)_GP[38] | | 10 | YI5_(CCD5)_GP[41] | |
| 11 | TI1_(CCD1)_GP[37] | | 12 | TI6_(CCD6)_GP[42] | |
| 13 | YI0_(CCD0)_GP[36] | | 14 | YI7_(CCD7)_GP[43] | |
| 15 | GROUND | | 16 | GROUND | |
| 17 | C_WE_RNW_GP[35] | | 18 | C_FIELD_EM_A[21]_GP[34] | |
| 19 | VD_GP[53] | | 20 | HD_GP[52] | |
| 21 | CI3_(CDD11)_EM_A[17]_EM_D[04]_GP[47] | | 22 | CI4_(CDD12)_EM_A[16]_EM_D[03]_GP[48] | |
| 23 | CI2_(CDD10)_EM_A[18]_EM_D[05]_GP[46] | | 24 | CI5_(CDD13)_EM_A[15]_EM_D[02]_GP[49] | |
| 25 | CI1_(CDD9)_EM_A[19]_EM_D[06]_GP[45] | | 26 | CI6_(CDD14)_EM_A[14]_EM_D[01]_GP[50] | |
| 27 | CI0_(CDD8)_EM_A[20]_EM_D[07]_GP[44] | | 28 | CI7_(CDD15)_EM_A[13]_EM_D[00]_GP[51] | |
| 29 | GROUND | | 30 | GROUND | |
| 31 | VCLK_GP[31] | | 32 | VSYNC_EM_CS4n_GP[32] | |
| 33 | GROUND | | 34 | GROUND | |
| 35 | VPBECLK_GP[30] | | 36 | HSYNC_EM_CS5n_GP[33] | |
| 37 | GROUND | | 38 | GROUND | |
| 39 | YOUT3_GP[25]_BOOTMODE3 | | 40 | YOUT4_GP[26]_FASTBOOT | |
| 41 | YOUT2_GP[24]_BOOTMODE2 | | 42 | YOUT5_GP[27] | |
| 43 | YOUT1_GP[23]_BOOTMODE1 | | 44 | YOUT6_GP[28] | |
| 45 | YOUT0_GP[22]_BOOTMODE0 | | 46 | YOUT7_GP[29] | |
| 47 | GROUND | | 48 | GROUND | |
| 49 | COUT3_EM_D[3]_GP[17] | | 50 | COUT4_EM_D[4]_GP[18] | |
| 51 | COUT2_EM_D[2]_GP[16] | | 52 | COUT5_EM_D[5]_GP[19] | |
| 53 | COUT1_EM_D[1]_GP[15] | | 54 | COUT6_EM_D[6]_GP[20] | |
| 55 | COUT0_EM_D[0]_GP[14] | | 56 | COUT7_EM_D[7]_GP[21] | |
| 57 | GROUND | | 58 | GROUND | |
| 59 | B0_LCD_FIELD_EM_A[3]_GP[11] | | 60 | R0_EM_A[4]_GP[10]_(AEAW2) | |
| 61 | G1_EM_A[1]_(ALE)_GP[9]_(AEAW1) | | 62 | B1_EMA[2]_(CLE)_GP[8]_(AEAW0) | |
| 63 | R2_EM_BA[0]_GP[6]_(AEM1) | | 64 | R1_EM_A[0]_GP[7]_(AEM2) | |
| 65 | B2_EM_BA[1]_GP[6]_(AEM0) | | 66 | G0_EM_CS2n_GP[12] | |
| 67 | EM_WAIT_(RDY/BSTn) | | 68 | LCD_OE_EM_CS3n_GP[13] | |
| 69 | GROUND | | 70 | GROUND | |
| 71 | EM_A[5]_GP[96] | | 72 | EM_A[9]_GP[92] | |
| 73 | EM_A[6]_GP[95] | | 74 | EM_A[10]_GP[91] | |
| 75 | EM_A[7]_GP[94] | | 76 | EM_A[11]_GP[90] | |
| 77 | EM_A[8]_GP[93] | | 78 | EM_A[12]_GP[89] | |
| 79 | EM_WEn | | 80 | EM_OEn | |
| 81 | GROUND | | 82 | GROUND | |
| 83 | MEM_EMD7-7_ENABLEn | | 84 | CLK_OUT_PWM2_GP[84] | |
| 85 | CI_EMA_ENABLEn | | 86 | GROUND | |
| 87 | RESETn | | 88 | GP[4]_PWM1 | |
| 89 | SYS_RESETn | | 90 | I2C_INT_ENABLEn | |
| 91 | VCC_1V8 | | 92 | VCC_1V8 | |
| 93 | GROUND | | 94 | GROUND | |
| 95 | VCC_3V3 | | 96 | VCC_3V3 | |
| 97 | GROUND | | 98 | GROUND | |
| 99 | VCC_5V | | 100 | VCC_5V | |

3.2.22 DC_P2, Peripheral Expansion

Table 15: DC_P2, Peripheral Expansion

| Pin | Signal | Conn | Pin | Signal | Conn |
|-----|-----------------------------|------|-----|-----------------------------|------|
| 1 | GROUND | | 2 | GROUND | |
| 3 | VCC_5V | | 4 | VCC_5V | |
| 5 | VCC_3V3 | | 6 | VCC_3V3 | |
| 7 | VIC_TINPOL_ENABLEn | | 8 | GROUND | |
| 9 | CLKS1_TINPOL_GP[98] | | 10 | CLKS0_TINPOL_GP[97] | |
| 11 | GP[00] | | 12 | GP[01] | |
| 13 | GP[02] | | 14 | GP[03] | |
| 15 | RS232_ENABLEn | | 16 | GROUND | |
| 17 | URXD0_GP[85] | | 18 | URTS0_PWM0_GP[88] | |
| 19 | UTXD0_GP[86] | | 20 | UCTS0_GP[87] | |
| 21 | GROUND | | 22 | GROUND | |
| 23 | HECC_RX_TINP1L_URXD1_GP[56] | | 24 | HECC_tX_TOUT1L_UTXD1_GP[55] | |
| 25 | GROUND | | 26 | CAN_ENABLEn | |
| 27 | AUDIO_CLK | | 28 | GROUND | |
| 29 | AXR0[3]_FSR0_GP[102] | | 30 | AXR0[2]_FSX0_GP[103] | |
| 31 | AFSR0_DR0_GP[100] | | 32 | AXR0[1]_DX0_GP[104] | |
| 33 | AHCLKR0_CLKR0_GP[101] | | 34 | ACLKR0_CLKX0_GP[99] | |
| 35 | GROUND | | 36 | GROUND | |
| 37 | I2C_CLK | | 38 | I2C_DATA | |
| 39 | AIC33_ENABLEn | | 40 | GROUND | |
| 41 | AXR0_FSR1_GP[106] | | 42 | AMUTEIN0_FSX1_GP[109] | |
| 43 | AMUTE0_DR1_GP[110] | | 44 | ACHLKX0_CLKR1_GP[108] | |
| 45 | ACLKX0_CLKX1_GP[106] | | 46 | AFSX0_DX1_GP[107] | |
| 47 | GROUND | | 48 | GROUND | |
| 49 | RESET_OUTn | | 50 | SPARE | |
| 51 | SPARE | | 52 | HCNTL0_MRXER_GP[76] | |
| 53 | HDS1n_RXD1_GP[79] | | 54 | HDS2n_RXD0_GP[78] | |
| 55 | HINTn_RXD3_GP[82] | | 56 | HRDYn_RXD2_GP[80] | |
| 57 | GROUND | | 58 | HD09_COL_GP[67] | |
| 59 | HHWIL_RXDV_GP[74] | | 60 | GROUND | |
| 61 | HD10_CRS_GP[68] | | 62 | HRNW_RXCLK_GP[77] | |
| 63 | GROUND | | 64 | GROUND | |
| 65 | HCSnMDC_GP[81] | | 66 | HASn_MDIO_GP[83] | |
| 67 | GROUND | | 68 | GROUND | |
| 69 | HD11_TXD3_GP[69] | | 70 | HD12_TXD2_GP[70] | |
| 71 | HD13_TXD1_GP[71] | | 72 | HD14_TXD0_GP[72] | |
| 73 | HCNTL1_TXEN_GP[75] | | 74 | ENET_ENABLEn | |
| 75 | GROUND | | 76 | GROUND | |
| 77 | SPARE | | 78 | HD15_TXCLK_GP[73] | |
| 79 | GROUND | | 80 | GROUND | |
| 81 | USER_I2C_IO.A0P6 | | 82 | USER_I2C_IO.A0P7 | |
| 83 | SPARE | | 84 | SPARE | |
| 85 | USER_I2C_IO.A1P2 | | 86 | USER_I2C_IO.A1P3 | |
| 87 | USER_I2C_IO.A1P0 | | 88 | USER_I2C_IO.A1P1 | |
| 89 | GROUND | | 90 | GROUND | |

3.2.23 DC_P3, VLYNQ Connector

The DC_P3 connector allows the user to connect the VLYNQ interface to other logic. The pinout for the DC_P3 connector is shown in the table below.

Table 16: DC_P3, VLYNQ Header

| Pin # | Signal | Conn | Pin # | Signal | Conn |
|-------|-------------------------|------|-------|------------------------|------|
| 1 | HD00_VLYNQ_SCRUN_GP[58] | | 2 | VLYNQ_CLOCK_GP[57] | |
| 3 | GROUND | | 4 | GROUND | |
| 5 | HD01_VLYNQ_RXD0_GP[59] | | 6 | HD05_VLYNQ_TXD0_GP[63] | |
| 7 | HD02_VLYNQ_RXD1_GP[60] | | 8 | HD06_VLYNQ_TXD1_GP[64] | |
| 9 | GROUND | | 10 | GROUND | |
| 11 | VCC_3V3 | | 12 | DC_P3_VLYNQ_RESETn | |
| 13 | HD03_VLYNQ_RXD2_GP[61] | | 14 | HD07_VLYNQ_TXD2_GP[65] | |
| 15 | HD04_VLYNQ_RXD3_GP[62] | | 16 | HD08_VLYNQ_TXD3_GP[66] | |
| 17 | GROUND | | 18 | GROUND | |
| 19 | VCC_5V | | 20 | VCC_5V | |

3.3 Jumpers

The DM6437 EVM has four (4) jumpers which are used to make certain logic or feature determinations on the board. The function of each jumper is described in the table below.

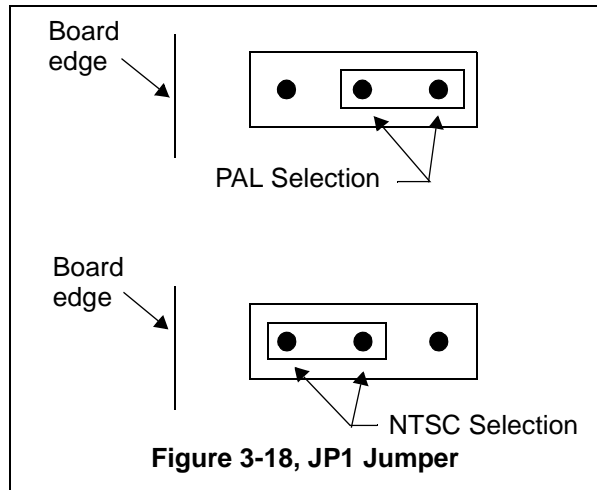
Table 17: Jumpers

| Jumper # | Function | Size |
|----------|-----------------|------|
| JP1 | NTSC/PAL Select | 1x3 |
| JP2 | CS2 Select | 2x4 |
| JP3 * | Reset | 1x2 |
| JP4 * | Power Up Reset | 1x2 |

* Not populated

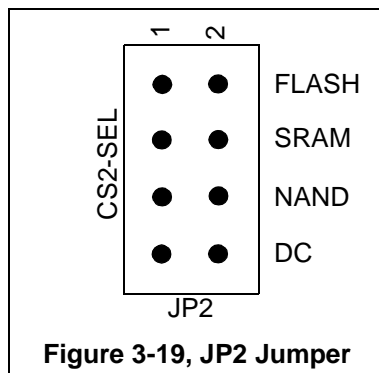
3.3.1 JP1 Jumper

Jumper JP1 is used to select the display output format, NTSC or PAL. This jumper **must** be populated in one of the two configurations. When the center to NTSC is selected the display output will be NTSC format. When the center to PAL is selected the display output will be in PAL format. These positions are shown in the figure below.



3.3.2 JP2 Jumper

Jumper JP2 is a jumper bank used to select the routing of the CS2 signal. It can be routed to Flash ROM, SRAM, NAND Flash, and daughter card connector. Only one of these 1-2 selections should be made. The positions are shown in the figure below.



3.3.3 JP3 Jumper

Jumper JP3 is a jumper used to allow external switches to interface to the DM6437 power up reset signal.

3.3.4 JP4 Jumper

Jumper JP4 is a jumper used to allow external switches to interface to the DM6437 reset signal.

3.4 LEDs

The DM6437 EVM has eight (8) LEDs. Four of these LEDs (DS1-4) are under user control and addressed over the I²C bus. LED DS5 indicates the presence of +5 volts on the board. The remaining LEDs, DS501 and DS502 indicate embedded USB status. DS502 is on when embedded USB emulation is selected and off when the external JTAG emulator is plugged into connector J6. DS501 blinks as packets are sent to and from the embedded USB emulator. The LED functions are summarized in the table below.

Table 18: LEDs

| LED # | Use | Color |
|-------|---------------------------|-------|
| DS1 | User Defined | Green |
| DS2 | User Defined | Green |
| DS3 | User Defined | Green |
| DS4 | User Defined | Green |
| DS5 | +5V present | Red |
| DS501 | Embedded Emulation Status | Green |
| DS502 | Embedded/external EMU | Green |

3.5 Switches

The DM6437 EVM has seven (7) switches. These switches are used to create certain actions on the board or to select certain functions on the board. The switch functions are summarized in the table below.

Table 19: Switches

| SW # | Function |
|------|-----------------------------|
| SW1 | Bootload Mode Select |
| SW2 | DM6437 Muxing Configuration |
| SW3 | EMIF Data Select |
| SW4 | 4 position user readable |
| SW5 | Power On Reset |
| SW6 | Reset |
| SW7 | Slide Switch |

3.5.1 SW1, Bootload Mode Select

Switch SW1 is an 8 position switch used to select the source of the bootload. Five (5) of the eight (8) positions are used. The selections are shown in the table below.

Table 20: SW1, Bootload Mode Select

| SW1[4:1] | SW1[5] | Auto Detected | Boot Description | Notes | DSPBOOTADDR default |
|----------|--------|---------------|--|------------------|---------------------|
| 0000 | x | x | Emulation Boot In this mode, FASTBOOT setting is don't care (not used by bootloader code) | DM6437 is master | 0x0010 0000 |
| 0001 | 1* | 0 | HPI Boot | DM6437 is slave | 0x0010 0000 |
| 0001 | 1* | 1 | PCI Boot without auto-initialization | DM6437 is slave | 0x0010 0000 |
| 0010 | 1* | 0 | PCI Boot with auto-initialization | DM6437 is slave | 0x0010 0000 |
| 0010 | 1* | 1 | HPI Boot | DM6437 is slave | 0x0010 0000 |
| 0100 | 0 | x | EMIFA ROM Direct Boot | DM6437 is master | 0x4200 0000 |
| 0100 | 1 | x | EMIFA ROM Fast Boot | DM6437 is master | 0x0010 0000 |
| 0101 | x | x | I2C Boot | DM6437 is master | 0x0010 0000 |
| 0110 | 1* | x | SPI Boot (McBSP peripheral) | DM6437 is master | 0x0010 0000 |
| 0111 | 1* | x | NAND Flash | DM6437 is master | 0x0010 0000 |
| 1000 | x | x | UART | DM6437 is master | 0x0010 0000 |
| 1011 | x | x | EMAC Boot through secondary bootloader | DM6437 is slave | 0x0010 0000 |

x = don't care, * these boot modes must be accompanied with FASTBOOT = 1.

3.5.2 SW2, Bootload Configuration Select

Switch SW2 is an 4 position switch used to select the DM6437 multiplexing options at reset. The selection are shown in the table below.

Table 21: SW2, Bootload Configuration Select

| Position | Function | Description |
|----------|----------|------------------------------|
| 1 | AEM2 | Specifies EMIF mode at reset |
| 2 | AEM1 | Specifies EMIF mode at reset |
| 3 | AEM0 | Specifies EMIF mode at reset |
| 4 | AEAW2 | Specifies EMIF mode at reset |

3.5.3 SW3, EMIF Data Select

Switch SW3 is used to select between data bus pins for the asynchronous EMIF controller. The functions of this switch are shown in the table below.

Table 22: SW3, EMDATA Select

| Position | Function | Description |
|----------|-------------------|--|
| 1 | Not used | Not Used |
| 2 | MEM_EMD7-0_SELECT | 0=Selects C10-7 as EMIF data bus D0:D7 pins 1=Selects C10-7 as COUT data bus D0:D7 pins |

3.5.4 SW4, 4 Position User Readable

Switch SW4 is a 4 position bank of user readable switches via the I²C expander. The individual switches can be placed in any position and read by the user software from the expander. See the section on I²C expanders for more information.

3.5.5 SW5, Power On Reset Switch

Switch SW5 is a momentary switch that asserts power on reset to the DM6437 device.

3.5.6 SW6, Reset Switch

Switch SW6 is a momentary switch that asserts a reset to the DM6437 processor.

3.5.7 SW7, Slide Switch

Switch SW7 is a 2 position slide switch used by demonstration software. The switch is read via a I²C expander. Refer to the I²C section for more information.

3.6 Test Points

The EVM has 51 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

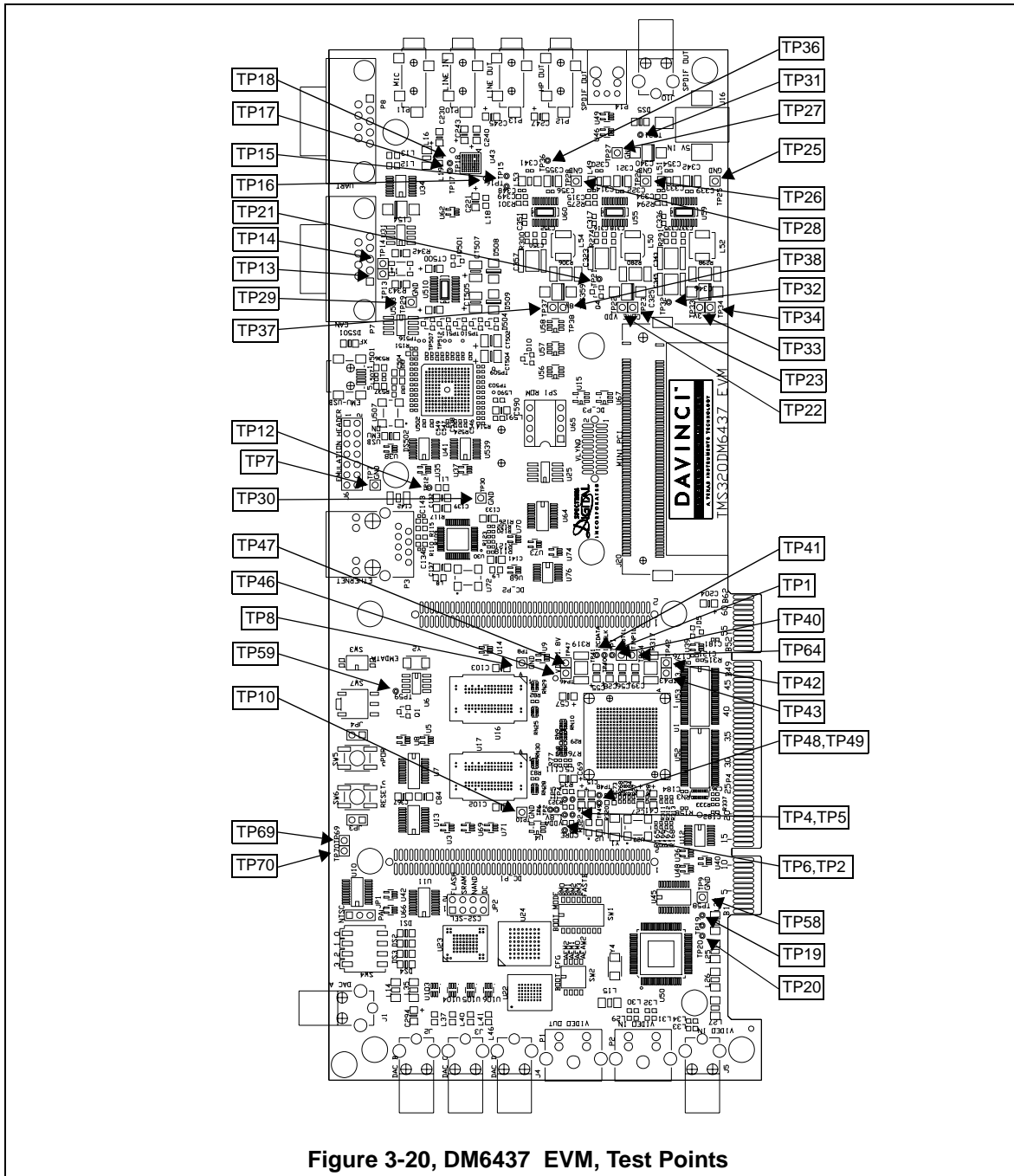


Figure 3-20, DM6437 EVM, Test Points

Table 23: DM6437 EVM Test Points

| Test Point # | Signal | Test Point # | Signal |
|--------------|-----------------------------|--------------|----------------------------|
| TP1 | RESETOUTn | TP27 | GND |
| TP2 | RSV4 | TP28 | GND |
| TP6 | RSV5 | TP29 | GND |
| TP7 | GND | TP30 | GND |
| TP8 | GND | TP31 | VCC_5V |
| TP10 | GND | TP32 | 3V3_PWR_OK |
| TP12 | Ethernet PHY Interrupt Pin | TP36 | 1V8_PWR_OK |
| TP13 | CAN Driver Output B_CANH | TP40 | DM6437 I2CCLK |
| TP14 | CAN Driver Output B_CANL | TP41 | DM6437 I2CDATA |
| TP15 | Codec MFP2 Pin | TP52 | VDD_1P1V |
| TP16 | Codec MPF3 Pin | TP53 | VDD_1P1V |
| TP17 | Codec GPIO1 Pin | TP58 | VIDEO DECODER GLCO/I2C Pin |
| TP18 | Codec GPIO2 Pin | TP59 | VIC INPUT CLOCK |
| TP19 | VIDEO DECODER AVID/GPIO Pin | TP61 | DM6437 HECC_RX |
| TP20 | VIDEO DECODER INTREQ Pin | TP64 | DM6437 HECC_TX |
| TP21 | CORE_PWR_OK | TP69 | DM6437 PWM1 |
| TP25 | GND | TP70 | DM6437CLK_OUT |
| TP26 | GND | | |

Table 24: Power Pair Test Points

| Power Pairs Input1 | Power Pairs Input2 | Power Domain | Resistance Between Inputs |
|--------------------|--------------------|--------------|---------------------------|
| TP4 | TP5 | DDR_VDDL | 0.1 ohms |
| TP22 | TP23 | DSP_CORE_VDD | 0.025 ohms |
| TP33 | TP34 | VCC_3V3 | 0.025 ohms |
| TP37 | TP38 | VCC_1V8 | 0.025 ohms |
| TP42 | TP43 | DVD_3V3 | 0.025 ohms |
| TP47 | TP46 | DVDD_1V8 | 0.025 ohms |
| TP48 | TP49 | PLL_PWR18 | 0.1 ohms |
| TP52 | TP53 | VDDA_1P1V | 0.1 ohms |
| TP54 | TP55 | VDDA_1P8V | 0.1 ohms |

Appendix A

Schematics

This appendix contains the schematics for the DM6437 EVM.

SCHMATIC CONTENTS

- SHEET01 - TITLE
- SHEET02 - BLOCK DIAGRAM
- SHEET03 - DSP CLKS/RST/EMU
- SHEET04 - EMULATION
- SHEET05 - DSP Serial/CAN/I2C
- SHEET06 - DSP VP/EMIF/PCI/ENET
- SHEET07 - DSP DDR Interface
- SHEET08 - DSP DACS/GND-pins
- SHEET09 - DSP Power Pins

- SHEET10 - Boot DIP Switches
- SHEET11 - VIC
- SHEET12 - I2C Expanders
- SHEET13 - I2C Expanders 2
- SHEET14 - DDR2 Memories
- SHEET15 - EMIF Muxing
- SHEET16 - NAND-Flash/SRAM
- SHEET17 - NOR-Flash/EEPROM
- SHEET18 - ENET Muxing
- SHEET19 - ENET

- SHEET20 - CAN
- SHEET21 - RS232
- SHEET22 - PCI-Mux
- SHEET23 - PCI-Mux II
- SHEET24 - PCI-Connector
- SHEET25 - VLYNQ
- SHEET26 - AIC33
- SHEET27 - SPDIF/TVP5146-Switch
- SHEET28 - TVP5146
- SHEET29 - Video Out

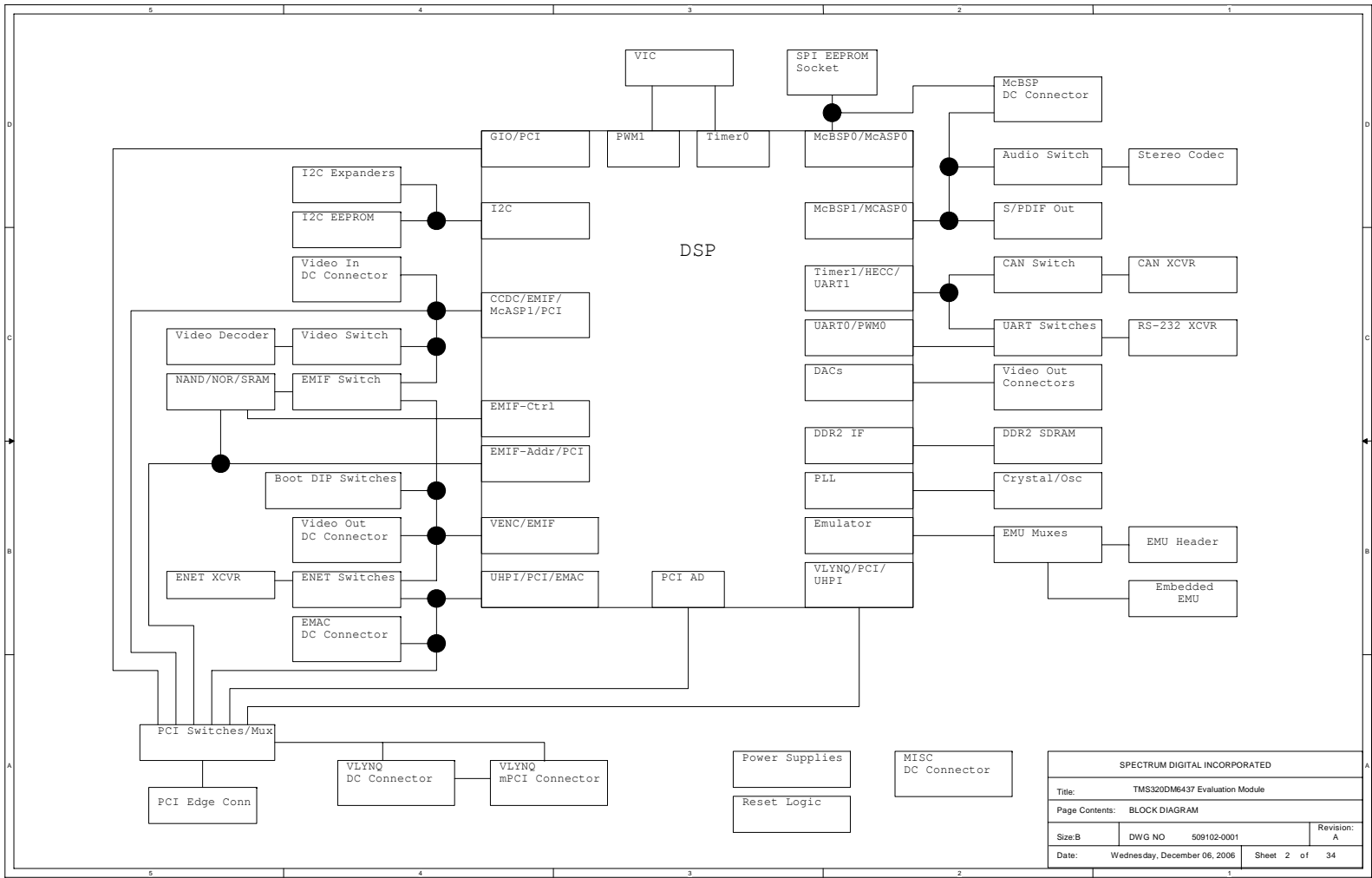
- SHEET30 - VIDEO DC Conn.
- SHEET31 - EMAC/MCBSP DC Conn.
- SHEET32 - VLYNQ/EMIF DC Conn.
- SHEET33 - RESET SUPERVISOR
- SHEET34 - POWER

| I2C Address Table | | | |
|-------------------|-----------|-----------|--|
| ADDRESS | | DEVICE | FUNCTION |
| HEX | BINARY | | |
| 0x38 | 00111000B | PCF8574 | USER INPUT Expander - 0111(A2)(A1)(A0) |
| 0x39 | 00111001B | PCF8574 | LED Expander - 0111(A2)(A1)(A0) |
| 0x3A | 00111010B | PCF8574 | VIC PLL Expander - 0111(A2)(A1)(A0) |
| 0x3B | 00111011B | PCF8574 | VLYNQ IO Expander - 0111(A2)(A1)(A0) |
| 0x50 | 01010000B | CAT24C256 | EEPROM - 1010(A2)(A1)(A0) |
| 0x1B | 00011011B | AIC33 | AUDIO CODEC - 00110(MFF1)(MFP0) |
| 0x5D | 01011101B | TVP5146 | VIDEO DECODER - 101110(I2CA) |

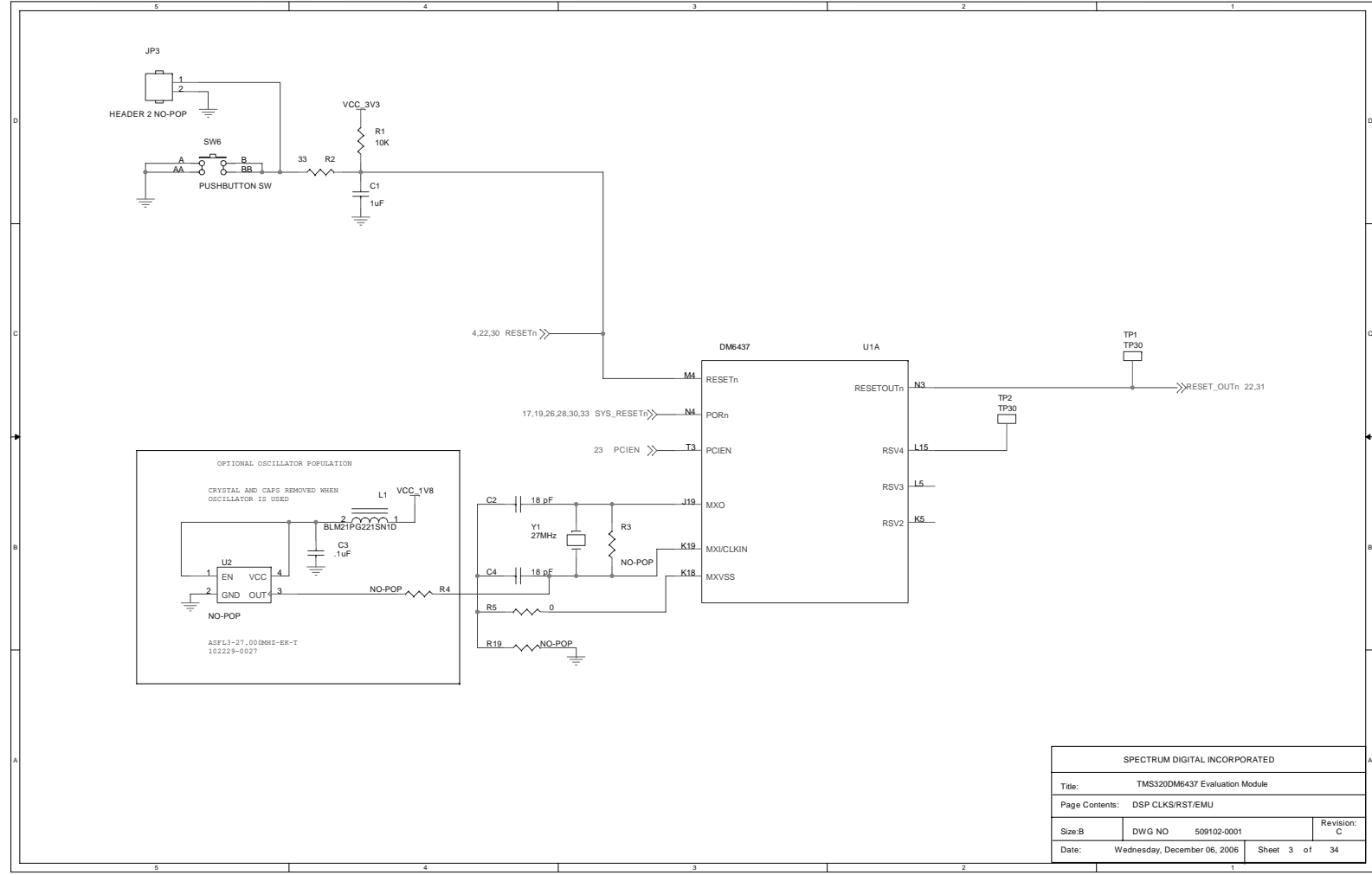
| REVISION STATUS OF SHEETS | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|
| REV | A | A | B | B | | | | | | |
| REV | 31 | 32 | 33 | 34 | | | | | | |
| SH | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
| REV | A | C | C | A | A | B | A | A | A | A |
| SH | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| REV | C | A | C | A | A | A | A | A | A | A |
| SH | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

| REV | R.R.P. | DATE |
|--------|--------|------------|
| DRK | R.R.P. | 06/01/2006 |
| T.W.R. | T.W.R. | 06/01/2006 |
| R.R.P. | R.R.P. | 06/01/2006 |
| R.R.P. | R.R.P. | 06/01/2006 |
| C.M.D. | C.M.D. | 06/01/2006 |
| R.R.P. | R.R.P. | 06/01/2006 |
| R.R.P. | R.R.P. | 06/01/2006 |

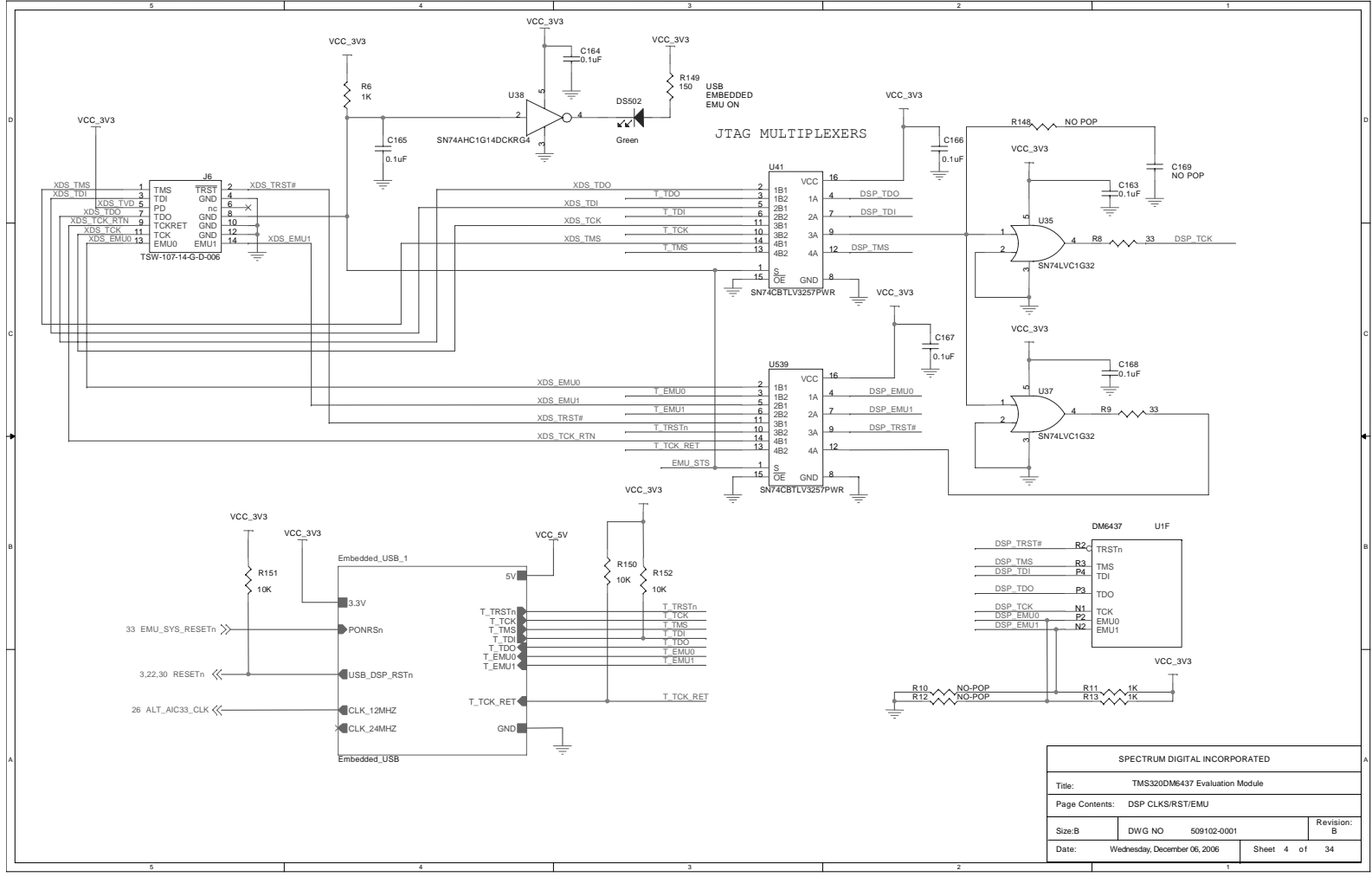
| SPECTRUM DIGITAL INCORPORATED | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: TITLE SHEET | | | |
| Size: B | DWG NO | 509102-0001 | Revision: C |
| Date: | Wednesday, December 06, 2006 | Sheet | 1 of 34 |



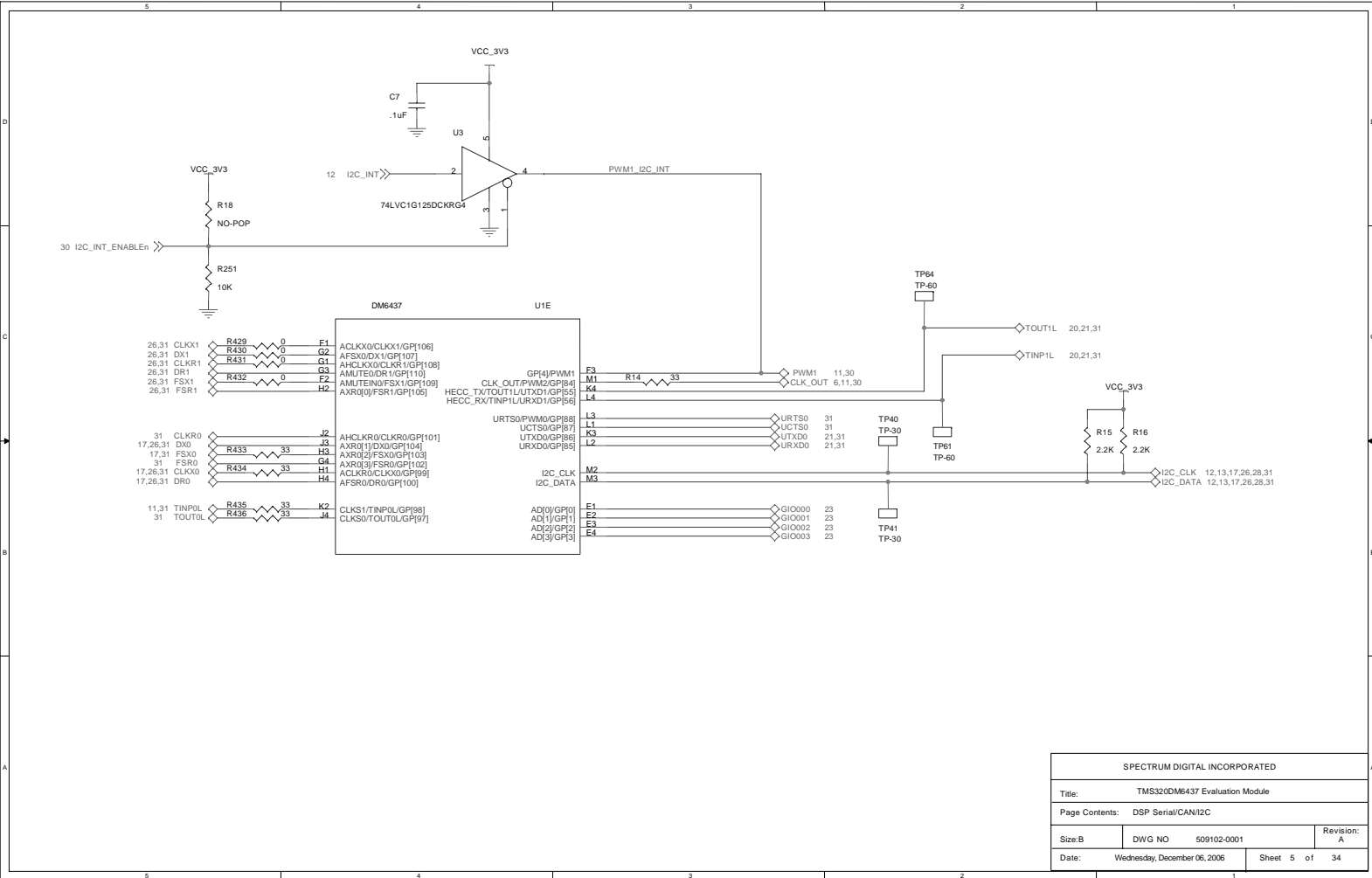
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: BLOCK DIAGRAM | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 2 of | 34 |



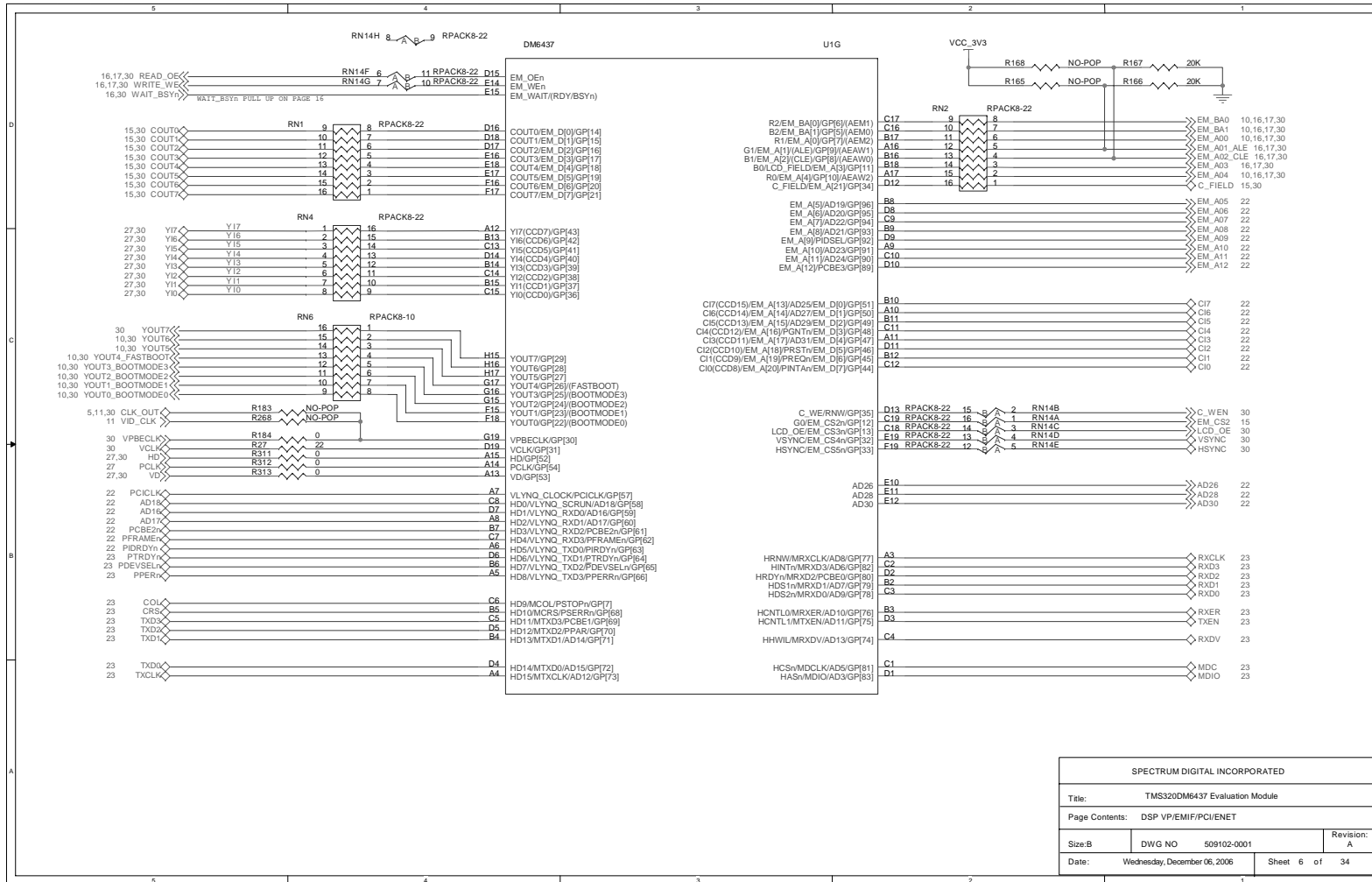
| | | | |
|---------------------------------------|------------------------------|---------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP CLKs/RST/EMU | | | |
| Size: B | DWG NO | 509102-0001 | Revision: C |
| Date: | Wednesday, December 06, 2006 | Sheet 3 of 34 | |



| | | | |
|---------------------------------------|------------------------------|---------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP CLKs/RST/EMU | | | |
| Size: B | DWG NO | 509102-0001 | Revision: B |
| Date: | Wednesday, December 06, 2006 | Sheet 4 of 34 | |

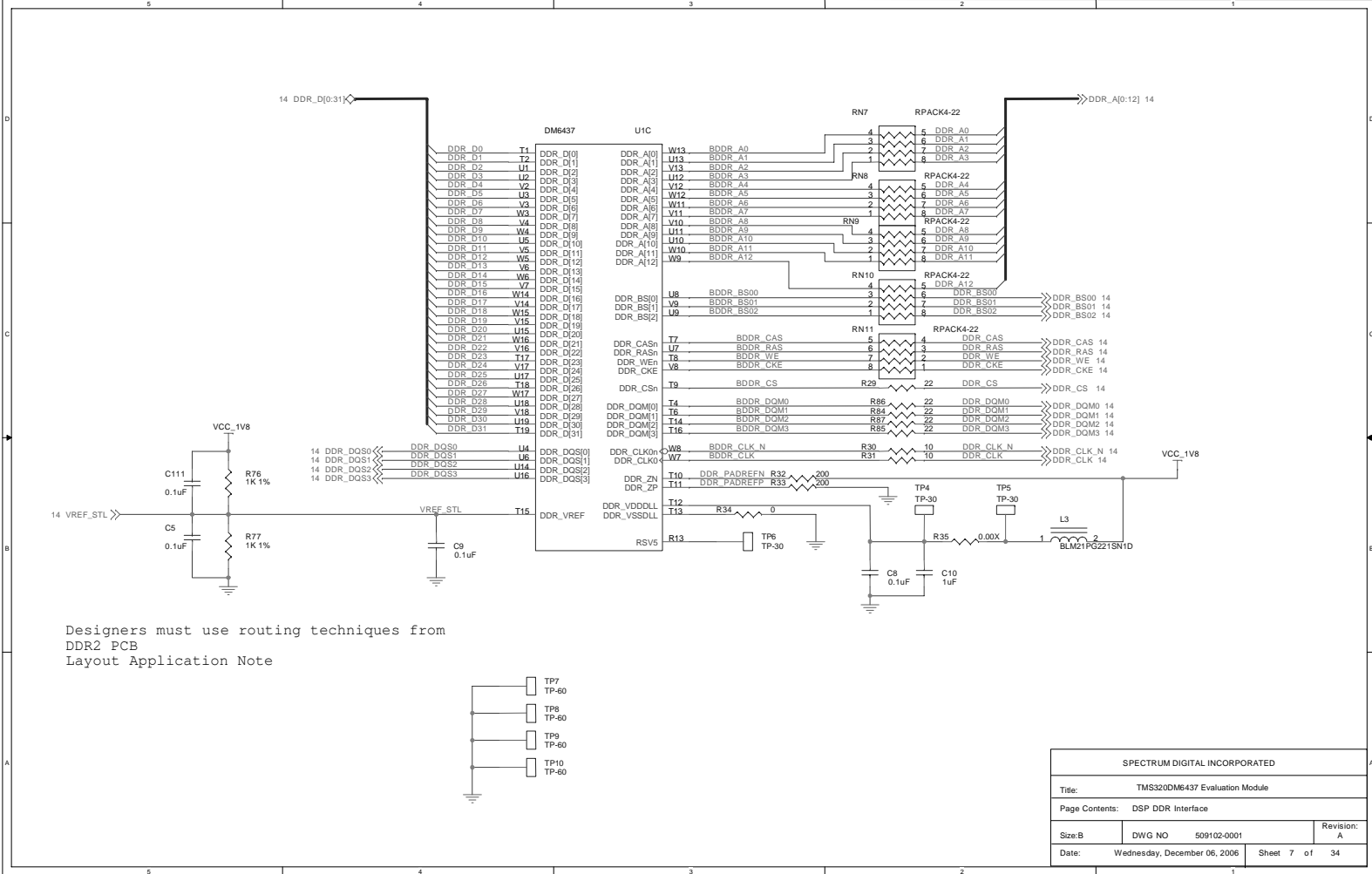


| | | | |
|---------------------------------------|------------------------------|-------------|---------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP Serial/CAN/I2C | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | | Sheet 5 of 34 |

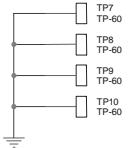


| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP VP/EMIF/PCI/ENET | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet | 6 of 34 |

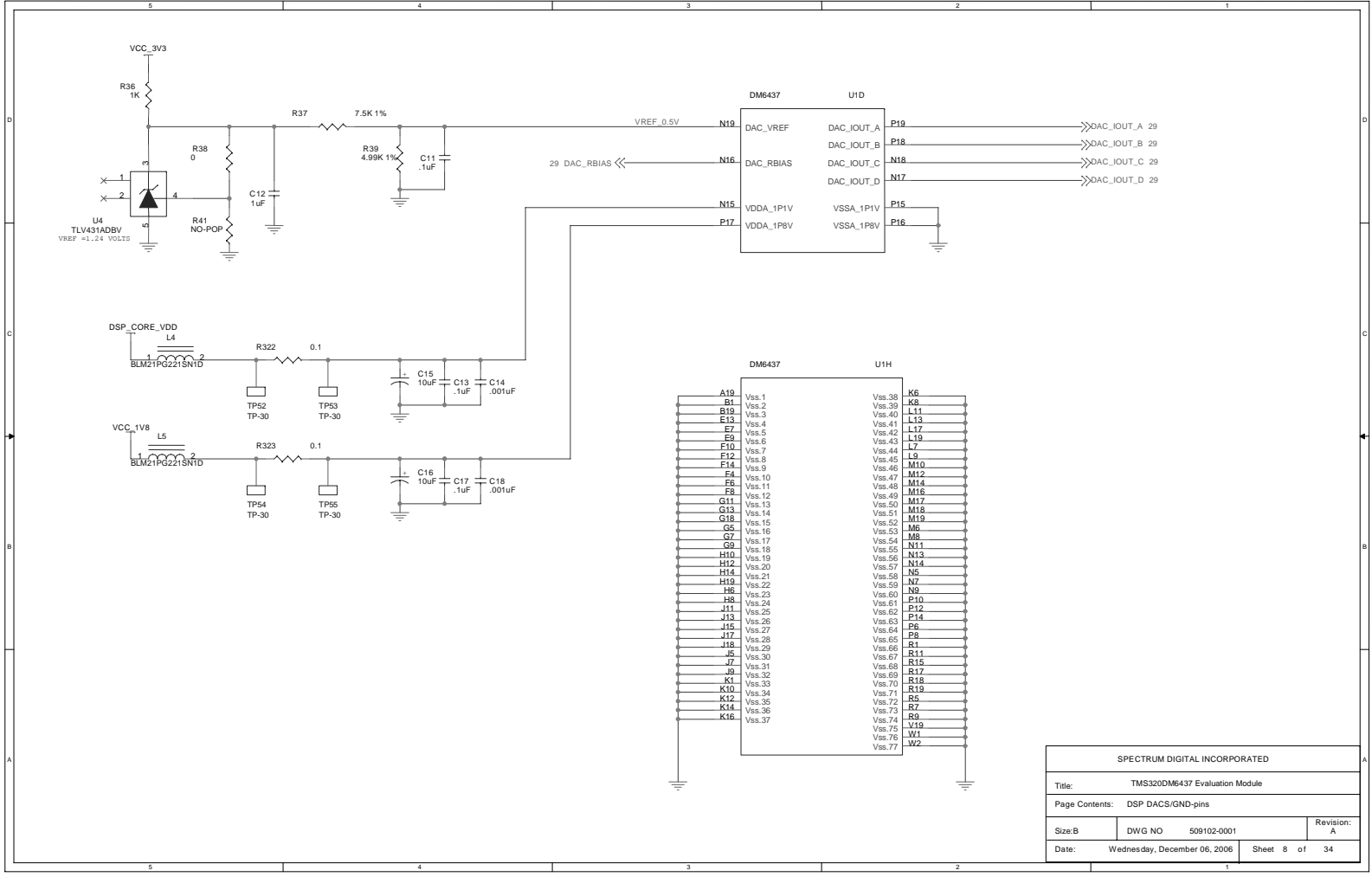
Spectrum Digital, Inc



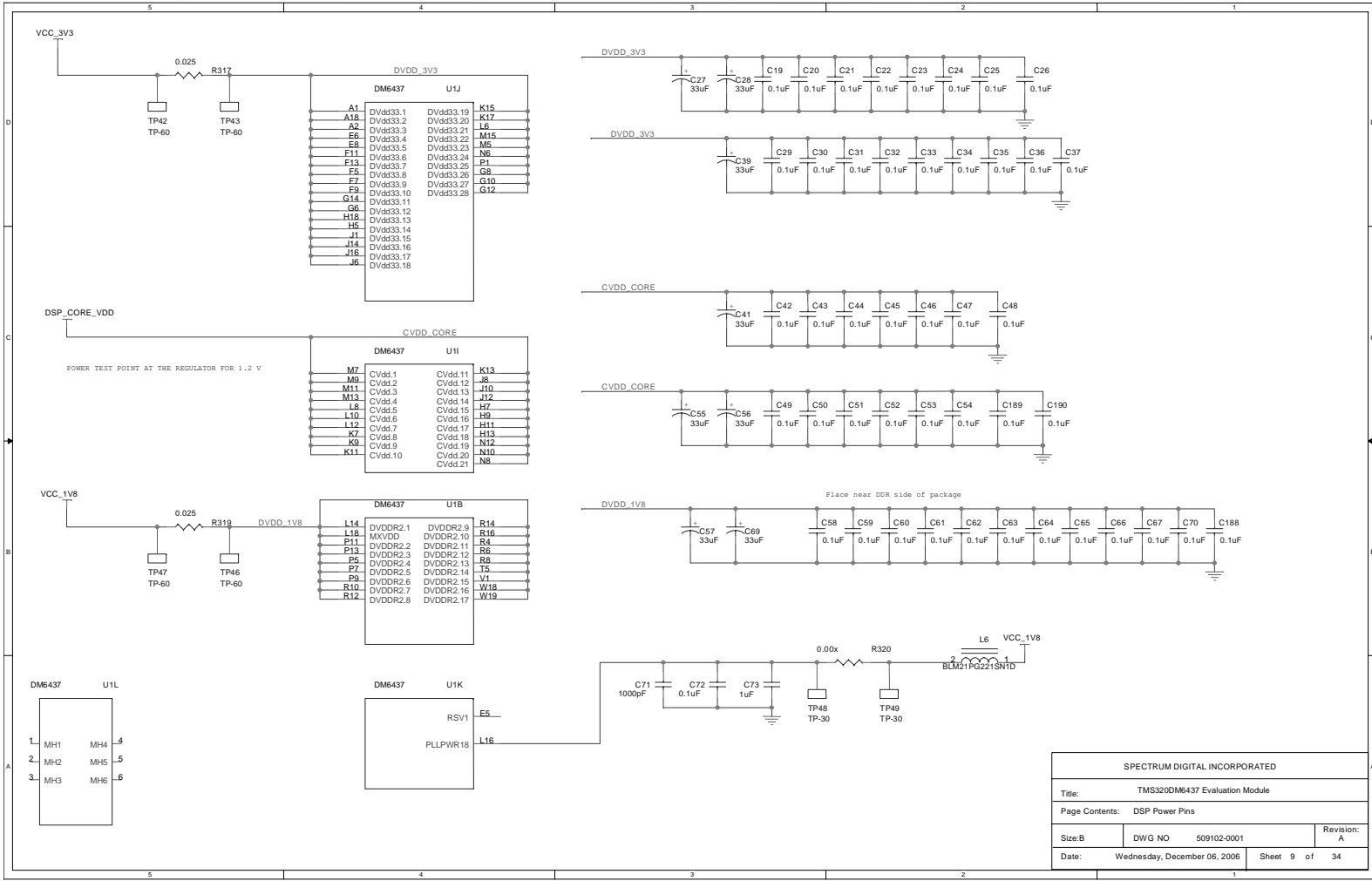
Designers must use routing techniques from
DDR2 PCB
Layout Application Note



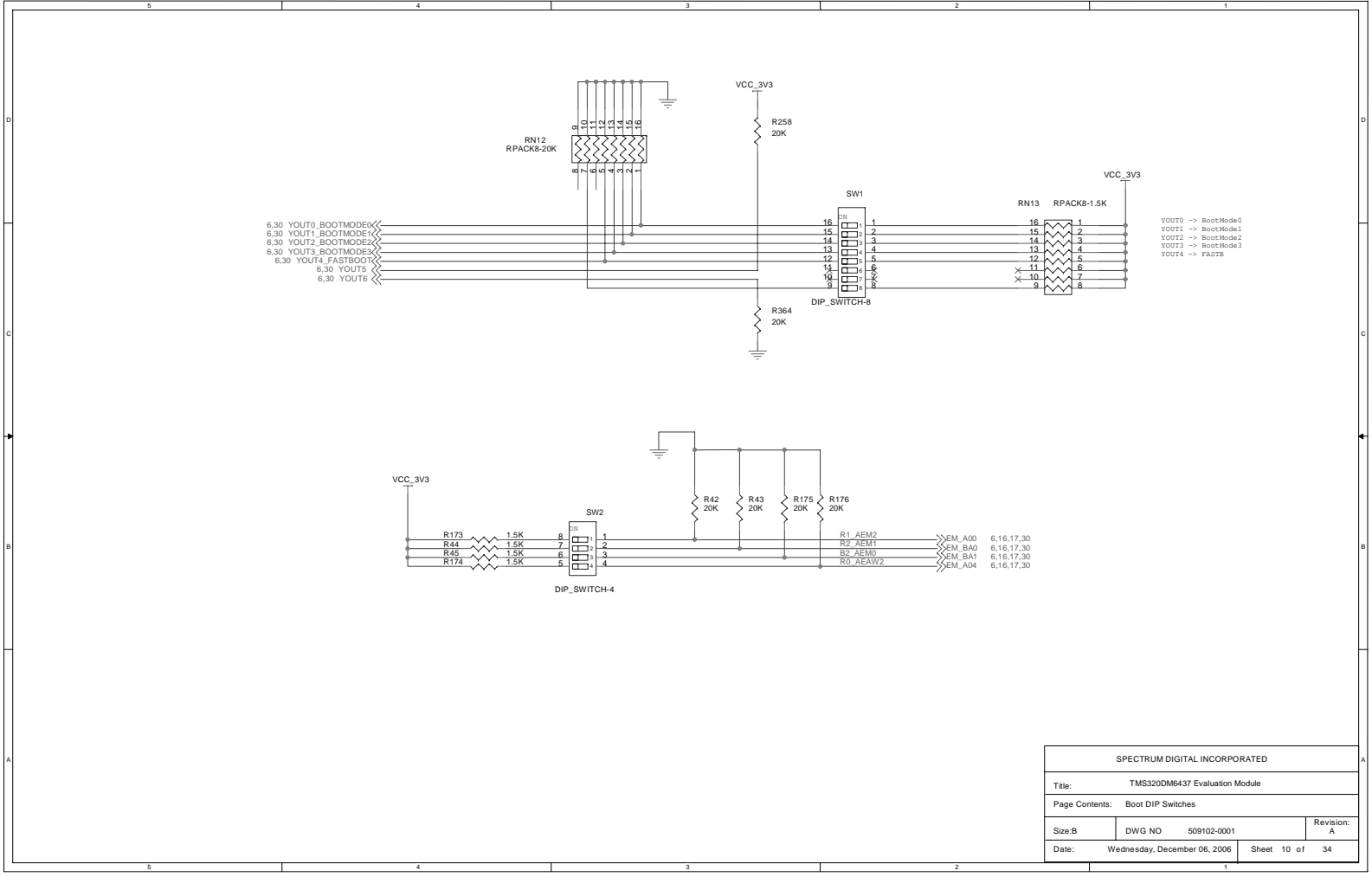
| SPECTRUM DIGITAL INCORPORATED | | | |
|---------------------------------------|------------------------------|---------------|-------------|
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP DDR Interface | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 7 of 34 | |



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|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP DACS/GND-pins | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 8 of | 34 |

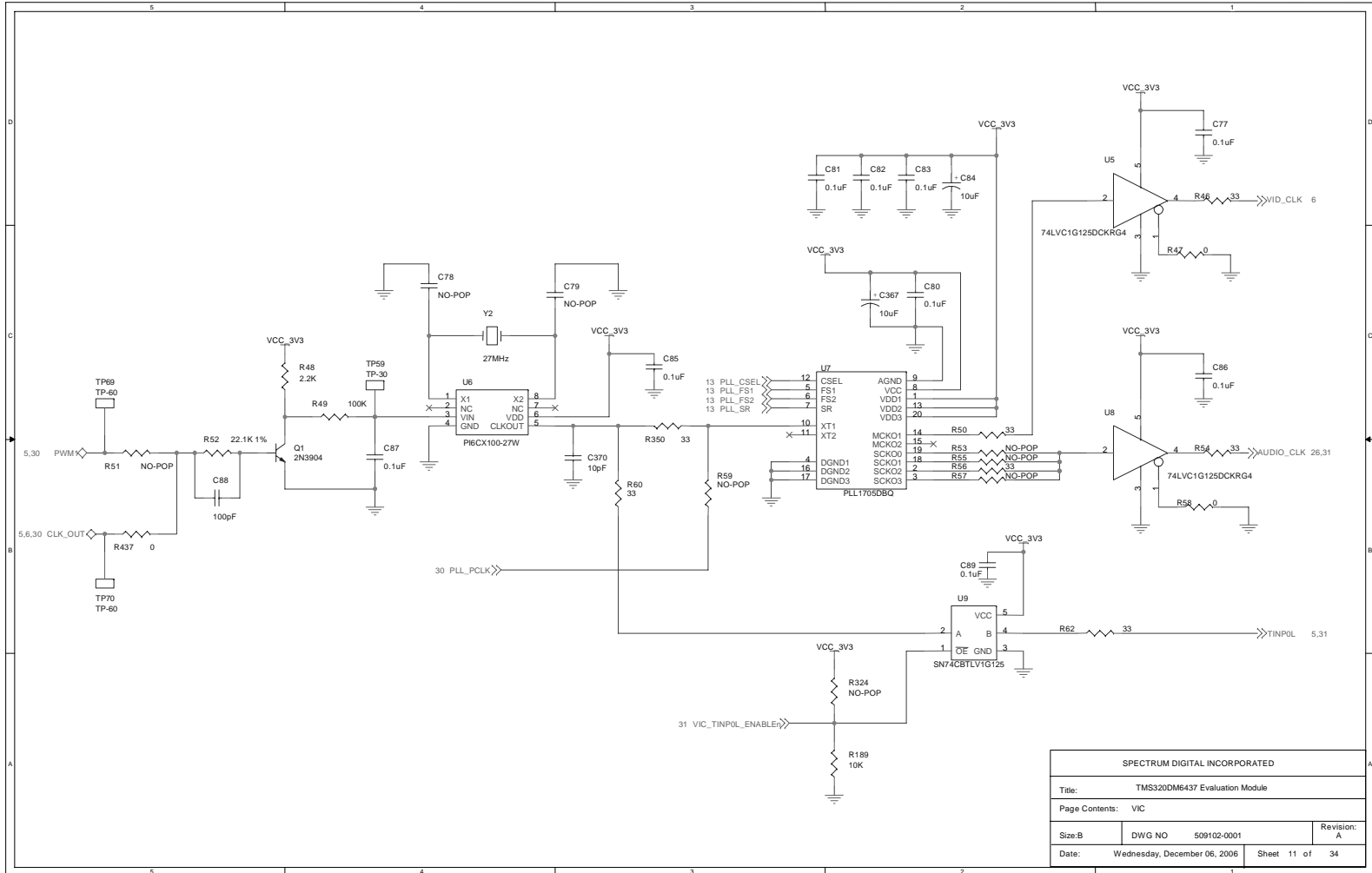


| SPECTRUM DIGITAL INCORPORATED | | | |
|---------------------------------------|---------------------|-------------|--|
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DSP Power Pins | | | |
| Size: B | DWG NO: 509102-0001 | Revision: A | |
| Date: Wednesday, December 06, 2006 | Sheet 9 of 34 | | |

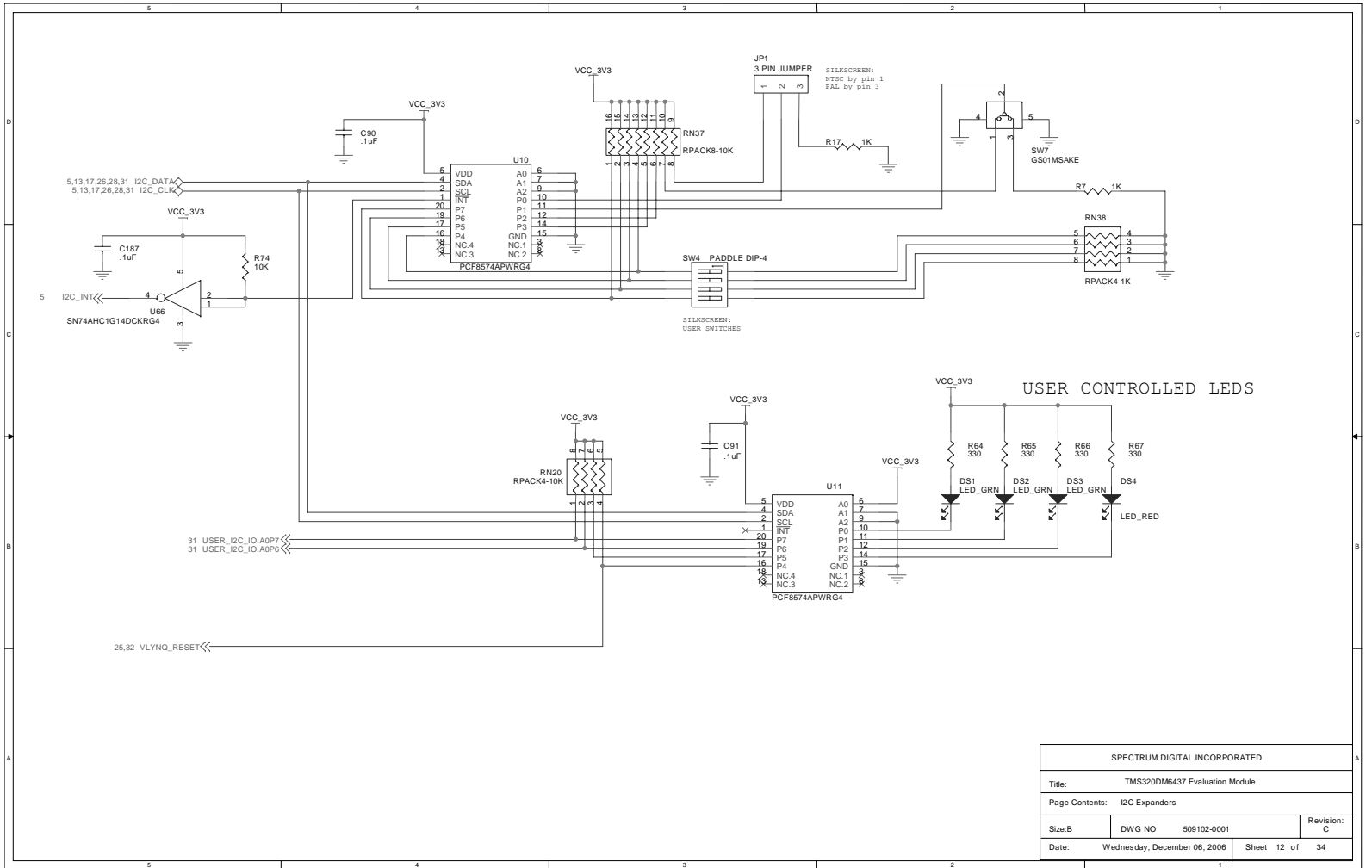


YOUT0 -> BootMode0
 YOUT1 -> BootMode1
 YOUT2 -> BootMode2
 YOUT3 -> BootMode3
 YOUT4 -> FASTB

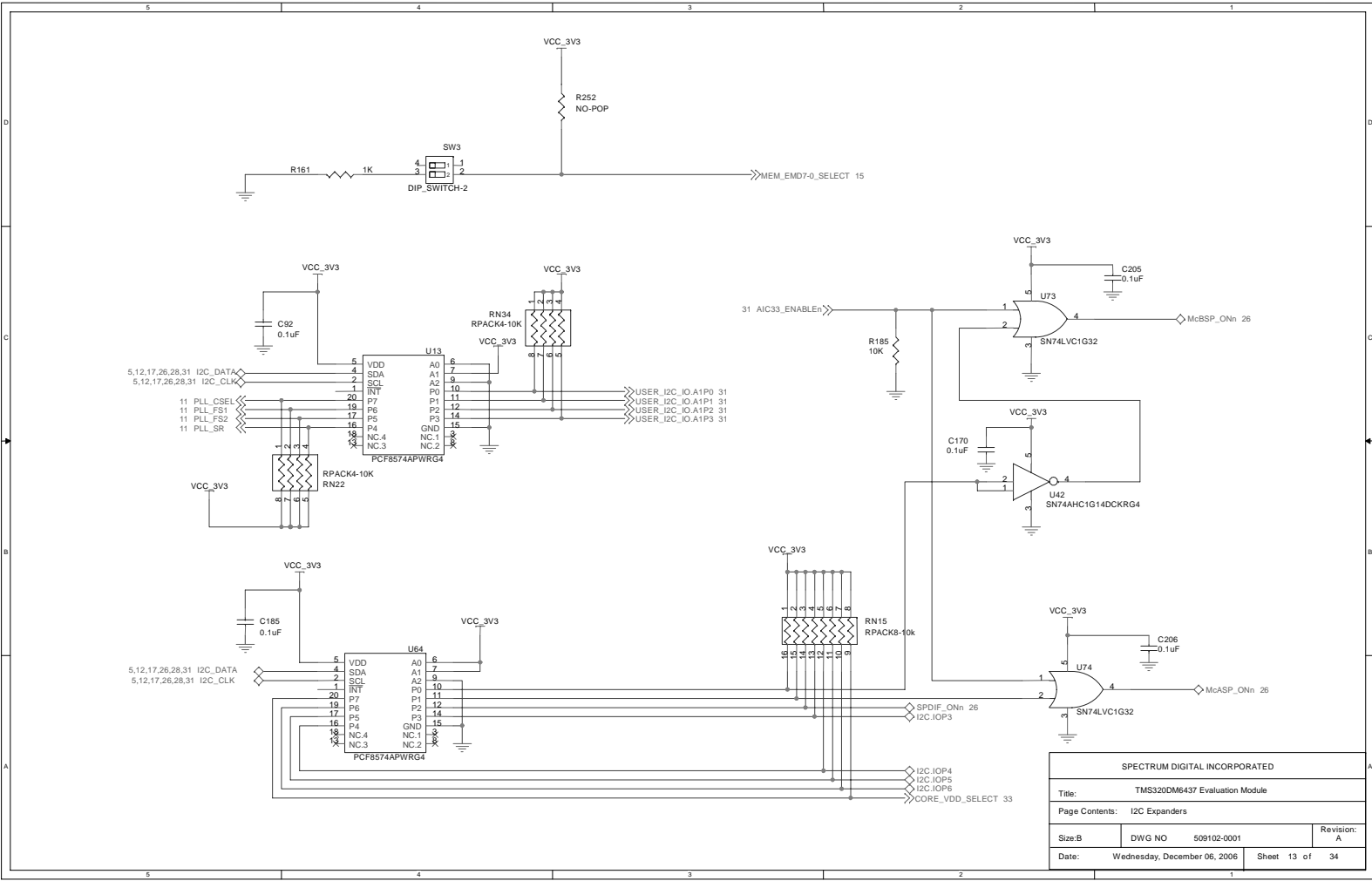
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Comments: Boot DIP Switches | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet | 10 of 34 |



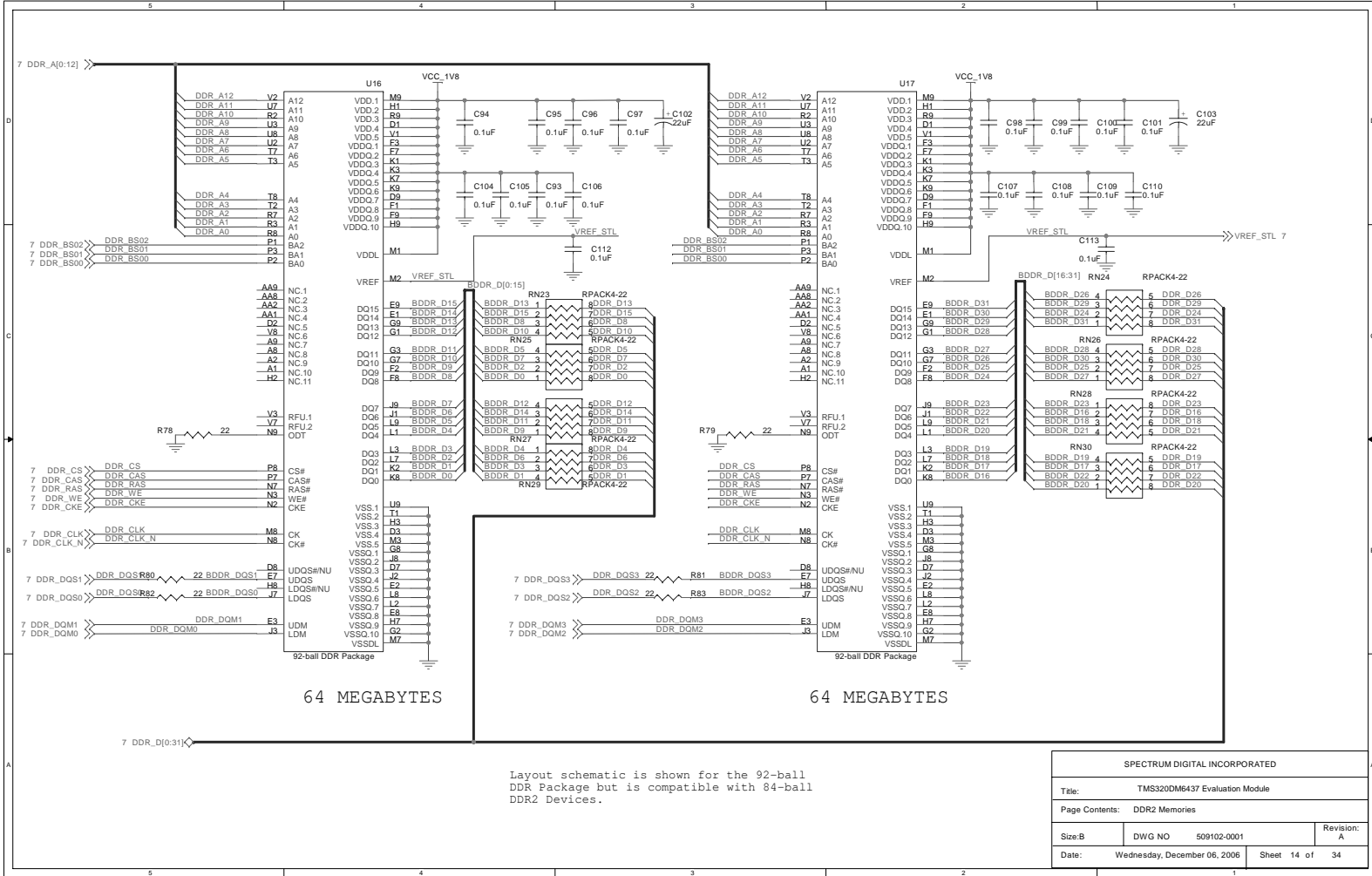
| | | | |
|---------------------------------------|------------------------------|----------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: VIC | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 11 of 34 | |



| | | | |
|---------------------------------------|------------------------------|----------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: I2C Expanders | | | |
| Size: B | DWG NO | 509102-0001 | Revision: C |
| Date: | Wednesday, December 06, 2006 | Sheet 12 of 34 | |



| | | | |
|---------------------------------------|---------------------|-------------|--|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: I2C Expanders | | | |
| Size: B | DWG NO: 509102-0001 | Revision: A | |
| Date: Wednesday, December 06, 2006 | Sheet 13 of 34 | | |

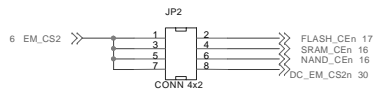
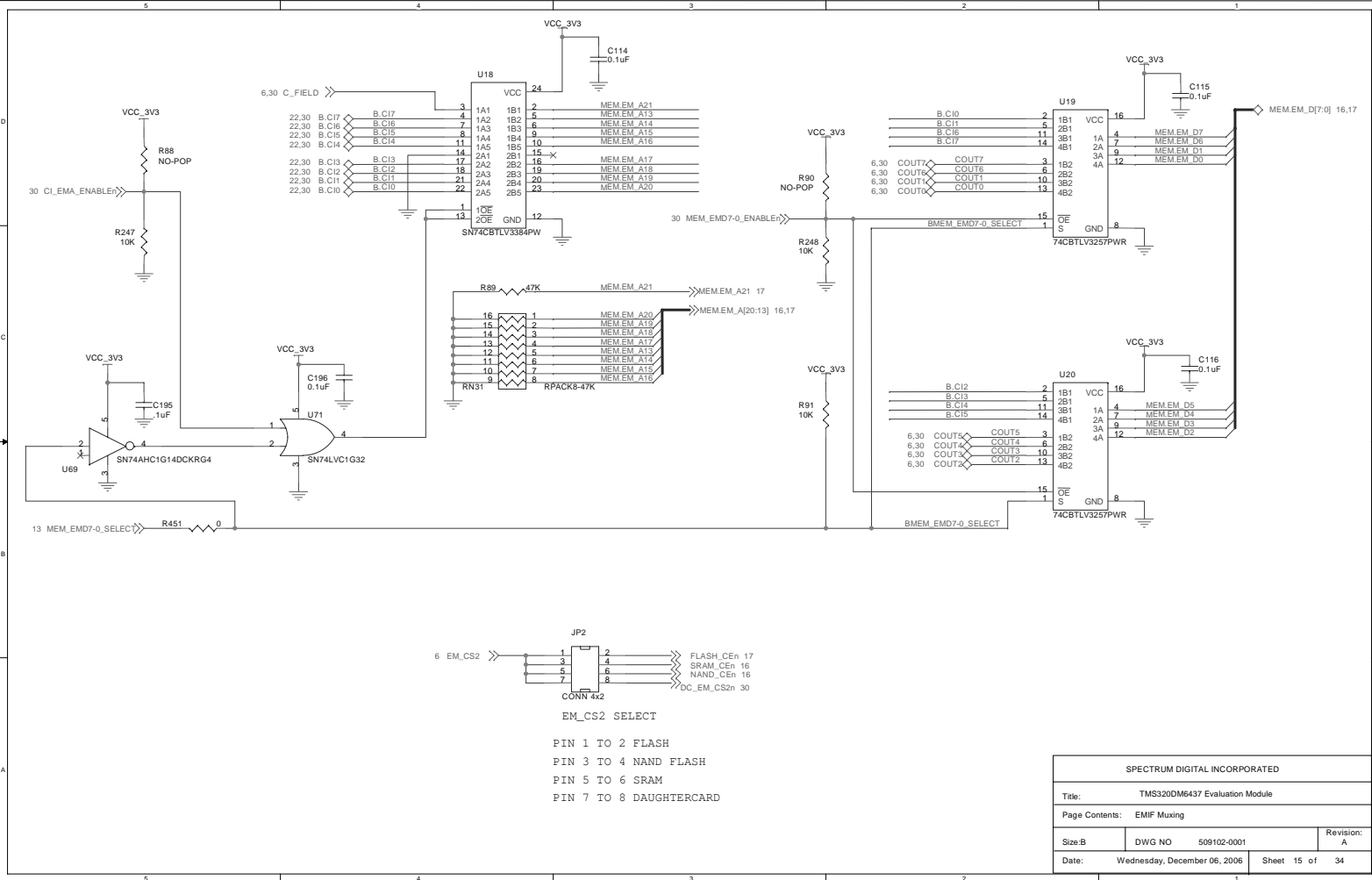


64 MEGABYTES

64 MEGABYTES

Layout schematic is shown for the 92-ball
 DDR Package but is compatible with 84-ball
 DDR2 Devices.

| | | | |
|---------------------------------------|--------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: DDR2 Memories | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: Wednesday, December 06, 2006 | Sheet | 14 of | 34 |



EM_CS2 SELECT

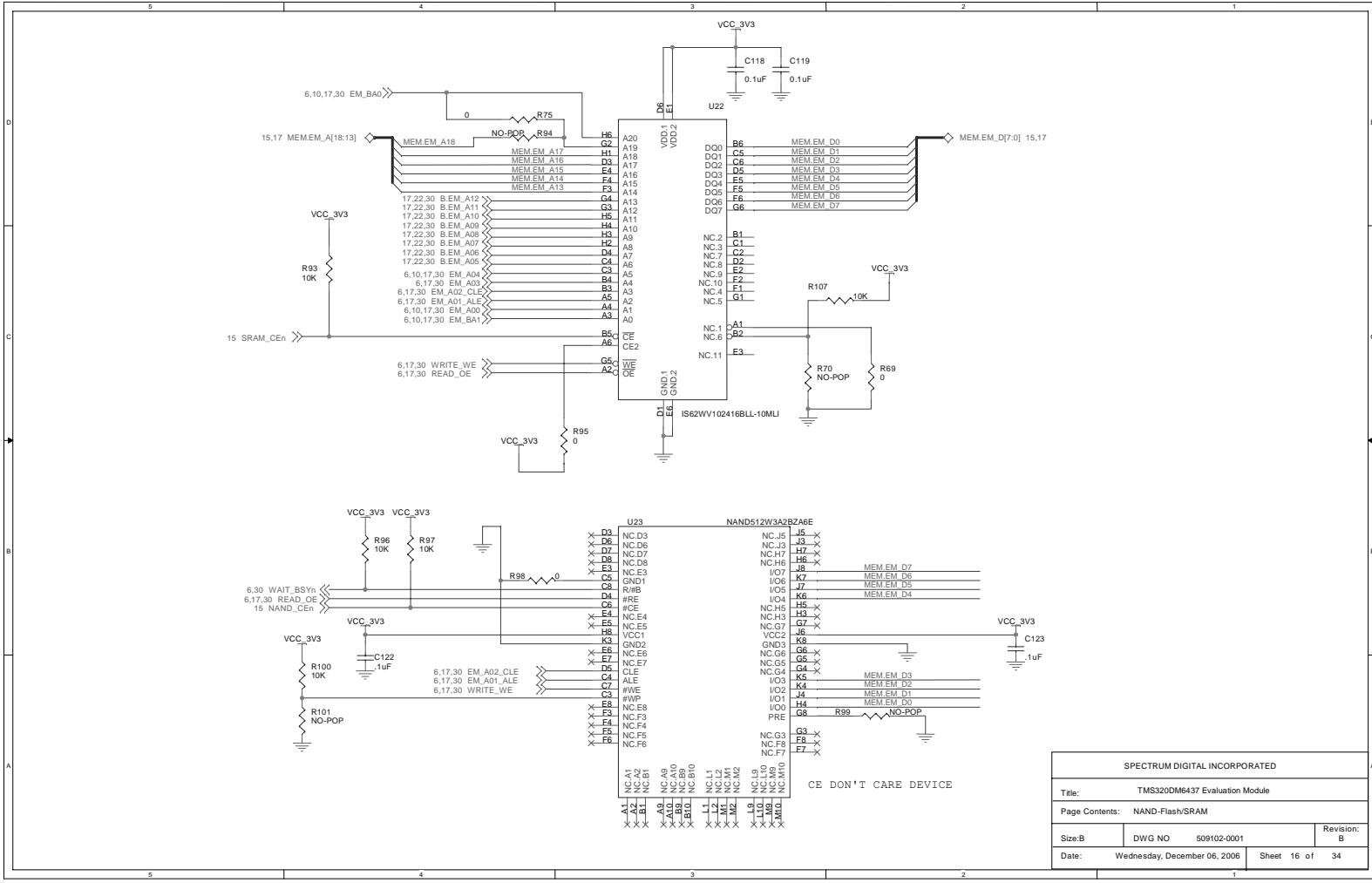
PIN 1 TO 2 FLASH

PIN 3 TO 4 NAND FLASH

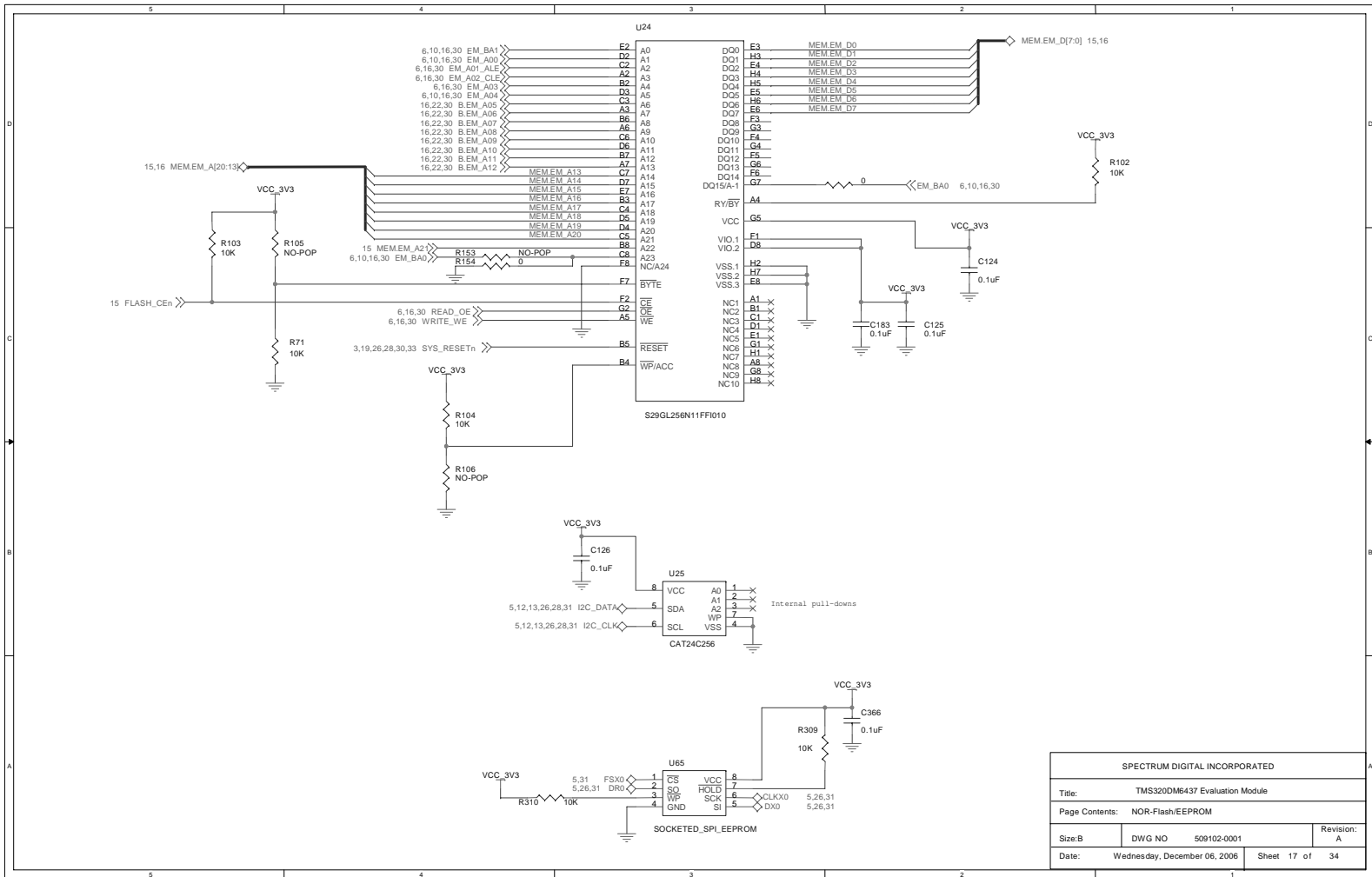
PIN 5 TO 6 SRAM

PIN 7 TO 8 DAUGHTERCARD

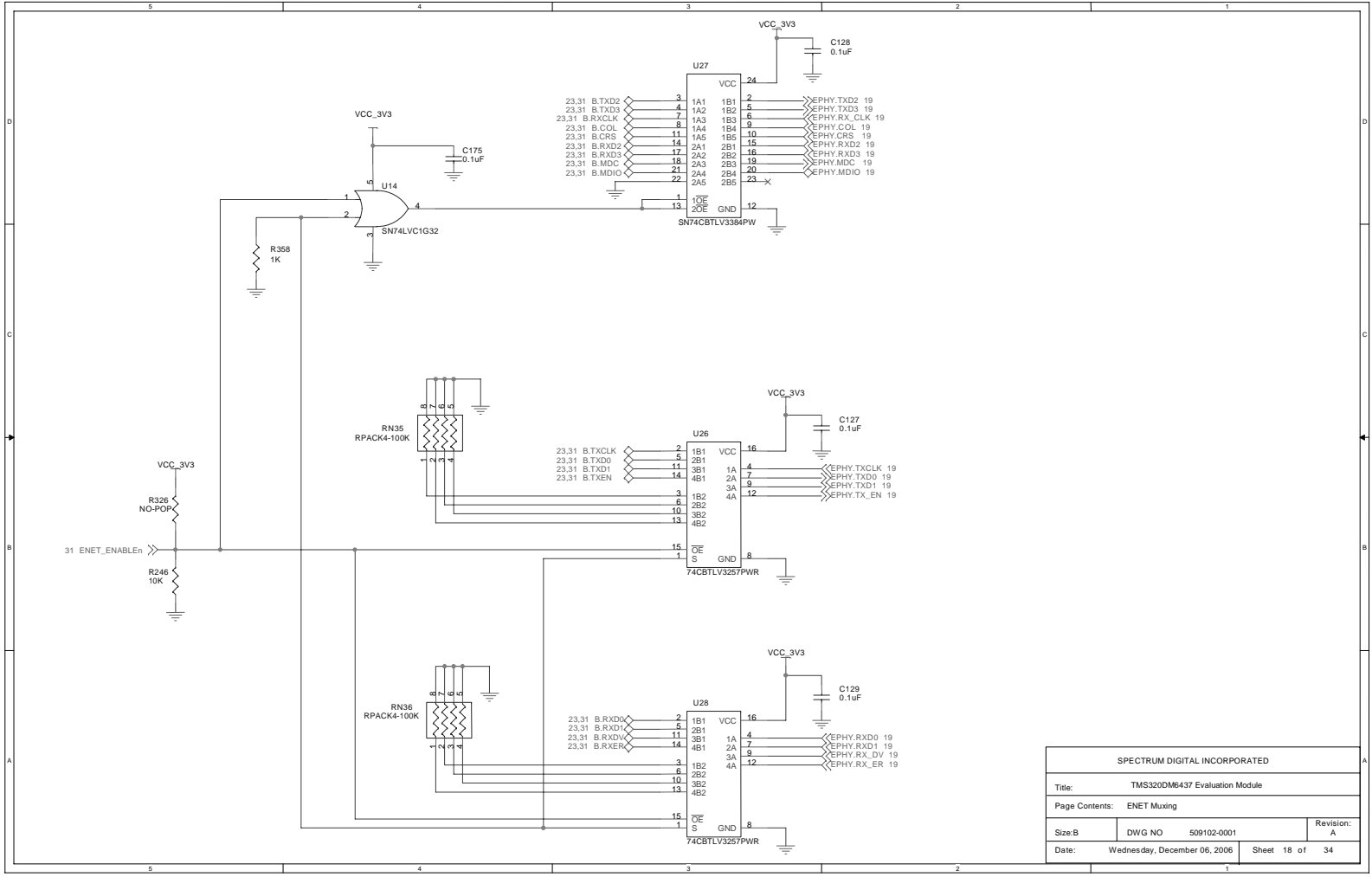
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: EMIF Muxing | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet | 15 of 34 |



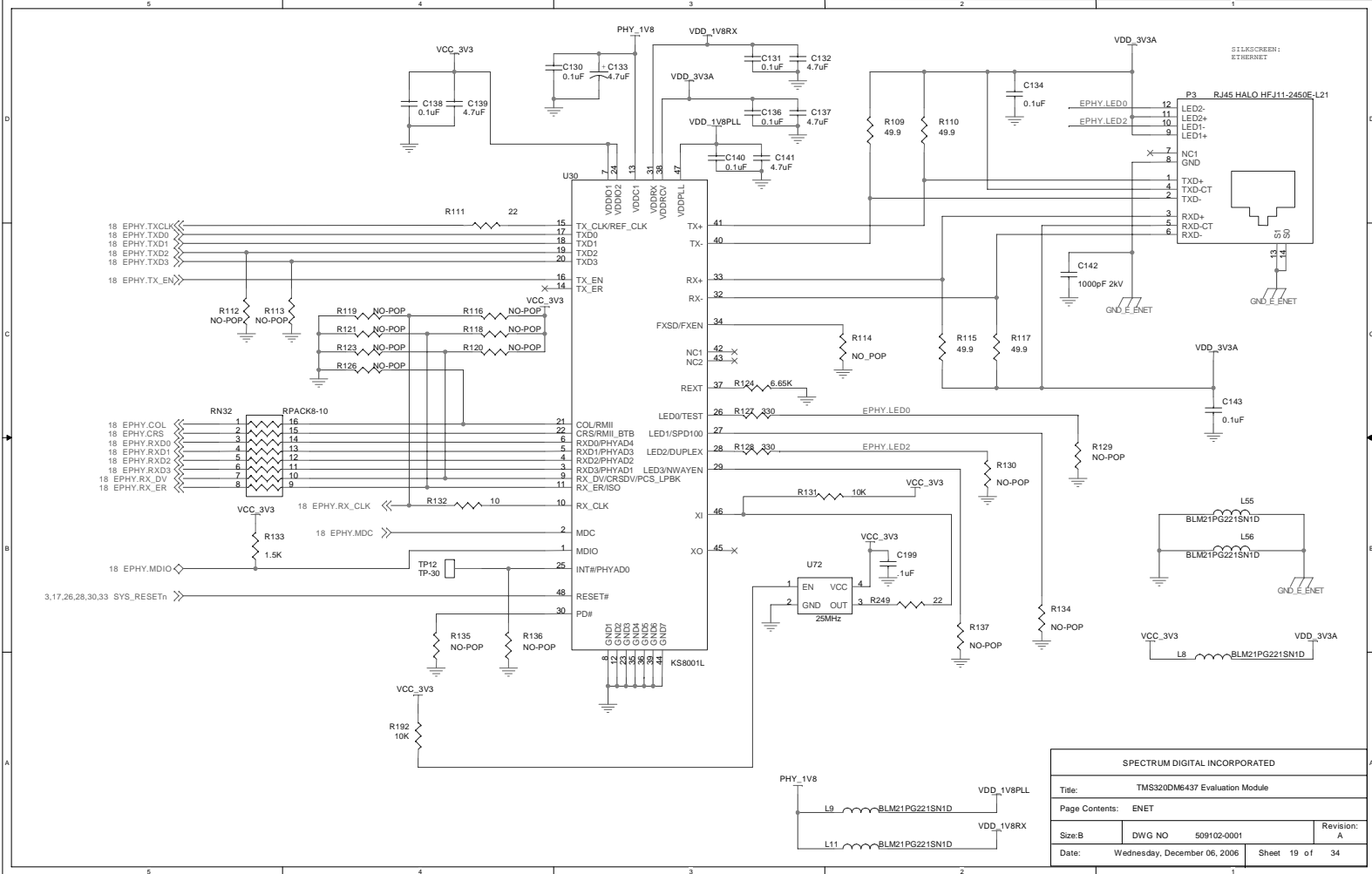
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: NAND-Flash/DRAM | | | |
| Size: B | DWG NO | 509102-0001 | Revision: B |
| Date: | Wednesday, December 06, 2006 | Sheet | 16 of 34 |



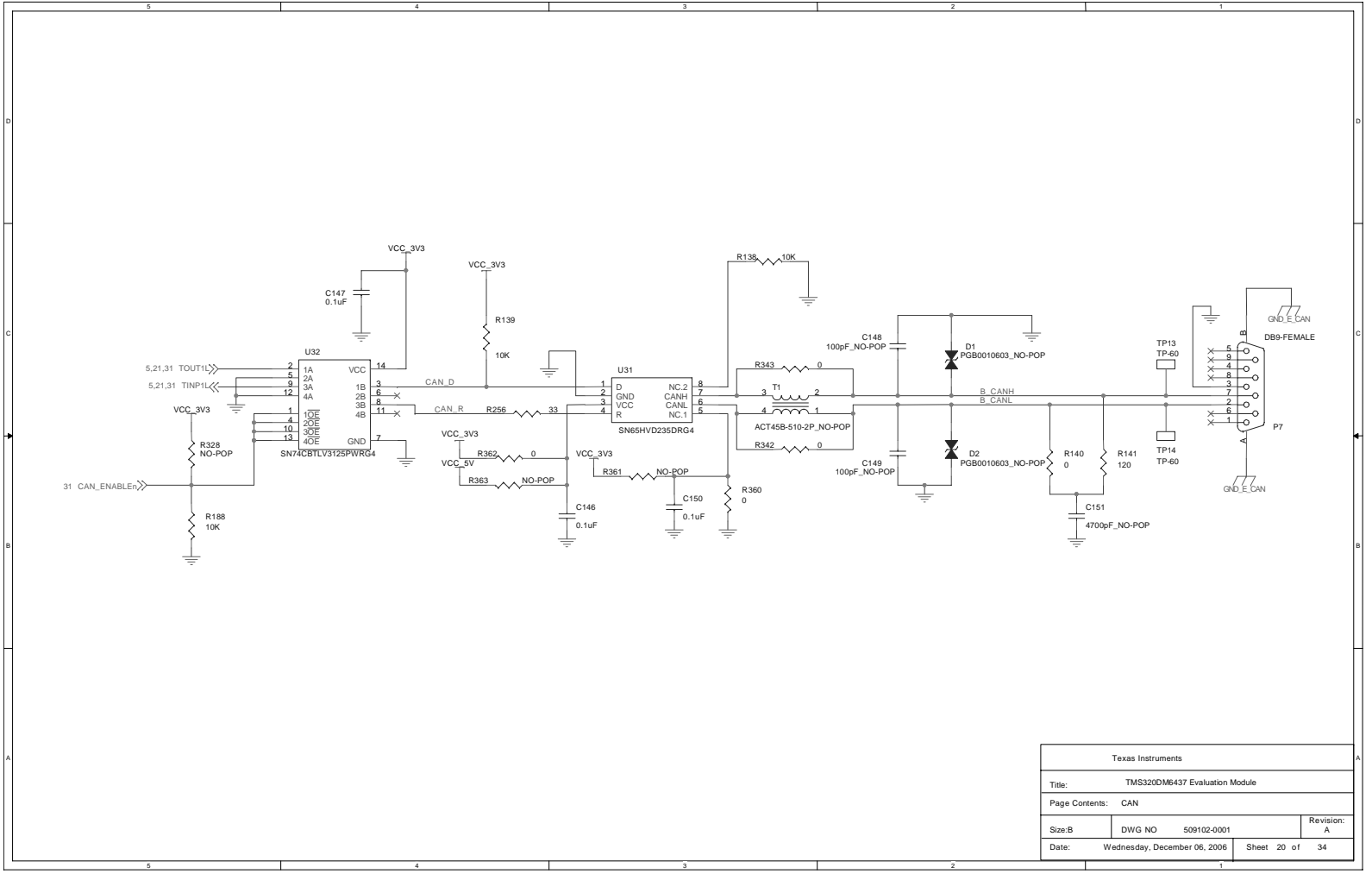
| SPECTRUM DIGITAL INCORPORATED | | | |
|---------------------------------------|------------------------------|-------------|----------------|
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: NOR-Flash/EEPROM | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | | Sheet 17 of 34 |



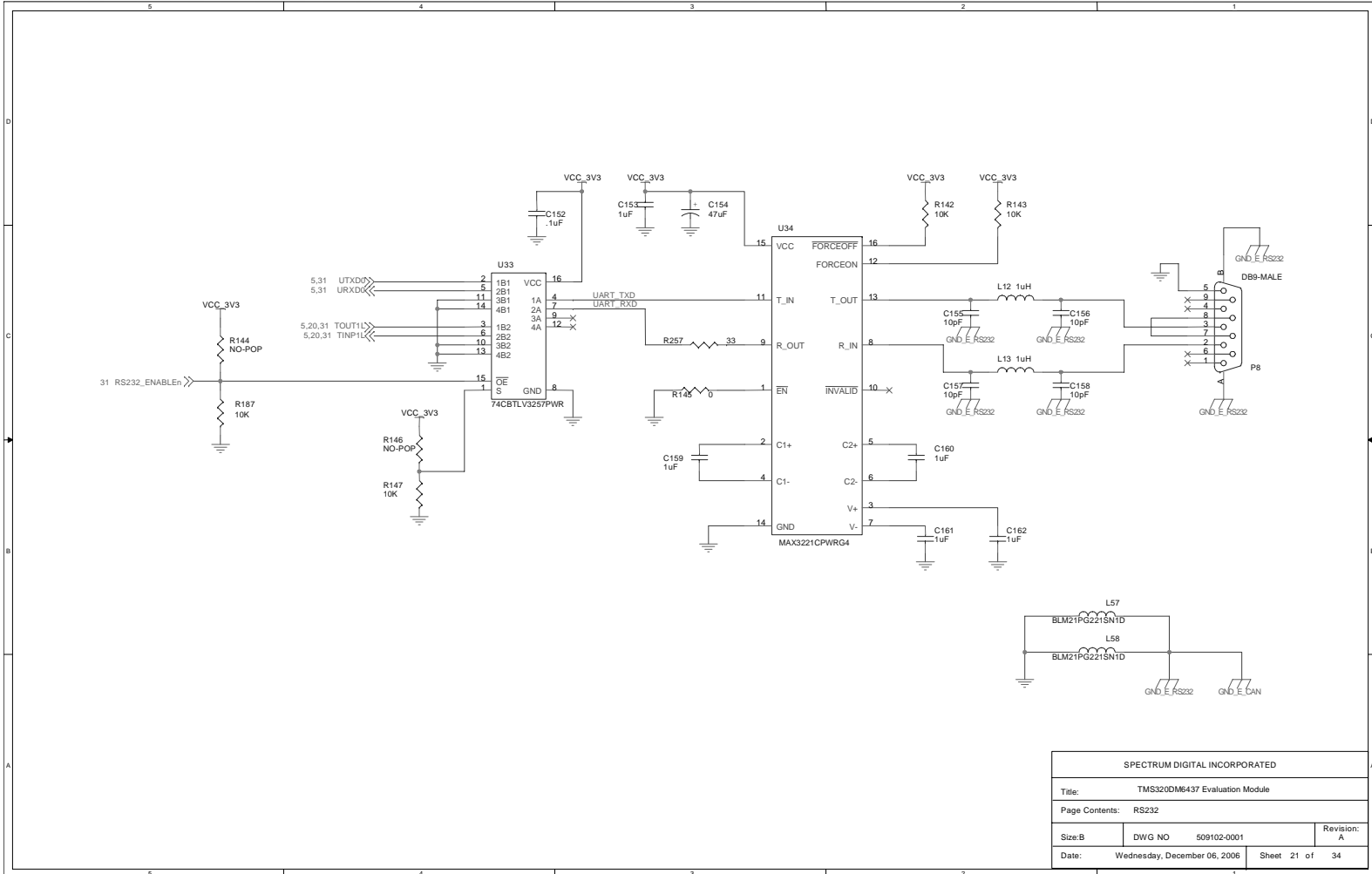
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: ENET Muxing | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 18 of | 34 |



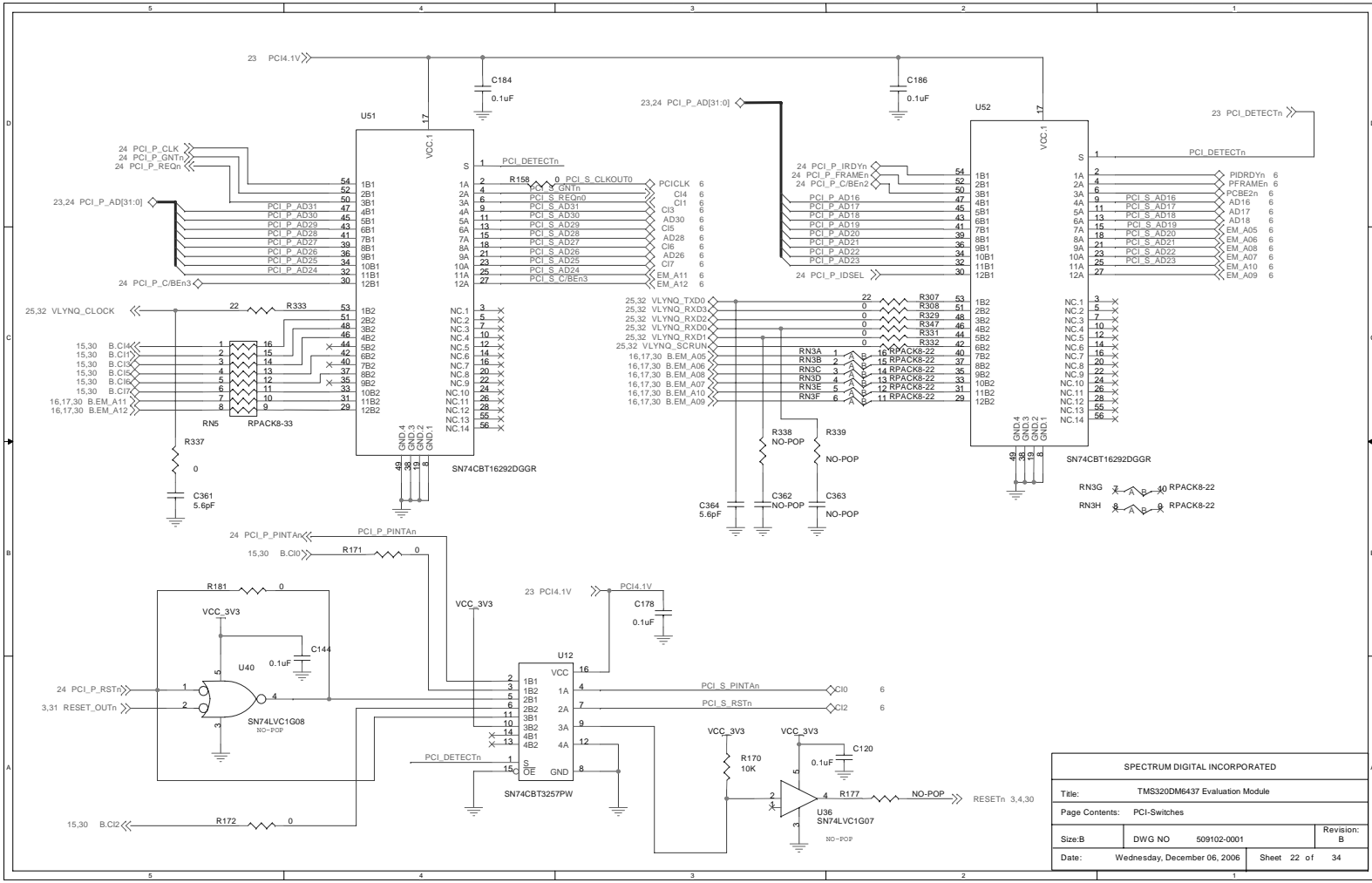
| SPECTRUM DIGITAL INCORPORATED | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: ENET | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet | 19 of 34 |



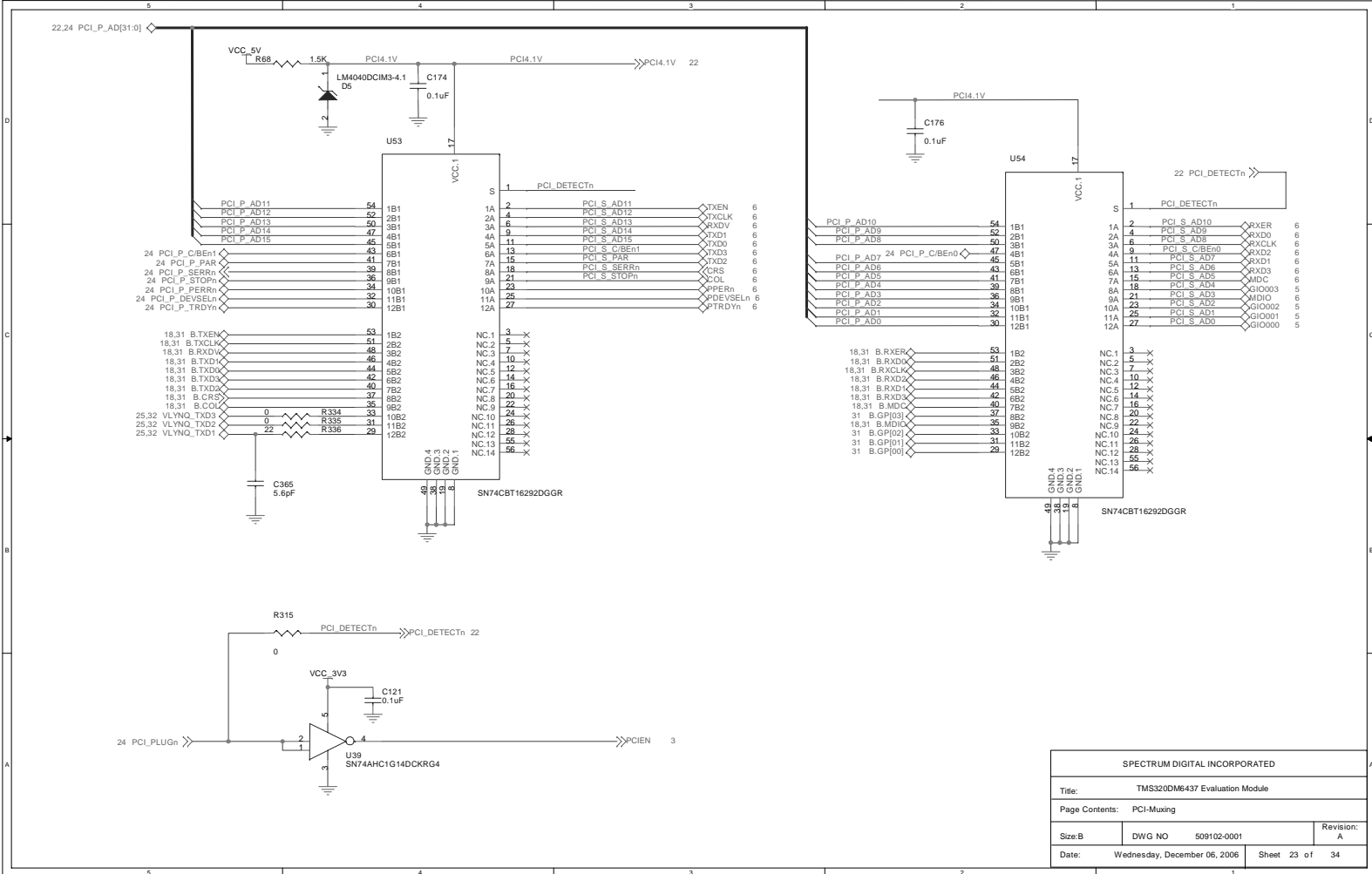
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| Texas Instruments | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: CAN | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet | 20 of 34 |

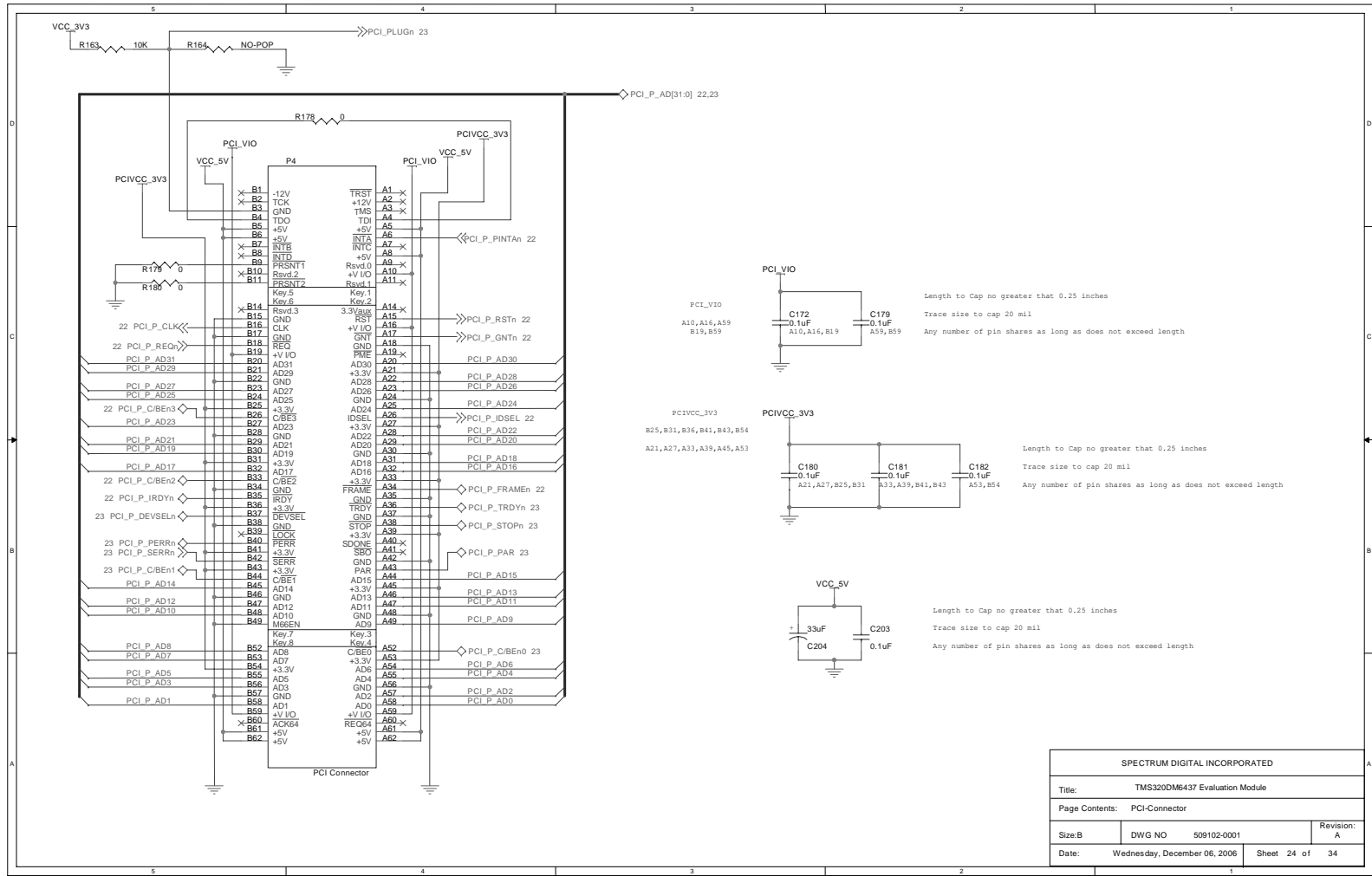


| | | | |
|---------------------------------------|------------------------------|-------------|----------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: RS232 | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | | Sheet 21 of 34 |



| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: PCI-Switches | | | |
| Size: B | DWG NO | 509102-0001 | Revision: B |
| Date: | Wednesday, December 06, 2006 | Sheet | 22 of 34 |





PCI_VIO
A10, A16, A59
B19, B59

Length to Cap no greater than 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

PCI_VCC_3V3
B25, B31, B36, B41, B43, B54
A21, A27, A33, A39, A45, A53

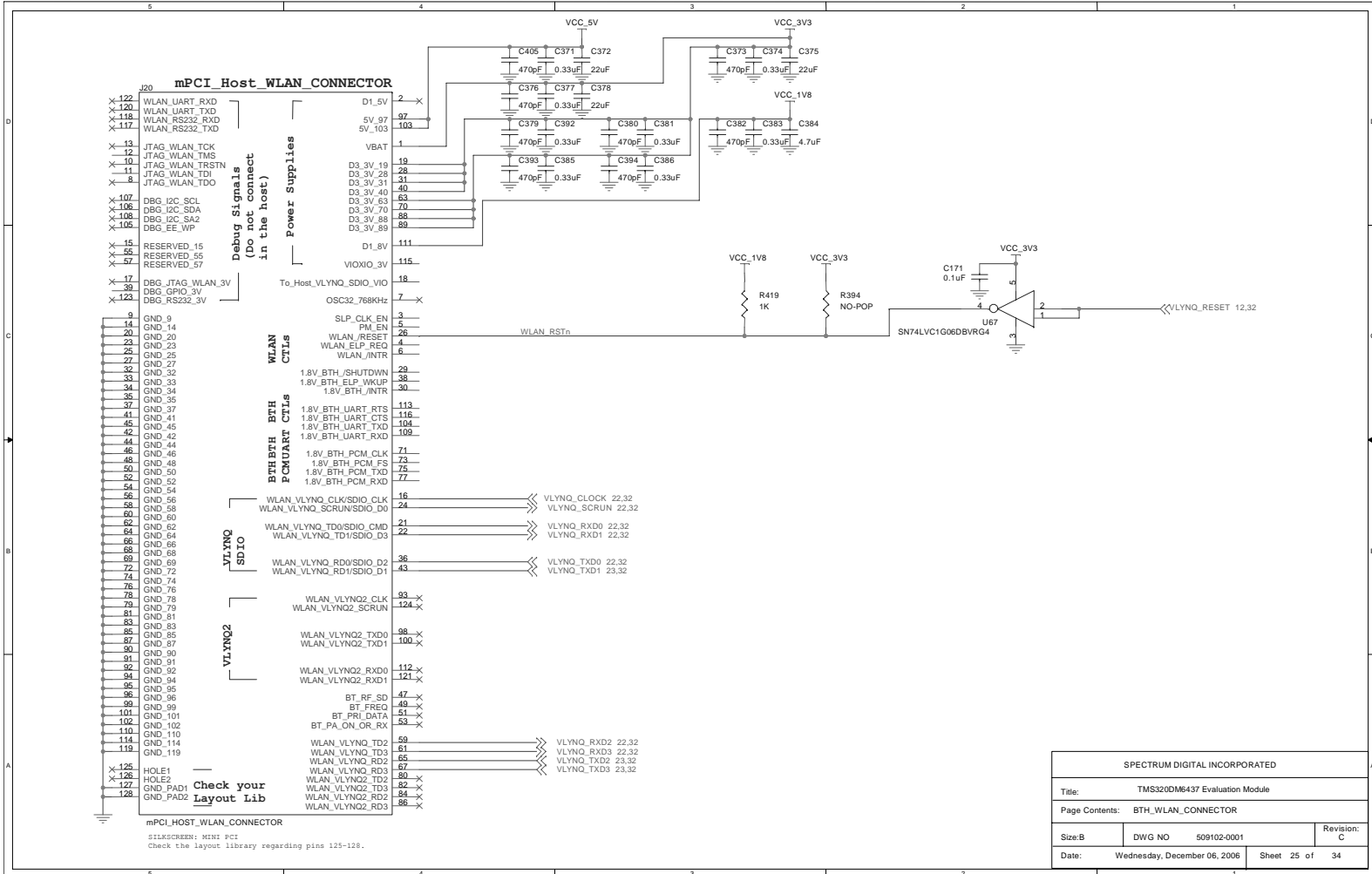
Length to Cap no greater than 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

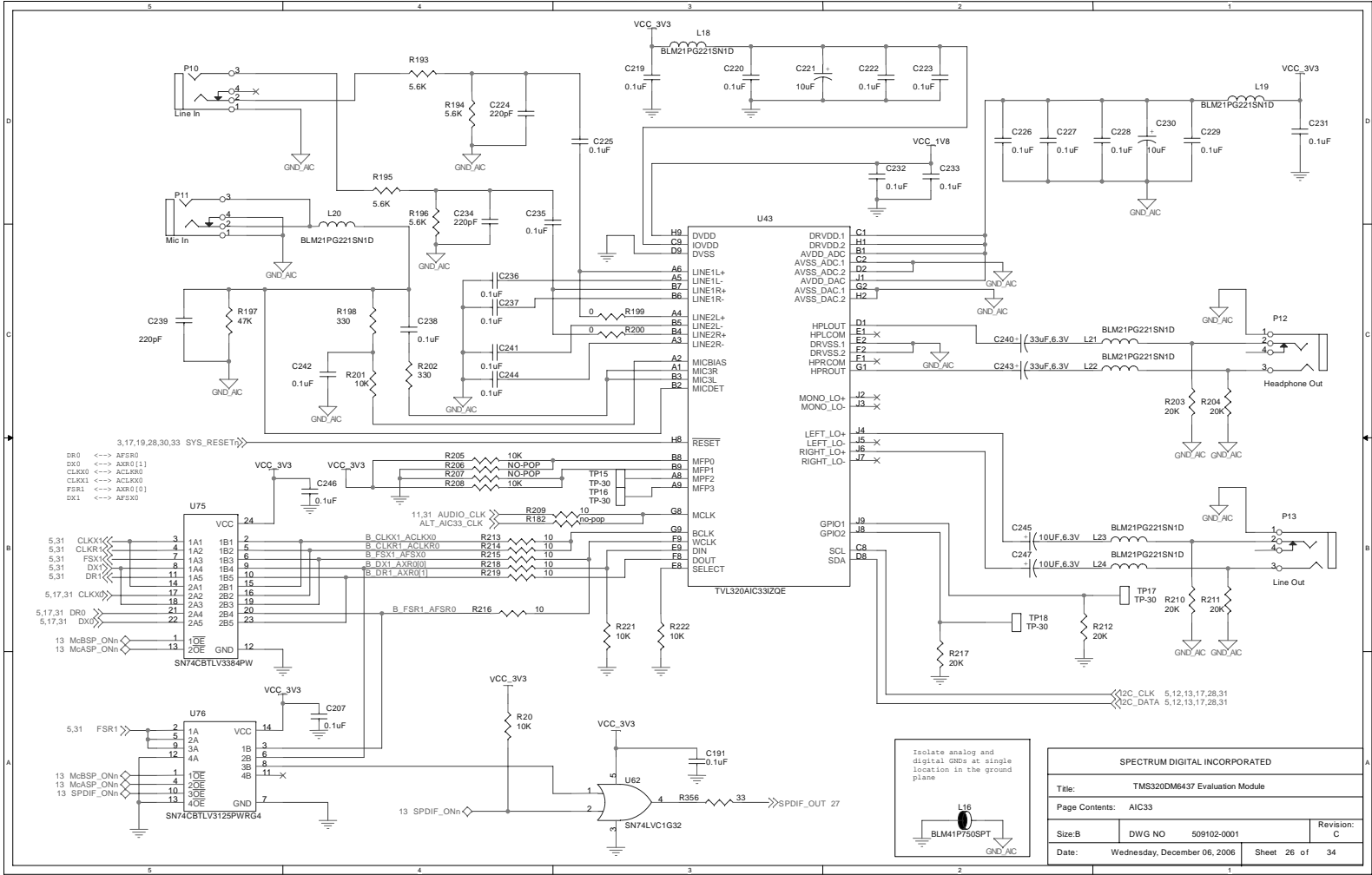
VCC_5V

Length to Cap no greater than 0.25 inches
Trace size to cap 20 mil
Any number of pin shares as long as does not exceed length

| SPECTRUM DIGITAL INCORPORATED | | | |
|---------------------------------------|---------------------|-------------|--|
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: PCI-Connector | | | |
| Size: B | DWG NO: 509102-0001 | Revision: A | |
| Date: Wednesday, December 06, 2006 | Sheet 24 of 34 | | |

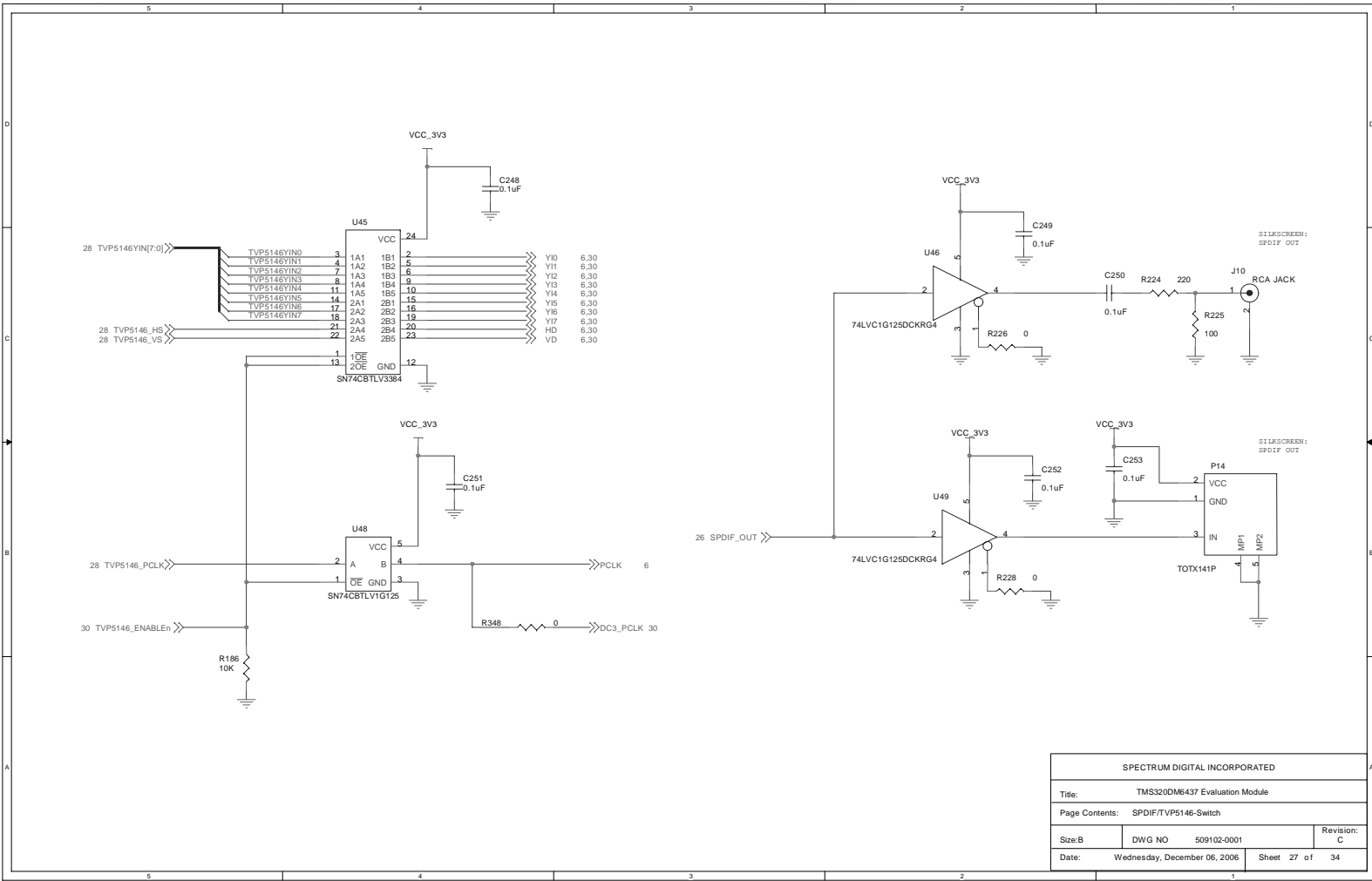
Spectrum Digital, Inc



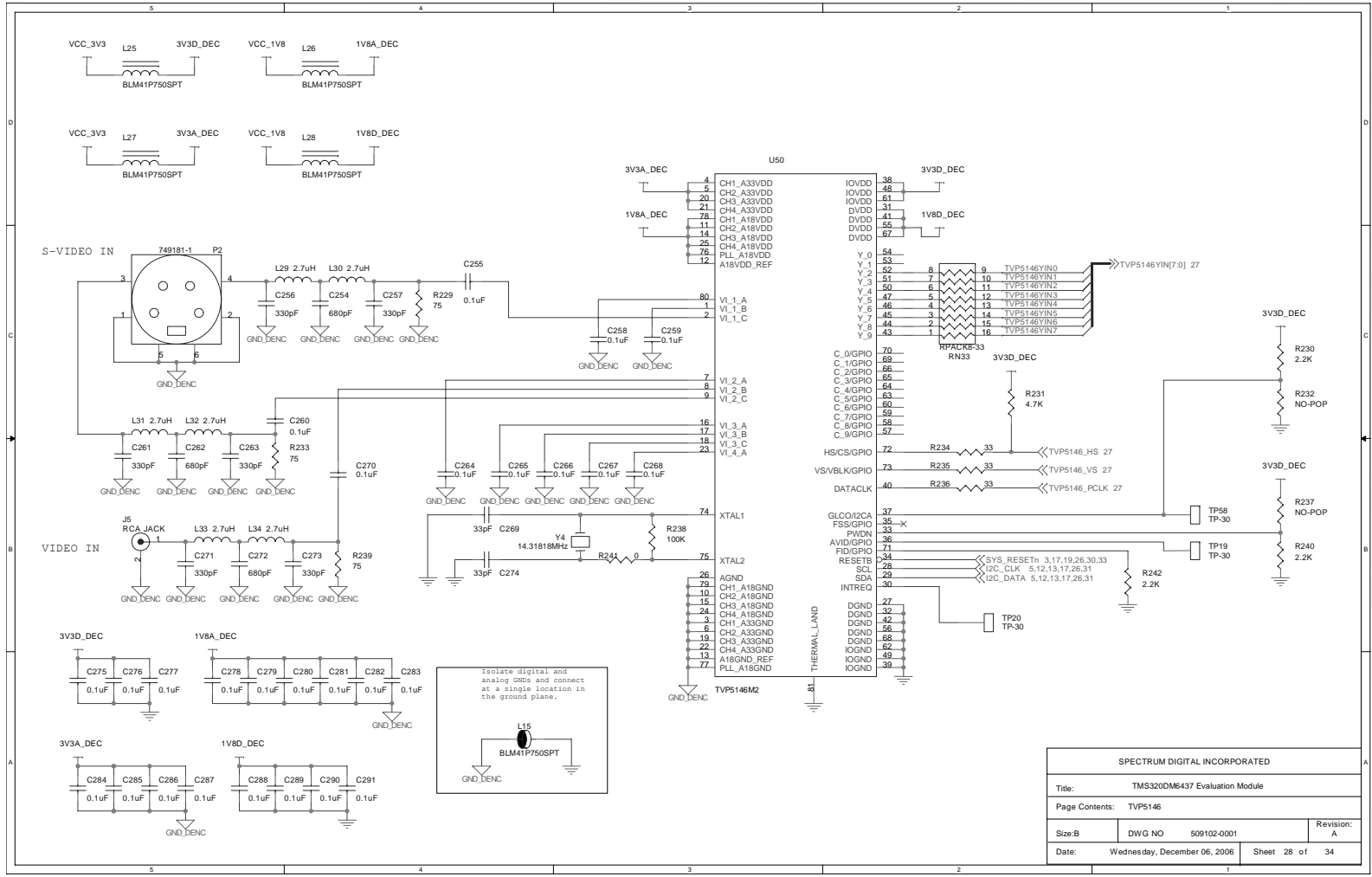


| | |
|---------------------------------------|---------------------|
| SPECTRUM DIGITAL INCORPORATED | |
| Title: TMS320DM6437 Evaluation Module | |
| Page Contents: AIC33 | |
| Size: B | DWG NO: 509102-0001 |
| Date: Wednesday, December 06, 2006 | Revision: C |
| Sheet 26 of 34 | |

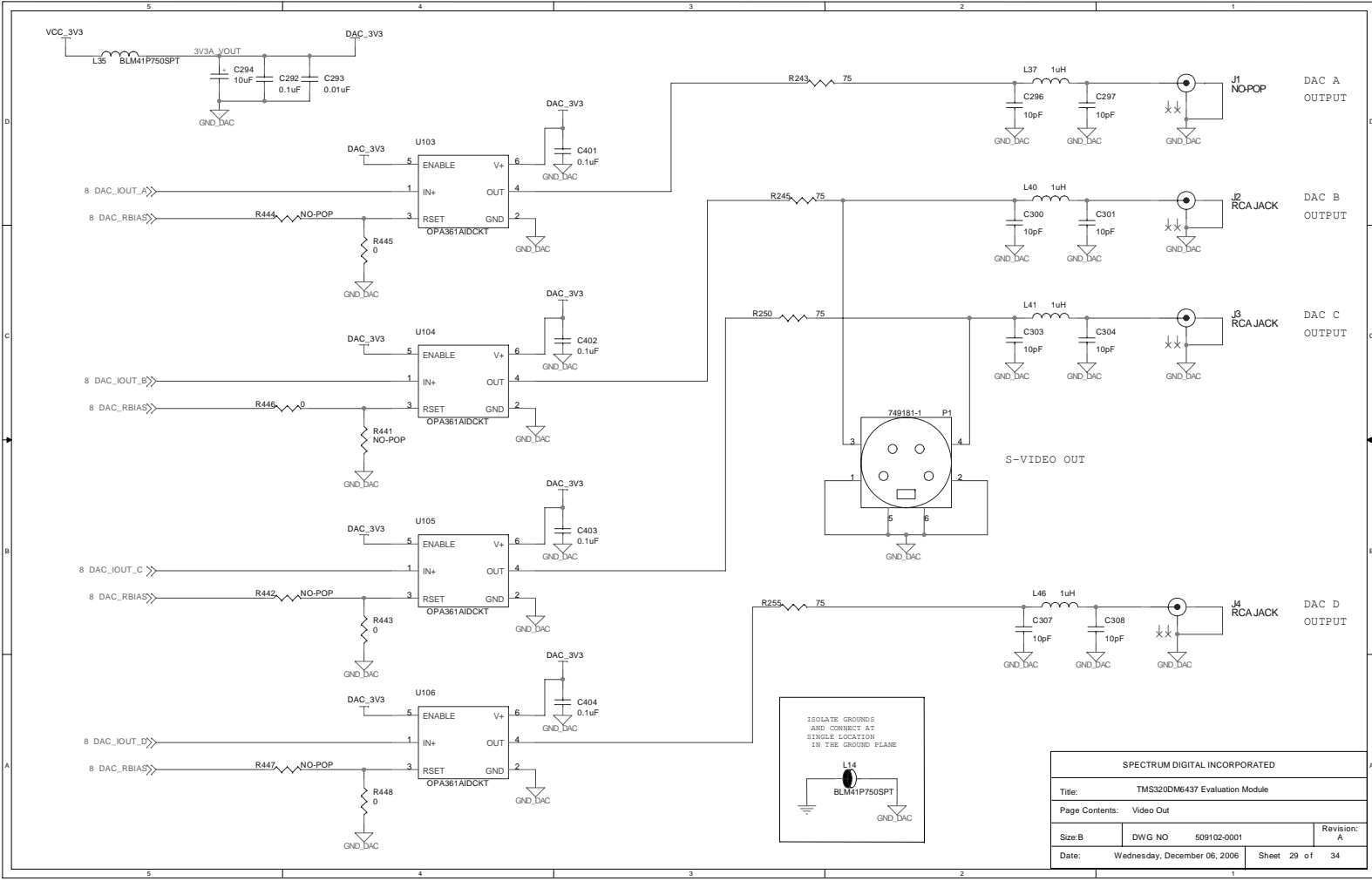
Spectrum Digital, Inc



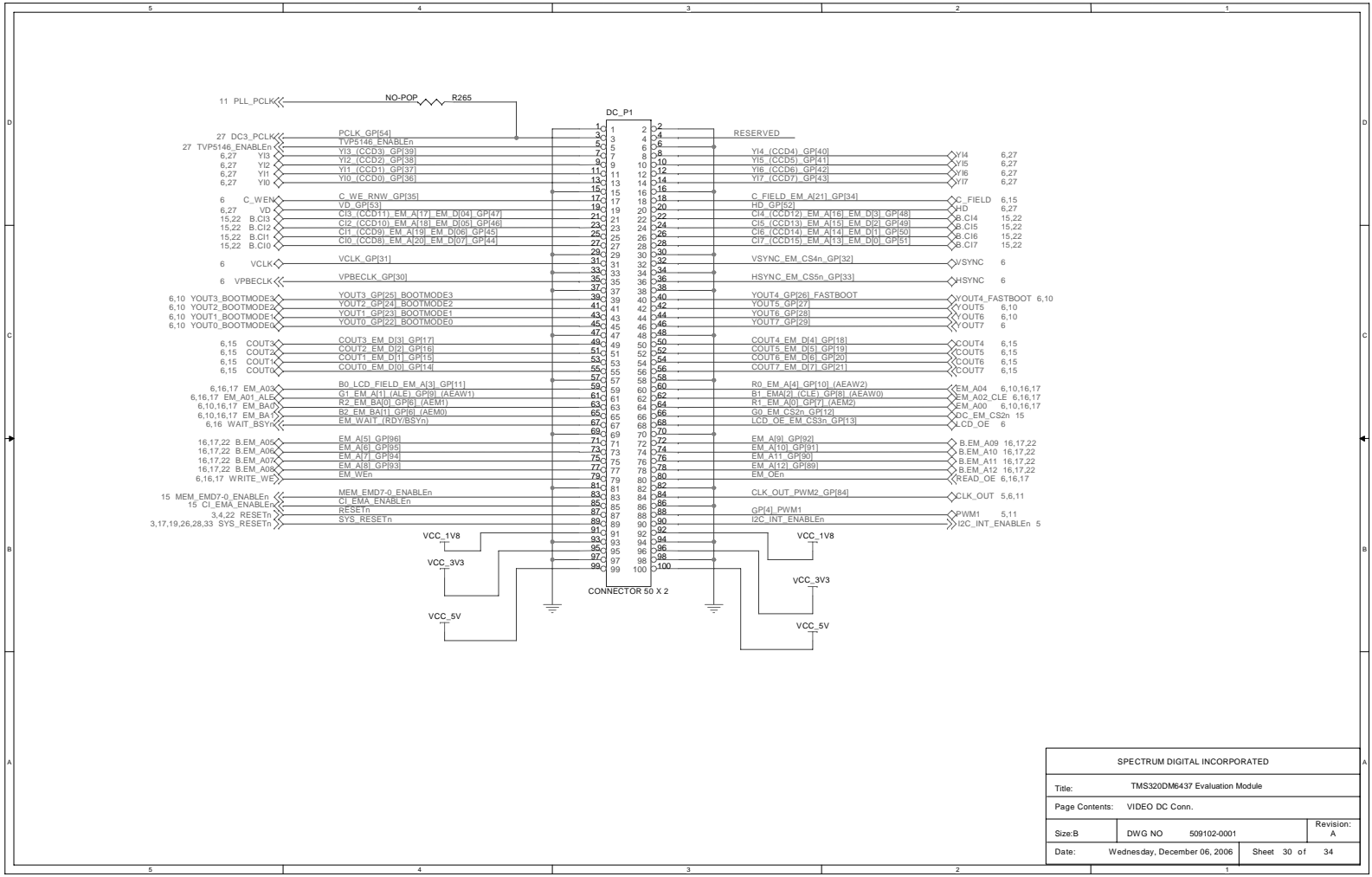
| | | | |
|---------------------------------------|------------------------------|----------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: SPDIF/TVPS146-Switch | | | |
| Size-B | DWG NO | 509102-0001 | Revision: C |
| Date: | Wednesday, December 06, 2006 | Sheet 27 of 34 | |



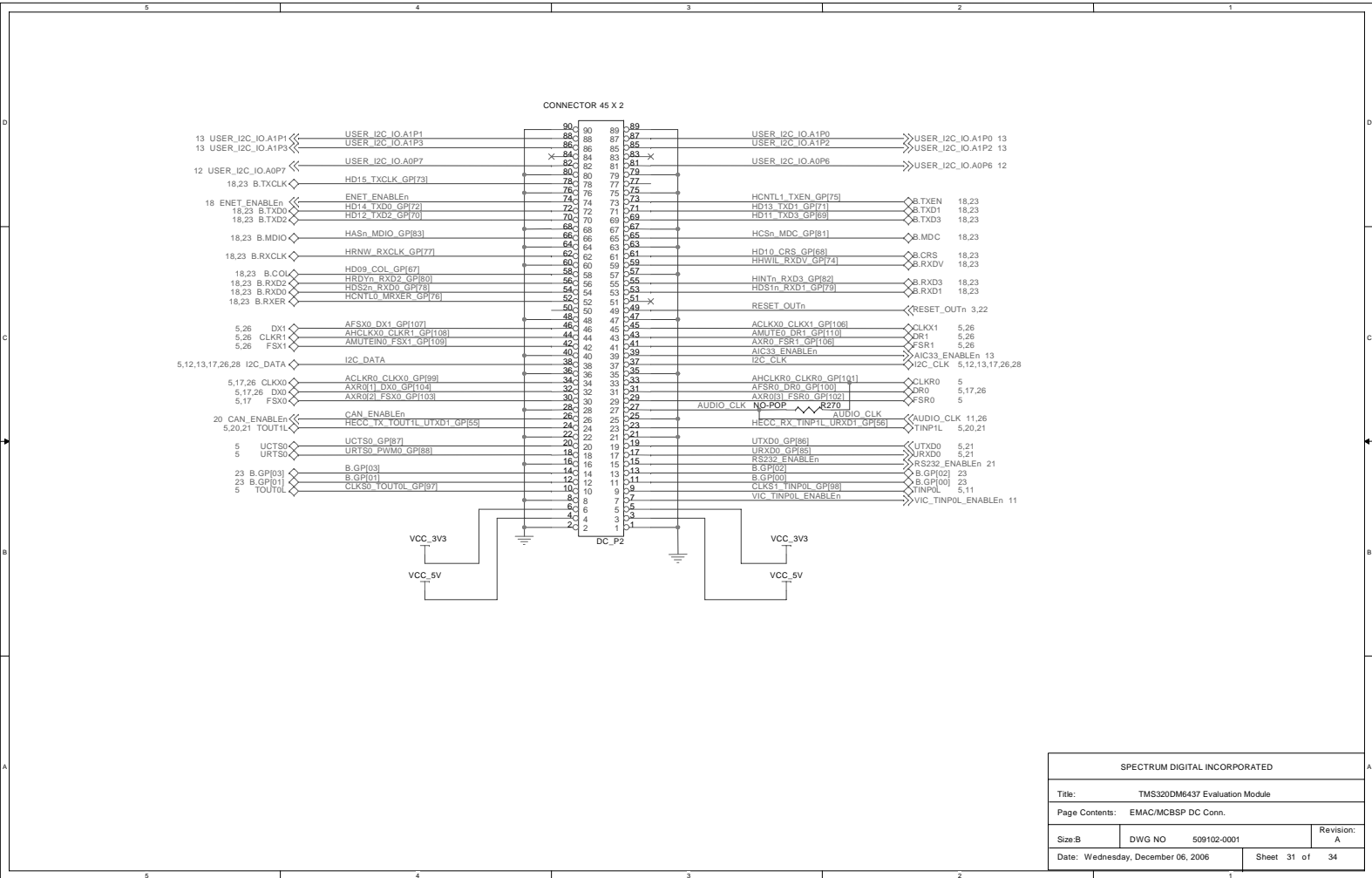
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: TVP5146 | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 28 of | 34 |



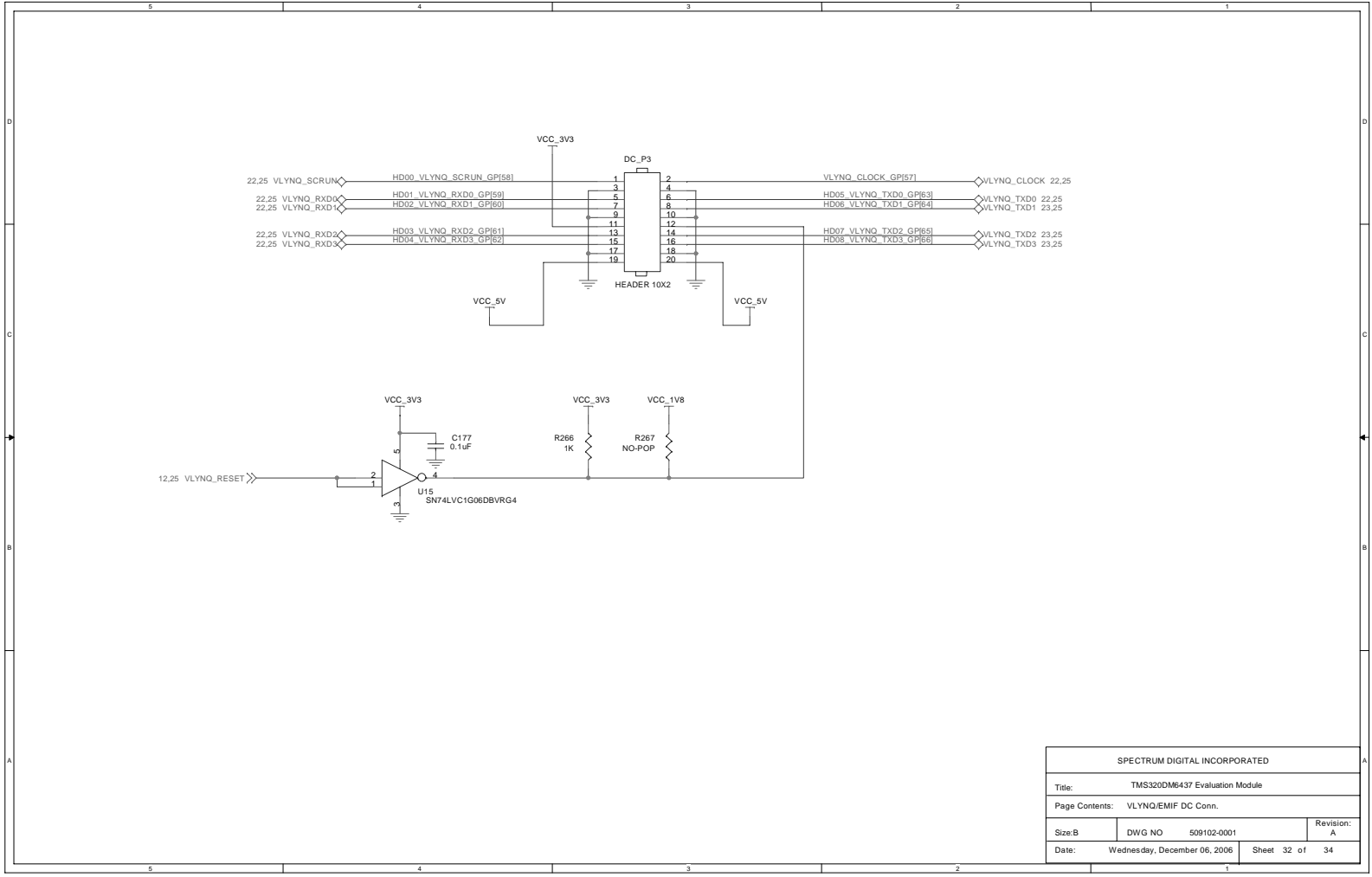
| | | | |
|---------------------------------------|----------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: Video Out | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: Wednesday, December 06, 2006 | Sheet 29 of 34 | | |



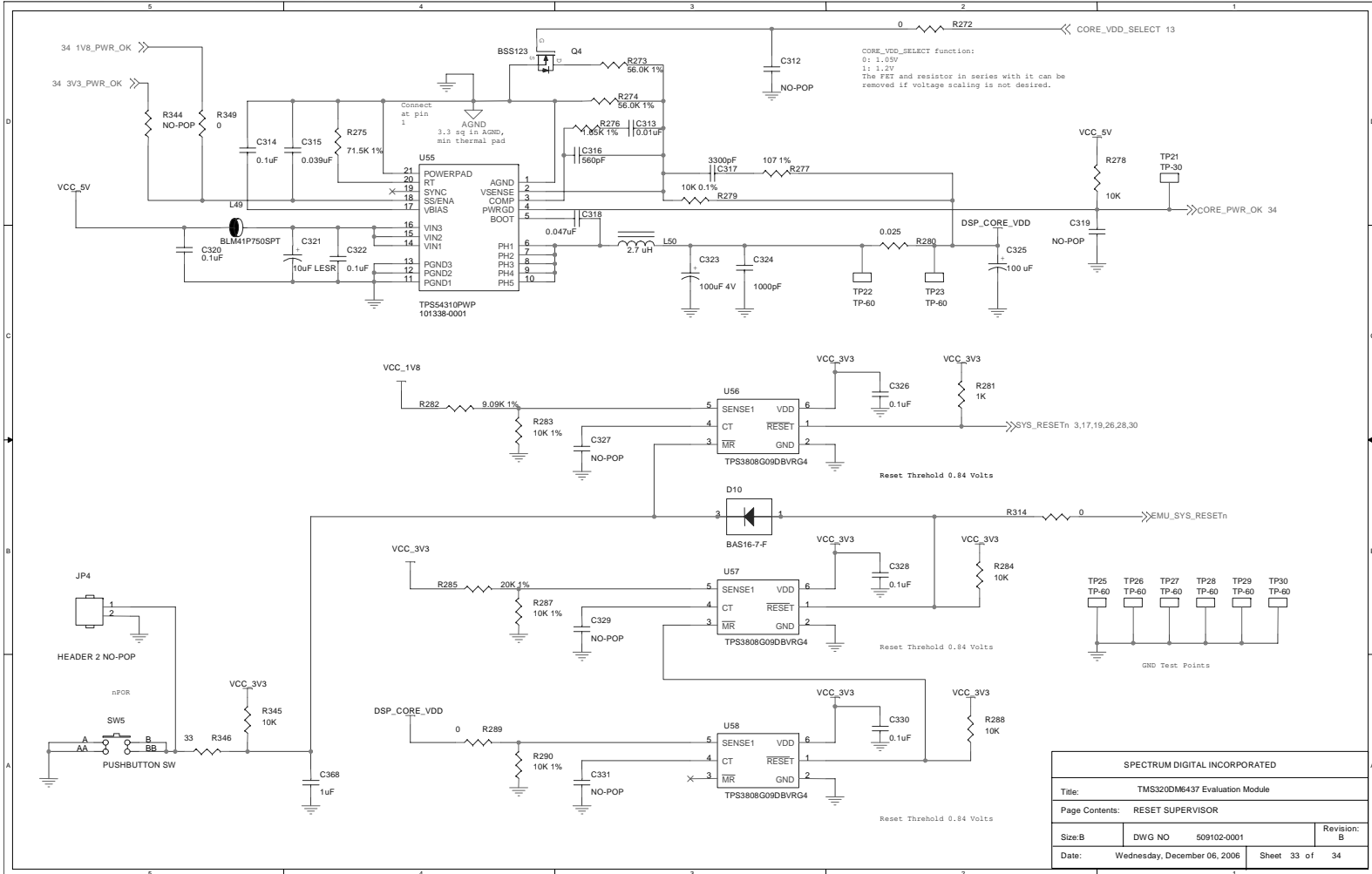
| | | | |
|---------------------------------------|------------------------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: VIDEO DC Conn. | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet | 30 of 34 |

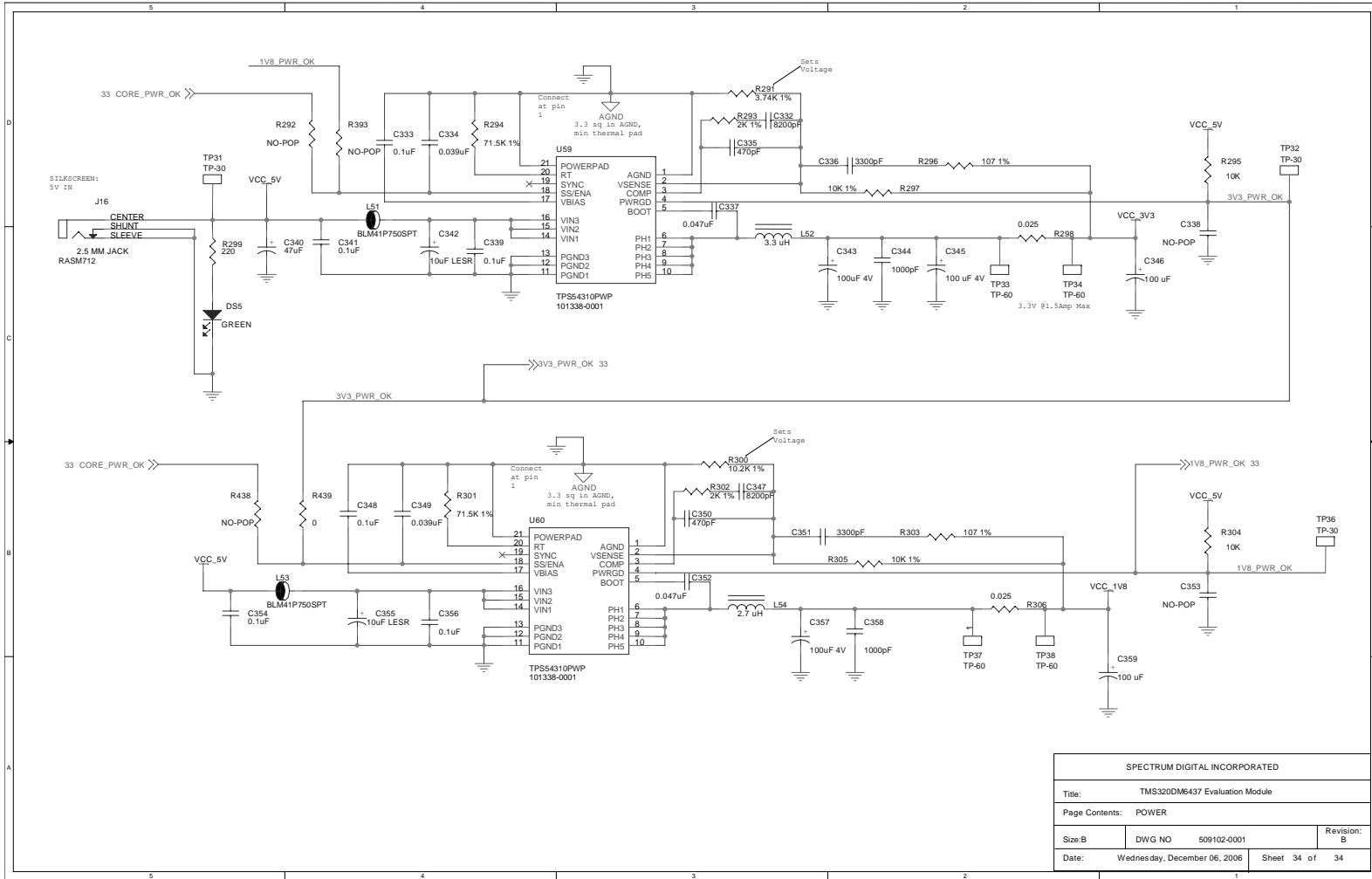


| | | | |
|---------------------------------------|----------------|-------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: EMAC/MCBS DP Conn. | | | |
| Size B | DWG NO | 509102-0001 | Revision: A |
| Date: Wednesday, December 06, 2006 | Sheet 31 of 34 | | |



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|---------------------------------------|------------------------------|----------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: VLYNQ/EMIF DC Conn. | | | |
| Size: B | DWG NO | 509102-0001 | Revision: A |
| Date: | Wednesday, December 06, 2006 | Sheet 32 of 34 | |





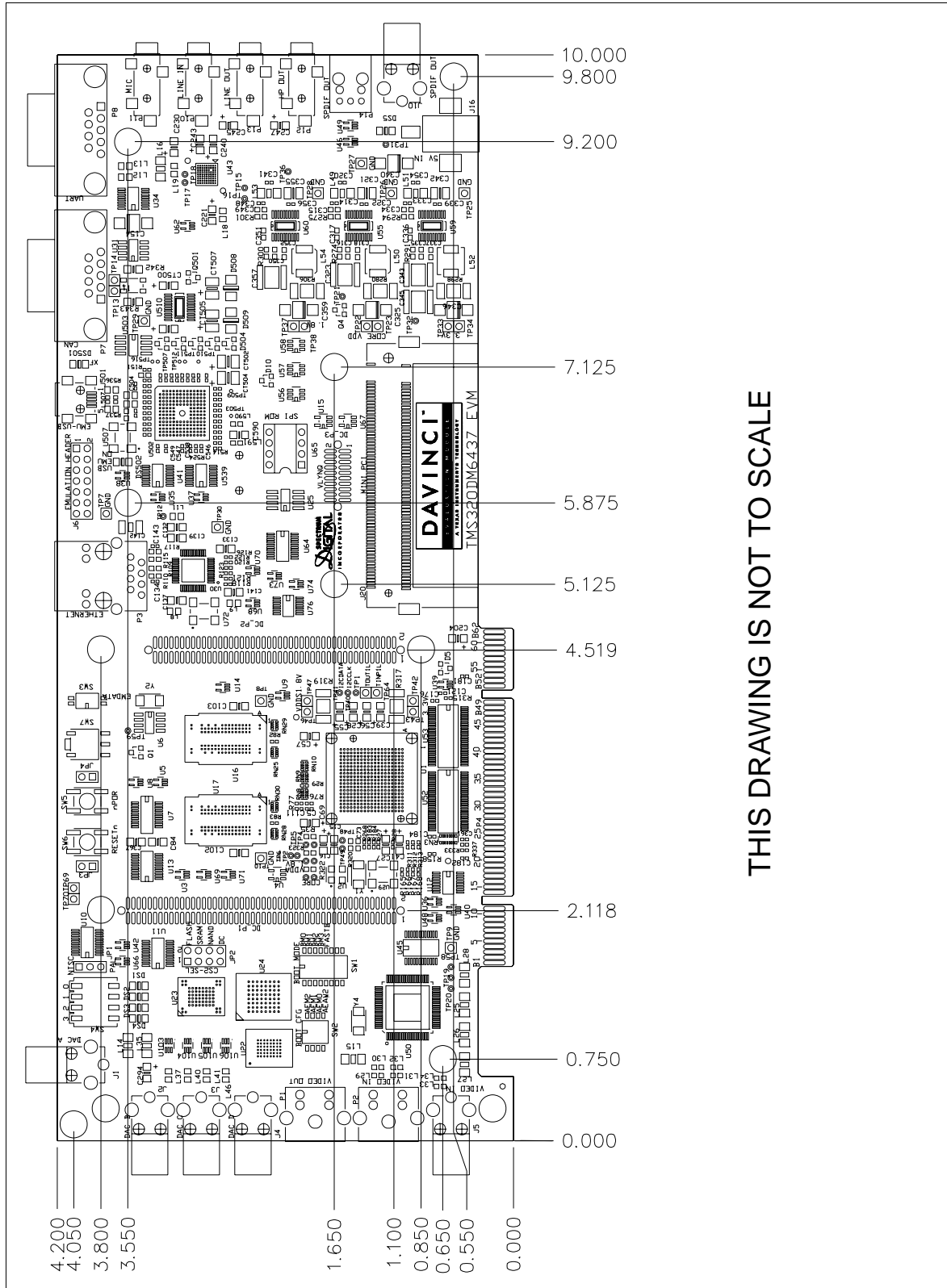
| | | | |
|---------------------------------------|------------------------------|----------------|-------------|
| SPECTRUM DIGITAL INCORPORATED | | | |
| Title: TMS320DM6437 Evaluation Module | | | |
| Page Contents: POWER | | | |
| Size: B | DWG NO | 509102-0001 | Revision: B |
| Date: | Wednesday, December 06, 2006 | Sheet 34 of 34 | |

Spectrum Digital, Inc

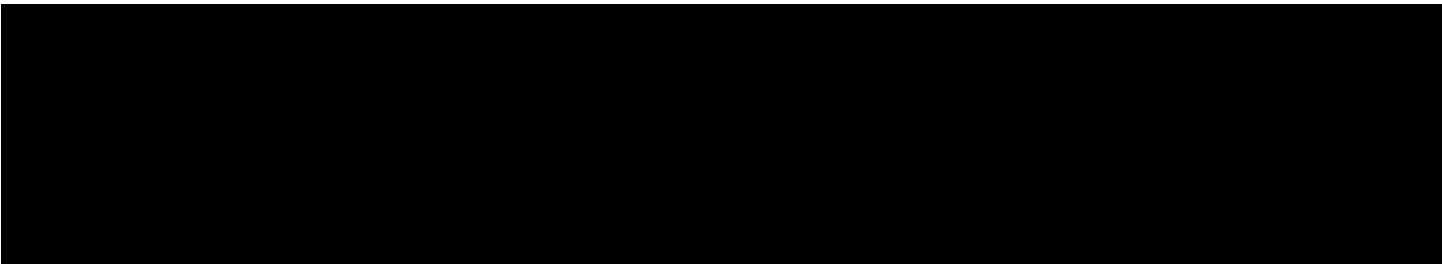
Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM6437 EVM produced by Spectrum Digital.



THIS DRAWING IS NOT TO SCALE



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509105-0001 Rev C