

***TMS320DM642 Evaluation
Module with TVP Video Decoders***

*Technical
Reference*

**TMS320DM642 Evaluation Module
With TVP Video Decoders
Technical Reference**

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About This Manual

This document describes the board level operations of the TMS320DM642 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM642 Digital Signal Processor.

The DM642 Evaluation Module is a table top or PCI plug-in card that allows engineers and software developers to evaluate certain characteristics of the TMS320DM642 DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM642 Evaluation Module will sometimes be referred to as the DM642 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Below are descriptions of the .pdf files. Refer to the Texas Instruments web page (<http://www.ti.com>) for the latest revisions of these documents.

Application Notes & User Guides

spra920.pdf: DM642 EVM Daughter card Interface Specification

sprs200b.pdf: TMS320DM642 Video/Imaging Fixed-Point Digital Signal Processor

spru041b.pdf: TMS320C6000 DSP Multichannel Audio Serial Port (McASP) Reference Guide

spru175a.pdf: TMS320C6000 DSP Inter-Integrated Circuit (I2C) Module Reference Guide

spru190d.pdf: TMS320C6000 Peripherals Reference Guide

spru295.pdf: TMS320DM642 EVM OSD FPGA User's Guide

spru610.pdf: TMS320C64x DSP Two-Level Internal Memory Reference Guide

spru628.pdf: TMS320C6000 DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module Reference Guide

spru629.pdf: TMS320C64x DSP Video Port/VCXO Interpolated Control (VIC) Port Reference Guide

Table 1: Manual History

Revision	History
A	Production Release
B	Updated for HD Filters

Table 2: Board History

Revision	History
A	Prototype Release
B	Production Release

Chapter 1

Introduction to the TMS320DM642 EVM

Chapter One provides a description of the TMS320DM642 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM642 EVM is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C64xx DSP family. The EVM also serves as a hardware reference design for the TMS320DM642 DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

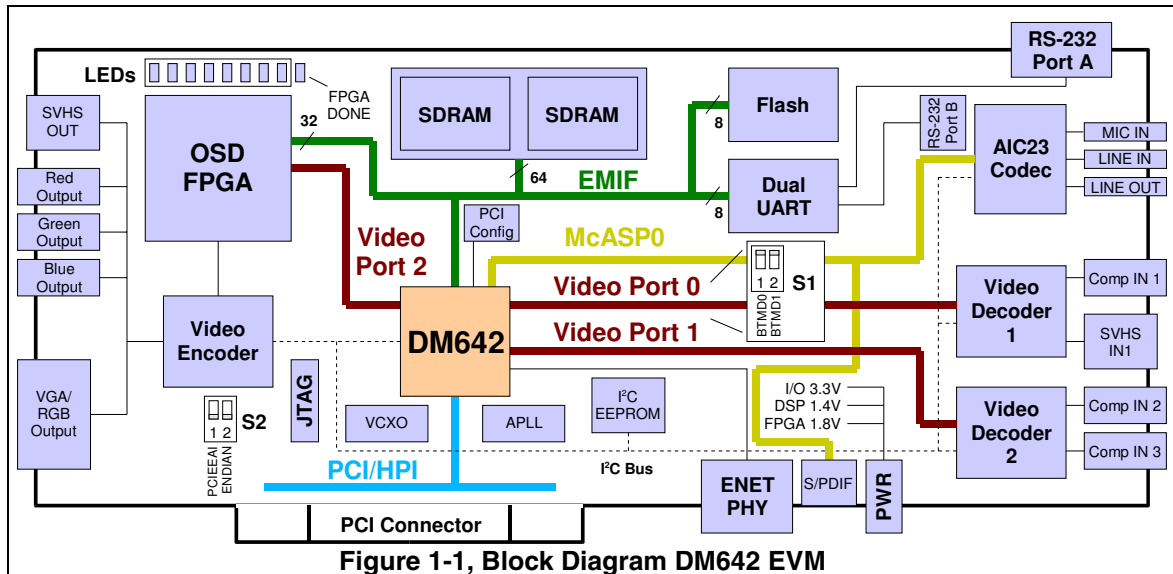


Figure 1-1, Block Diagram DM642 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320DM642 DSP operating at 720 MHz.
- Standalone or standard PCI computer slot operation
- 3 video ports with 2 on board decoders and 1 on board encoder
- 32 Mbytes of synchronous DRAM
- On Screen display (OSD) via FPGA
- 4 Mbytes of non-volatile Flash memory
- AIC23B stereo codec
- Ethernet interface
- Software board configuration through registers implemented in FPGA
- Configurable boot load options
- JTAG emulation through on-board external emulator interface

- 8 user LEDs
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- Dual UART with RS-232 drivers

1.2 Functional Overview of the TMS320DM642 EVM

The DSP on the DM642 EVM interfaces to on-board peripherals through the 64-bit wide EMIF or one of the three 8/16 bit wide video ports. The SDRAM, Flash, FPGA, and UART are each connected to one of the busses. The EMIF bus is also connected to the daughter card expansion connectors which are used for add-in boards.

On board video encoders and decoders interface to the video ports and expansion connectors. Two decoders and one encoder are standard on the EVM. On screen display functions are implemented in an external FPGA which resides between the output video port and the video decoder.

An on-board AIC23B codec allows the DSP to transmit and receive analog audio signals. I²C bus is used for the codec control interface and the McASP is used for data. Analog interface is done through three 3.5mm audio jacks that correspond to microphone input, line input, and line output. The codec can select the microphone or the line input as the active input. The analog output is driven to the line out (fixed gain) connector. The McASP can be re-routed to the expansion connectors in software.

A programmable gate array called an FPGA is used to implement glue logic that ties the board components together. The FPGA also has a register based software user interface that lets the user configure the board by reading and writing to these registers.

The EVM includes 8 LEDs which can be used to provide the user with interactive feedback. These LEDs are accessed by reading and writing to the FPGA registers.

An included 5V external power supply is used to power the board for stand alone applications whereas the PC bus supplies power when used as a PCI plug in card. On-board switching voltage regulators provide the 1.4V DSP core voltage and 3.3V I/O supplies. The board is held in reset until these supplies are within operating specifications. The EVM also has an LDO regulator which provides +1.8 volt FPGA core voltage, and +3.3 volt encoder and decoder supplies.

Code Composer communicates with the EVM through an external emulator via the 14 pin or 60 pin external JTAG connectors.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development environment. Code Composer communicates with the board through an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The C64xx family of DSPs has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are always 32-bits wide.

The memory map shows the address space of a generic DM642 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The EMIF (External Memory Interface) has 4 separate addressable regions called chip enable spaces (CE0-CE3). The SDRAM occupies CE0 while the Flash, UART, and FPGA are mapped to CE1. Daughter cards use CE2 and CE3. CE3 is configured for synchronous operation for on screen display functions and other synchronous registers implemented in the external FPGA.

Address	Generic DM642 Address Space	DM642 EVM
0x00000000	Internal Memory/Cache	Internal Memory/Cache
0x00040000	Reserved Space or Peripheral Registers	Reserved or Peripheral
0x80000000	EMIF CE0	SDRAM
0x90000000	EMIF CE1	Flash
0xA0000000	EMIF CE2	UART/FPGA Regs
0xB0000000	EMIF CE3	Daughter Card
		FPGA Sync Regs
		Daughter Card

Figure 1-2, Memory Map, DM642 EVM

1.5 Configuration Switch Settings

The EVM has two 2 position configuration switches that allow users to control the operational state of the DSP when it is released from reset. The configuration switches are labeled S1 and S2 on the EVM board.

Switch 1 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to EMIF boot (out of 8-bit Flash) in little endian mode. The table below shows the settings for switch S1.

Table 1: Configuration Switch S1 Settings

S1-2	S1-1	Configuration Description
Off	Off	No Boot
Off	On	HPI/PCI Boot
On	Off	Reserved
On *	On *	EMIF boot from 8-bit Flash

Configuration switch 2 controls the endianness of the DSP and PCI ROM enable. The tables below shows the settings for switch S2.

Table 2: Configuration Switch S2-1 Settings

S2-1	Configuration Description
Off	PCI EEPROM Disabled
On *	PCI EEPROM Enabled

Table 3: Configuration Switch S2-2 Settings

S2-1	Configuration Description
Off *	Little Endian Mode
On	Big Endian Mode

* Default as shipped configuration

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J5) or from the PCI slot. Internally, the +5V input is converted into +1.4V and +3.3V using Texas Instruments swift voltage regulators. The +1.4V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm barrel-type plug. LDO voltage regulators are used to generate the FPGA core voltage, and video input and output voltages.

There are five power test points on the EVM at TP4, TP8, TP13, TP15, and TP16. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 4: Power Test Points

Test Point	Voltage	Voltage Use
TP4	+1.4 V	DSP Core
TP8	+3.3 V	DSP I/O and logic
TP13	+1.8 V	FPGA
TP15	+3.3 V	Video encoder
TP16	+1.8 V	Video decoder

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320DM642 EVM.

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2.1 EMIF Interfaces

The DM642 incorporates a 64 bit wide external memory interface. Four chip enables divide up the address space and allow for synchronous and asynchronous accesses at 8,16,32, and 64 bits wide. The DM642 EVM uses chip enables CE0, CE1, and CE3. CE0 is routed to 64 bit wide SDRAM bus. CE1 is used for 8 bit Flash, UART, and FPGA functions. CE 3 is set for synchronous functions. Both CE2 and CE3 are routed to the daughter card interface connectors.

Table 1: EMIF Interfaces

Chip Select	Function
CE0	SDRAM bus
CE1	8 bit Flash, UART, FPGA functions
CE2	Daughter Card Interface
CE3	FPGA Sync Registers
	Daughter Card Interface

2.1.1 SDRAM Memory Interface

The DM642 EVM interfaces to 64 bit wide SDRAM bus in the CE0 space. This 32 megabyte SDRAM space is used for program, data, and video storage. The bus uses an external PLL device to operate the SDRAM at 133 megahertz for optimal performance. Refresh for SDRAM is handled automatically by the DM642.

The PLL used for the EMIF is a ICS512. The input clock to this PLL is 25 Megahertz. The table below shows the available frequencies using the 25 Megahertz input clock.

Table 2: PLL Frequencies

S1 Input	S2 Input	Multiplier	Output Frequency
0	0	4x	100 Mhz
0	Open	5.33x	133.25 Mhz *
0	1	5x	125 Mhz
Open	0	2.5x	62.5 Mhz
Open	Open	2x	50 Mhz
Open	1	3.33x	83.25 Mhz
1	0	6x	150 Mhz
1	Open	3x	75 Mhz
1	1	8x	200 Mhz

* Default setting

Strapping resistors R119, R121, R122, and R123 set the inputs for the S0, S1 inputs on the PLL.

The DM642 can be configured as the source of the EMIF clock. The ECLKIN pin is the default on the EVM. However it is possible to operate the EMIF clock as a divider function of the CPU clock. This configuration is done at reset via the ECLKINSEL0 and ECLKINSEL1 pins which are shared with the EMIF address pins EA19, and EA20. The table below shows this configuration.

Table 3: EMIF Interfaces

ECLKINSEL0	ECLKINSEL1	Mode
0	0	ECLKIN *
0	1	CPUCLK/4
1	0	CPUCLK/6
1	1	ECLKIN

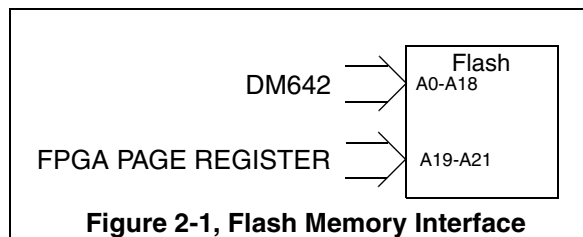
* Default

2.1.2 Flash Memory Interface

The DM642 has 4 megabytes of Flash memory mapped into the lower portion of the CE1 space. This Flash memory is used primarily for boot loading and storage of the FPGA configuration information. The CE1 space is configured as 8 bits wide on the DM642 EVM and the Flash memory is 8 bits wide. The memory address space available in CE1 space is smaller than the size of the Flash so the FPGA is used to create 3 extended page address lines. These extended address lines are addressable via the FPGA Flash Base Register and default to 000 binary at Reset. The addresses and pages are shown in the table below.

Table 4: Flash Memory Interface

Address Range	Page Number	Contents
0x9000 0000 0x9007 FFFF	Page 0	000B
	Page 1	001B
	Page 2	010B
	Page 3	011B
	Page 4	100B
	Page 5	101B
	Page 6	110B
	Page 7	111B



2.1.3 UART Interface

The dual UART (TLC16C752) is memory mapped into the upper half of the DM642's CE1 space along with the FPGA asynchronous registers. Each UART, A and B, occupies 8 locations. CE1 is configured for 8 bit accesses on the DM642 EVM. The addresses are shown in the table below.

Table 5: UART Addresses

UART	Address
A	0x9008 0000 - 0x9008 0007
B	0x9008 0008 - 0x9008 000F

The UARTs interface to the RS-232 line drivers. UART A is brought out to a DB-9 connector, J11, and UART B is routed to a double row header on the board, J12.

2.1.4 FPGA Asynchronous Memory Interface

The FPGA has 10 asynchronous memory registers which reside in the upper portion of the CE1 space. These registers implement various functions listed below. More information is available on these registers in the TMS320DM642 EVM OSD FPGA User's Guide, SPRU295. The addresses and registers are shown in the table below.

Table 6: FPGA Asynchronous Memory Interface

Address	Function	R/W	Bits
0x9008 0010	OSD Control Register	R/W	6
0x9008 0011	DMA Threshold LSB Register	R/W	8
0x9008 0012	DMA Threshold MSB Register	R/W	8
0x9008 0013	Interrupt Status Register	R	7
0x9008 0014	Interrupt Enable Register	R/W	5
0x9008 0015	GPIO Direction Register	R/W	8
0x9008 0016	GPIO Status Register	R/W	8
0x9008 0017	LED Register	R/W	8
0x9008 0018	Flash Page Register	R/W	3
0x9008 0019	Reserved		
0x9008 001A	Reserved		
0x9008 001B	Reserved		
0x9008 001C	Reserved		
0x9008 001D	Reserved		
0x9008 001E	Reserved		
0x9008 001F	FPGA Version Register	R	8

2.1.5 FPGA Synchronous Memory Interface

The FPGA implements synchronous registers in the CE3 space. These registers are used primarily for on screen display functions and some EVM glue functions. A list of the synchronous registers is shown in the table below.

Table 7: FPGA Synchronous Memory Interface

Address	Function	R/W	Bits
0xB000 0000	Synchronous Test Register	R/W	32
0xB000 0004	Audio PLL Data Register	R/W	16
0xB000 0008	OSD XSTART	R/W	12
0xB000 000C	OSD YSTART	R/W	12
0xB000 0010	OSD XSTOP	R/W	12
0xB000 0014	OSD YSTOP	R/W	12
0xB000 0018	Events Per Field	R/W	16
0xB000 001C 0xB000 003C	Reserved	R	32
0xB000 0040	OSD Data FIFO	W	32
0xB000 0044	OSD CLUT	W	32
0xB000 0048 0xB000 007C	Reserved	R	32

2.1.6 EMIF Buffer/Decoder Control

The EMIF buffer and decode functions are implemented with a GAL16LV8D generic array logic device, U15. the device performs basic decode for the flash and UART along with buffer control for CE1, CE2, and CE3. The VHDL is shown below.

```
FLASH_CE <= '0' when A22 = '0' and CE1 = '0' else '1';

UART_CSA <= '0' when A22 = '1' and A8 = '0' and A7 = '0'
           and A6 = '0' and CE1 = '0' else '1';

UART_CSB <= '0' when A22 = '1' and A8 = '0' and A7 = '0'
           and A6 = '1' and CE1 = '0' else '1';

EMIF_OE  <= '0' when CE1 = '0' or CE2 = '0' or CE3 = '0' else '1';

EMIF_DIR <= '1' when (CE1 = '0' and AOE = '0') or
                   (CE2 = '0' and AOE = '0') or
                   (CE3 = '0' and AOE = '0') else '0';
```


2.2 Video Port/McASP Interfaces

The DM642 has three on chip video ports. These ports can be subdivided to allow optional functions such as an McASP or SPDIF on ports 0 and 1. The DM642 EVM uses all three of these video ports. Video Port 0 and Video Port 1 are used for capture ports and Video Port 2 is used as a display port. In the standard EVM configuration, the Video Port 0 and Video Port 1 are programmed to be subdivided to allow the McASP function to be implemented and interface to an TLV320AIC23B stereo Codec, or to interface to SPDIF output J9.

2.2.1 Video Decoder Ports

On the DM642 EVM the subdivided Video Port 0 and Video Port1 are used as capture inputs, capture port 1 and capture port 2. These ports interface to TI TVP5416 and TVP5150A video decoders. The Video Ports are run through CBT switches so that they can be selectively disabled for daughter card use. The other half of the ports are used for on board McASP interface. The capture port 1 interfaces to video sources via an RCA style video jack J15 and four pin S-Video mini-din connector J16. The input should be a composite video source such as a DVD player or a video camera. The decoders are programmable via the DM642's I²C bus and can interface to all major composite video standards such as NTSC, PAL, and SECAM by appropriately programming the internal registers in the decoder.

2.2.2 Video Encoder Port

The DM642's Video Port 2 is used to drive the video encoder. It is routed through the FPGA U8 to implement advanced functions such as On Screen Display, but the default mode is to pass the video directly to the Phillips SAA7105 video encoder. The encoder can drive out either RGB, HD component video, NTSC/PAL composite video, or S-video depending on how the internal registers of the SAA7105 are programmed. The SAA7105 is configured by programming the internal registers via the DM642's I2C bus.

The encoder interfaces to composite or RGB display units. Standard Video RCA jacks provide RGB on J2,J3, and J4. J3 the green output can also be used for interfacing to composite display units. An S-Video 4 pin Mini Din J1 is also available. A 15 pin High Density DB connector J5 allows the EVM to drive VGA type monitors.

The DM642 EVM supports High Definition TV output but requires some filter changes as specified in the section under HDTV support.

2.2.3 FPGA Video Functions

The DM642 EVM uses a Xilinx XC2S300E series FPGA to implement enhanced video functions along with some other glue functions. In default mode the FPGA passes the video from the DM642's Video Port 2 to the Phillips SAA7105 Video Encoder. For HDTV the FPGA provides enhanced clocking and for on screen display functions the FPGA has FIFOs to mix the Video Port 2 data with the data from these internal FIFOs. The FIFO's in the FPGA are accessed via the DM642's EMIF in synchronous mode via the CE3 space. For more information on the implementation of the FPGA functions, the user should reference the document SPRU295, TMS320DM642 EVM OSD FPGA User's Guide.

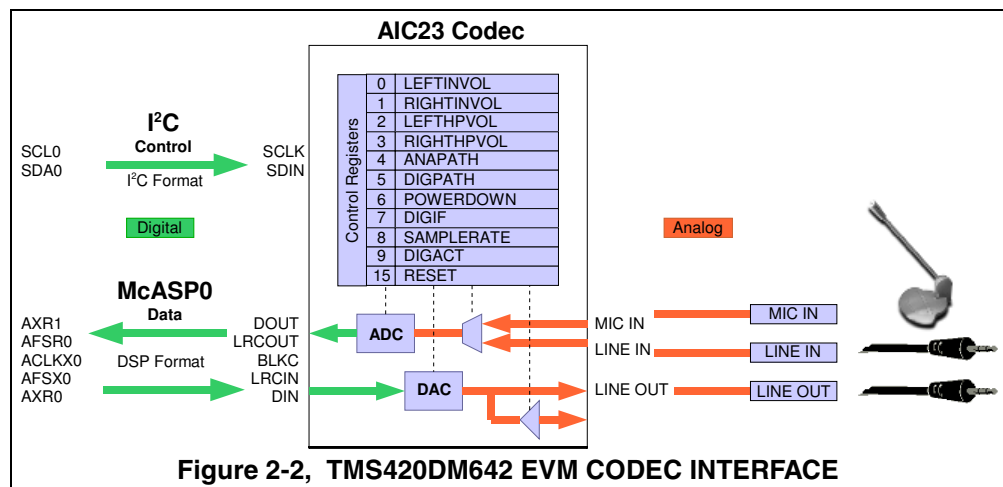
2.2.4 AIC23B Interface

The EVM uses a Texas Instruments AIC23B (P/N TLV320AIC23B) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I²C bus is used as the unidirectional control channel. The control channel is only used when configuring the codec, it is generally idle when audio data is being transmitted,

McASP is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which matches the McASP's burst mode.

The codec has a programmable clock from a PLL1708 PLL device. The default system clock is 18.432 Mhz. The internal sample rate generate subdivides the 18.432 MHz clock to generate common frequencies such as 48KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the codec interface on the DM642 EVM.



2.2.5 Audio PLL/VCXO Circuit/PLL1708 Clock Generator

The DM642 EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

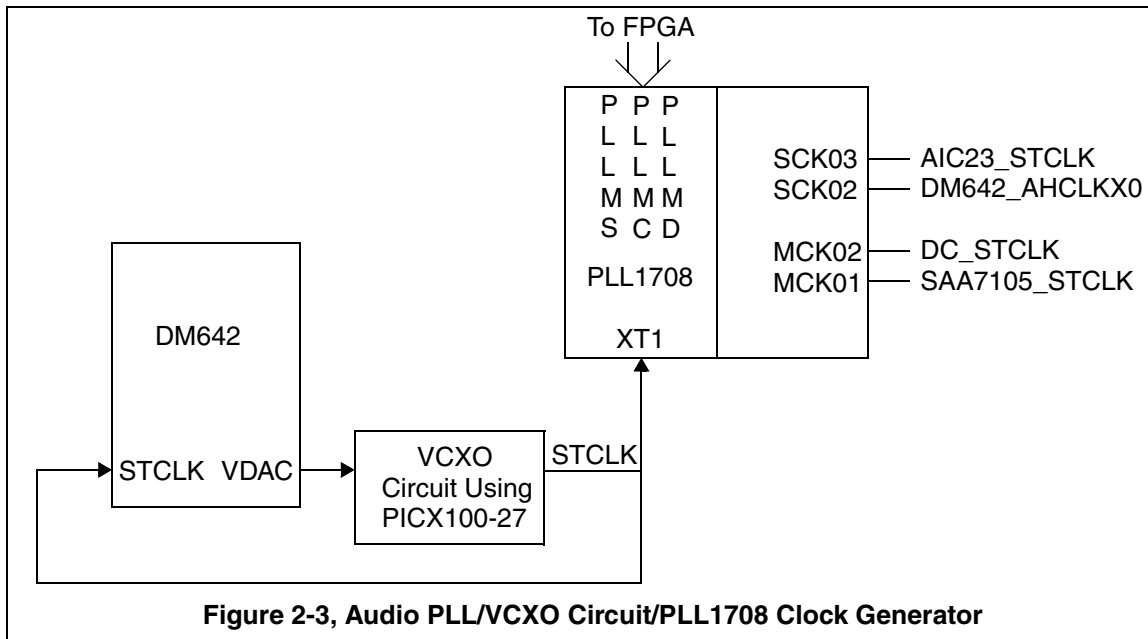
In streaming video applications the audio and video sequences can lose synchronization. The DM642 uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The STCLK is used to implement this feature and is created by the DM642's VDAC pin during a PICX100-27W Voltage Controlled Oscillator. The VDAC pin is controlled via internal DM642 registers.

The STCLK is also a source clock for the PLL1708 programmable PLL device. This device creates the clocks for the AIC23B Codec, SPDIF, daughter card STCLK and optional encoder clocking.

The PLL1708 is programmable via the PLL Data Register in the FPGA which serializes the user data to the proper format required by the PLL1708.

The diagram below is a simplified diagram of this clocking scheme.



2.3 PCI/HPI/Ethernet Interfaces

The DM642 supports a wide variety of peripheral interfaces. The DSP multiplexes a PCI bridge, host port interface, and ethernet MAC. The DM642 EVM supports all of these interfaces.

2.3.1 PCI Interface

The DM642 directly supports a PCI interface. Cross Bar Technology (CBT) mux and switches are used to separate the PCI bus from the DM642 so that the EVM can support both the PCI interface or ethernet interface. The CBT's also provide +5 volt interface logic support for the PCI interface.

The CBT's are automatically configured for PCI operation when the board is plugged into a PCI slot via the PCI-Detect signal

2.3.2 PCI EEPROM Interface

The DM642 EVM supports an external EEPROM which holds optional PCI configuration values when enabled. The EEPROM is enabled from configuration switch S2. When S2-1 is "on" the PCI configuration uses the EEPROM parameters for configuration. If S2-1 is "off", the internal DM642 default registers are used for configuration. The table below shows the contents of the EEPROM when shipped from the factory.

Table 8: EEPROM Memory Map

Address	Value	Description of Contents
0x00	0x104C	Vendor ID
0x01	0x9065	Device ID
0x02	0x0000	Calls Code [7:0]/Revision ID
0x03	0xFF00	Class Code [23:8]
0x04	0x1652	Subsystem Vendor ID
0x05	0x0642	Subsystem ID
0x06	0x0000	Max_Latency/Min_Grant
0x07	0x0000	PC_D1/PC_D0 Power Consumed
0x08	0x0000	PC_D3/PC_D2 Power Consumed
0x09	0x0000	PD_D1/PC_D0 Power Dissipated
0x0A	0x0000	PD_D3/PC_D2 Power Dissipated
0x0B	0x0000	Data_Scale (PD_D3 ... PC_D0)
0x0C	0x0000	0000 0000 PMC[14:9], PMC[5], PMC[3]
0x00D	0xC593	Checksum

2.3.3 Ethernet Interface

In a standalone mode the DM642 ethernet MAC is automatically selected, and routed to the PHY via CBT muxes. The EVM DM642 uses an Intel LXT971 PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, J8. The PHY directly interfaces to the DM642. The ethernet address is stored in the I²C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.3.4 HPI Interface

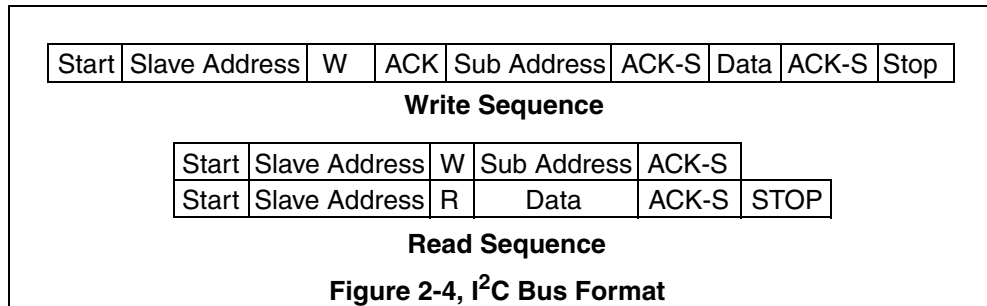
The DM642 is equipped with a host port that supports multiplexed or non-multiplexed accesses. The EVM supports Host Port Interface accesses via the PCI Connector. The signals for the DM642's HPI port are brought out to the PCI connectors and the user can interface to them via these connectors. The table in Section 3 enumerates the signals used for HPI accesses. The EVM automatically enables the EMAC when the EVM is not inserted into a PC. Furthermore, it drives the PCI_EN pin on the DM642 Low disabling the PCI bus.

The HPI width signal is controlled at reset by the HD05/HWDTHSEL pin on the DM642. The default width is 16 bit mode. There are 2 strapping resistors R206 and R207 which allow the user to change the default mode for the HPI width.

When using 32 bit HPI mode the EMAC needs to be disabled, so the user will need to ground B3 on the PCI forcing PCI_DETECT# low (installing R250 will also force PCI_DETECT# low) which automatically disables the EMAC, and allows all 32 bits of access to be enabled. However, to force the PCI_EN pin on the DM642 low, R249 needs to be removed.

2.4 I²C Interface

The I²C bus on the DM642 is ideal for interfacing to the control registers of many devices. On the DM642 EVM the I²C bus is used to configure the video encoder, video decoders, and stereo Codec. An I²C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.



The addresses of the on board peripherals are shown in the table below.

Table 9: I²C Memory Map

Device	Address	R/W	Function
TVP5146	0xBA	R/W	Capture 1 Decoder
TVP5150A	0xB8	R/W	Capture 2 Decoder
SAA7105	0x88	R/W	Encoder
TLV320AIC23B	0x1A	R/W	CODEC
24WC256	0x50	R/W	I ² C EEPROM

2.5 SPDIF Interface

The McASP pins on the DM642 can be configured to operate as a SPDIF transmitter. The DM642 EVM supports a single SPDIF output which is routed to RCA jack, J9. The SPDIF output pin is routed to a driver and filter circuit. When the SPDIF interface is enabled the TLV320AIC23B codec is disabled.

2.6 Daughter Card Interface

The EVM provides three expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory, peripherals, and video port expansion.

The pin outs for this interface are documented in Section 3. For more detailed information on daughter card designs please refer to Texas Instrument's document SPRA920, the DM642 EVM Daughter Card Interface Specification.

The memory connector provides access to the DSP's EMIF signals to interface with memories and memory mapped devices. It supports byte addressing on 32 bit boundaries. The signals on this bus are buffered.

The video ports are brought out to the daughter card interface. Four signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 10: Daughter Card Video Enable

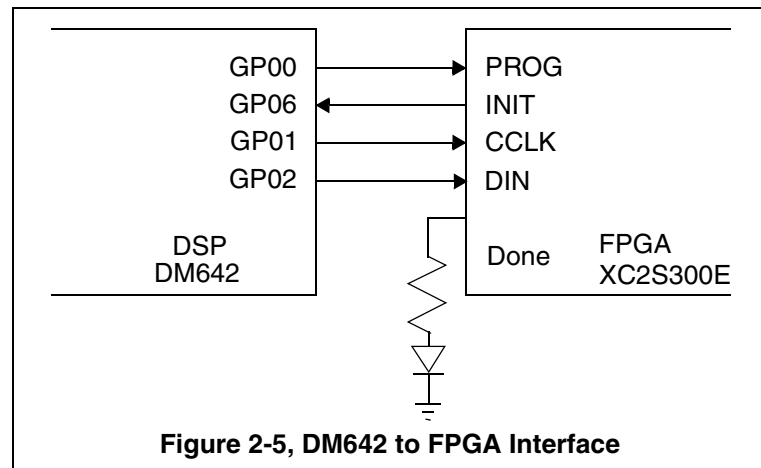
Signal	State To Enable Daughter Card Use	DM642 Signals Enables
EXP_CAPTURE1_EN	1	Video Port 0 Data 0-11 All Video Port 0 Control
EXP_CAPTURE2_EN	1	Video Port 1 Data 0-11 All Video Port 1 Control
EXP_AUDIO_EN	1	Video Port 0 Data 12-19 Video Port 1 Data 12-19
EXP_DISPLAY_EN	1	Video Port 0 Data 0-19 All Video Port 2 Control

Other than the buffering, most daughter card signals are not modified on the board.

2.7 Programming the FPGA

The FPGA on the DM642 EVM is programmed via the DSP. The Xilinx XC2S300 FPGA supports a serial programming interface and the DM642 EVM uses this serial interface to program the on board FPGA.

In standard configuration the FPGA contents are stored in the upper half of Flash page 0. The lower half of Flash Page 0 contains the code loaded by the internal boot loader. This code is loaded at reset and programs the on board FPGA. The DM642 interface to the FPGA is shown below.



2.8 DM642 Core CPU Clock

The DM642 EVM uses a 60 Megahertz oscillator to generate the input clock CLKIN. The DM642 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via the CLKMODE0 and CLKMODE1 pins on the DM642 device. At reset these pins are sampled, and this determines the PLL multiplier for the internal CPU clock. The strapping of these pins is done with discrete resistors on the EVM, reference designators R171, R172, R203 and R205.

The table below specifies the available PLL multipliers.

Table 11: DM642 Core CPU Clock

CLKMODE1	CLKMODE0	PLL Multiplier	Frequency
0	0	Bypass	60 Mhz
0	1	CLKIN times 6	360 Mhz
1	0	CLKIN times 12 *	720 Mhz
1	1		Reserved

* Default

2.9 HDTV Implementation

Version 3 of the DM642 EVM is shipped with High Definition output filter installed. For most applications this improves quality and appearance. Since the bandwidth requirements for High Definition TV are greater than standard Definition TV, at times to meet Standard Definition application specifications a lower resolution frequency may be necessary. The diagrams below indicate the procedure for qualified personnel to implement this conversion. Included below is a list of suggested components required to implement this procedure.

The figure below indicates the position of the components to be modified.

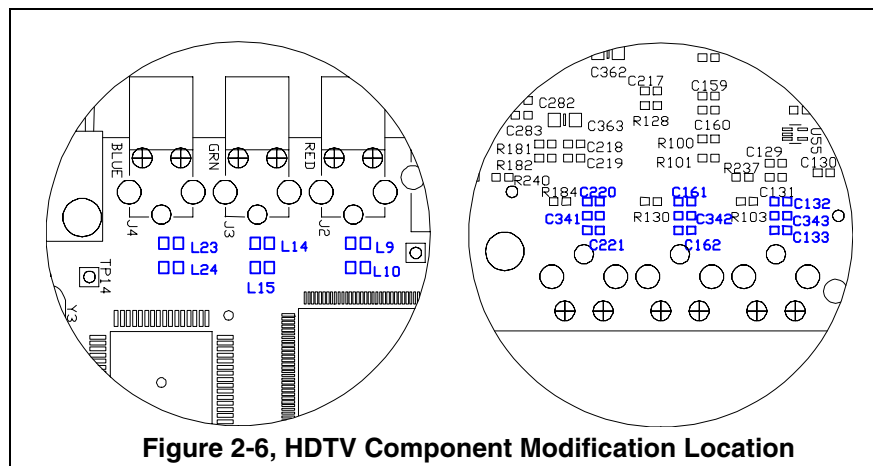


Figure 2-6, HDTV Component Modification Location

The sequence to update the EVM is:

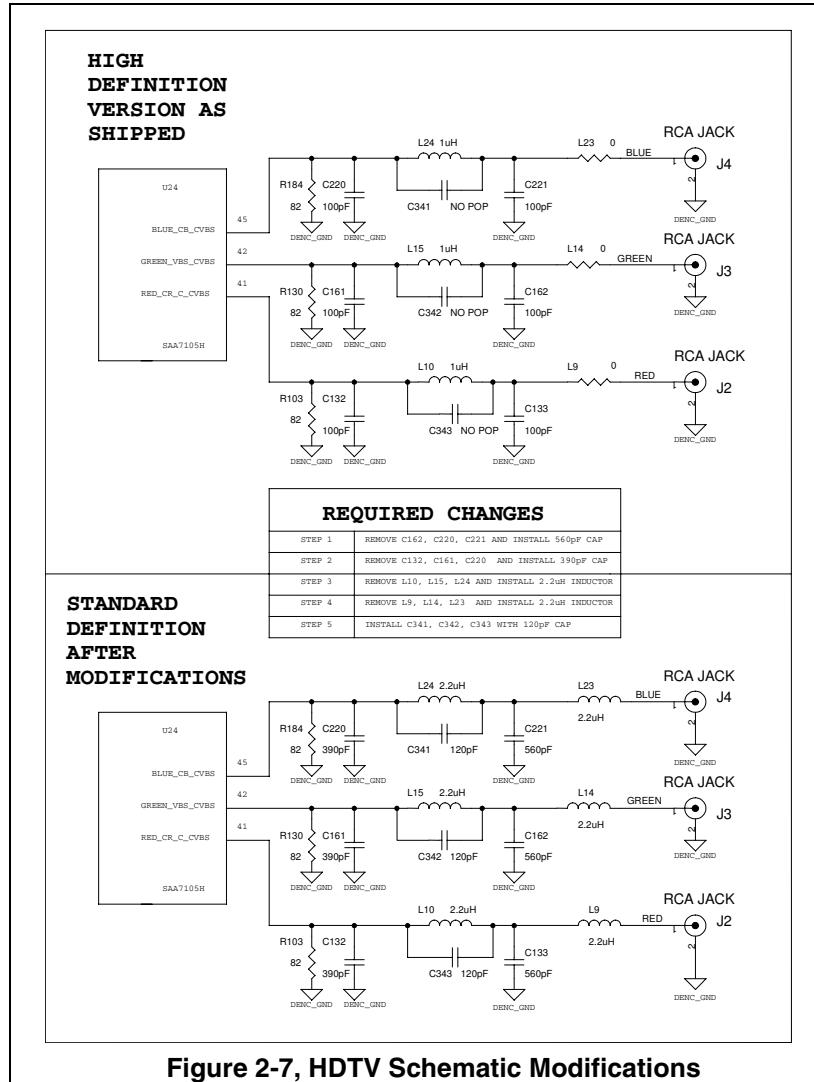
1. Remove C133, C162, and C221. Replace with 560pF capacitors.
2. Remove C132, C161, and C220, Replace with 390pF capacitors.
3. Remove L10, L15, and L24. Replace with 2.2uH inductors
4. Remove L14, L19, and L23. Replace with 2.2uH inductors
5. Install 120pF capacitors at C341, C342, and C343.

The table below shows the suggested component list.

Table 12: Suggested Component List

Device	Component Number	Qty	Manufacturer's Part #
560pF capacitor	C133, C162, C221	3	Panasonic ECU-V1H561KBV
390pF capacitor	C132, C161, C220	3	Panasonic ECU-V1H391KBV
120pF capacitor	C341, C342, C343	3	Panasonic ECU-V1H121KBV
2.2uH inductor	L10, L14, L15, L19, L23, L24	6	Panasonic ELJ-FD2R2KF

The figure below shows a section of the schematic for the encoder output prior to and after modification. The sequence is outlined.



Chapter 3

Physical Description

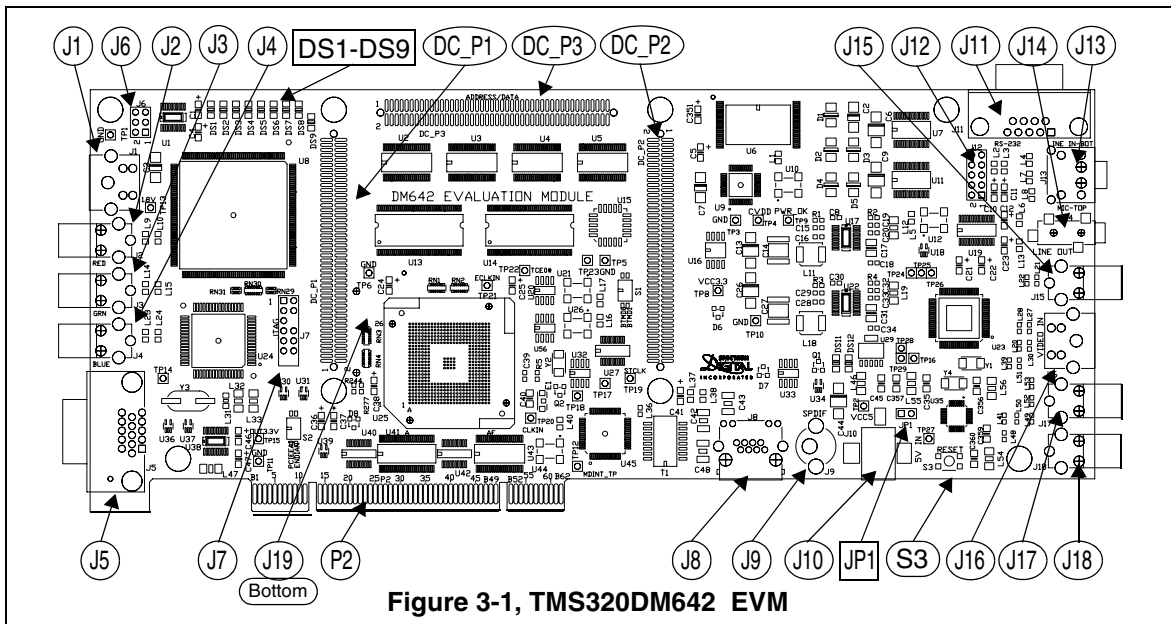
This chapter describes the physical layout of the TMS320DM642 EVM and its connectors.

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3.1 Board Layout

The DM642 EVM is a 8.75 x 4.5 inch (210 x 115 mm.) multi-layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the DM642 EVM.



3.2 Connectors

The TMS320DM642 EVM has 24 connectors which provide the user access to the various signals on the EVM.

Table 1: TMS320DM642 EVM Connectors

Connector	# Pins	Function
J1	4	S-Video Out
J2	2	Video Out -Red
J3	2	Video Out - Green
J4	2	Video Out - Blue
J5	15	VGA Video Out
J6	6	FPGA Optional JTAG Programmer Header
J7	14	JTAG
J8	8	Ethernet
J9	3	SPDIF
J10	2	+5 Volts In
J11	9	RS-232
J12	10	RS-232
J13	2	Microphone/ Audio Line In
J14	2	Audio Line Out
J15	2	Composite Video In
J16	4	S-Video In
J17	2	Composite Video In
J18	2	Composite Video In
J19	60	60 Pin Emulation header (bottom side)
JP1	2	Optional Reset Header
P2	124	PCI Bus Connector
DC_P1	80	Video Port 2/Misc Expansion
DC_P2	80	Video Port 0/Video Port 1 Expansion
DC_P3	80	EMIF Expansion

3.2.1 J1, S-Video Out Connector

J1 is a four pin mini din connector which interfaces to an output display device. The connector is driven directly by the Philips SAA7105 video encoder. The pin out is the connector is shown below.

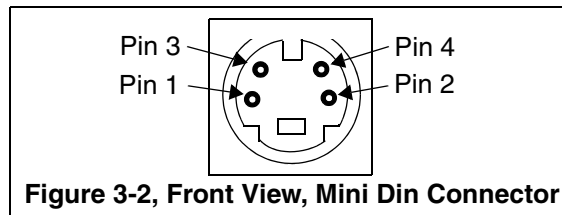
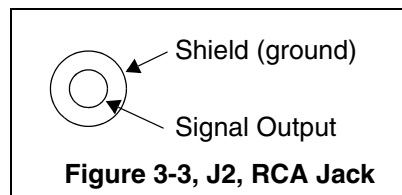


Table 2: J1, Mini Din Connector

Pin #	Signal Name
1	Ground
2	Ground
3	Luma (Y)
4	Chroma (C)

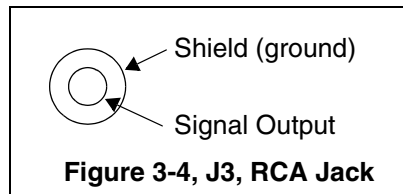
3.2.2 J2, Video Out - RED and Pr

J2 is a RCA jack which drives the RED signal when the encoder is in the R-G-B mode. This output is also used in HDTV mode to drive the Pr component of the video. The pinout of this connector is shown below.



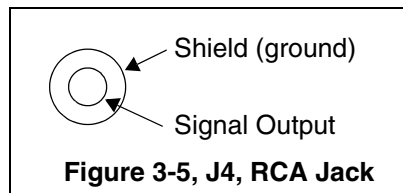
3.2.3 J3, Video Out - Green and Y

J3 is an RCA jack used to interface to the GREEN or composite video of the display device. This connector is driven directly by the Philips SAA7105 video encoder. This output is also used in HDTV mode to drive the Y component of the video. The pinout of this connector is shown below.



3.2.4 J4, Video Out - Blue and Pb

J4 is an RCA jack used to interface to the Blue of an RGB device. This connector is driven directly by the Philips SAA7105 video encoder. This output is also used in HDTV mode to drive the Pb component of the video. The pinout of this connector is shown below.



3.2.5 J5, PC Video Output Connector

Connector J5 provides the standard personal computer monitor video output 15 pin high density female D-connector. The signals on the pins are shown in the table below.

Table 3: J5, PC Video Output Connector

Pin #	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	Key
10	Ground
11	No connect
12	No connect
13	Horizontal Sync
14	Vertical sync
15	No Connect

3.2.6 J6, FPGA Programming Connector

Connector J6 is 2 x 3 double row header allowing JTAG programming the FPGA, U8. The signals on the pins are shown in the table below. This interfaces to a Xilinx programming pod.

Table 4: J6, FPGA Programming Connector

Pin #	Signal Name
1	+3.3 Volts
2	Ground
3	FPGA-TCK
4	FPGA-TDI
5	FPGA-TDO
6	FPGA-TMS

3.2.7 J7, JTAG Interface

The TMS320DM642 EVM is supplied with a 14 pin header interface, J7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown in the figure below.

TMS	1	2	TRST-	Header Dimensions Pin-to-Pin spacing, 0.100 in. (X,Y) Pin width, 0.025-in. square post Pin length, 0.235-in. nominal
TDI	3	4	GND	
PD (+3.3V)	5	6	no pin (key)	
TDO	7	8	GND	
TCK-RET	9	10	GND	
TCK	11	12	GND	
EMU0	13	14	EMU1	

Figure 3-6, JTAG INTERFACE

3.2.8 J8, Ethernet Connector

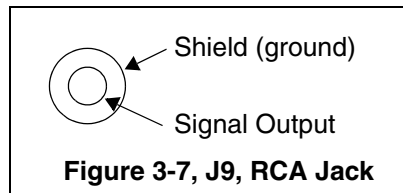
Connector J8 is a standard RJ-45 ethernet connector. The connector pin out is shown

Table 5: J8 Connector Pin Out

Pin #	Signal Name
1	LXT TXD
2	LXT TXM
3	LXT RXP
4	Terminator 1
5	Terminator 2
6	LXT RXM
7	Terminator 3
8	Terminator 4

3.2.9 J9, Expansion Connector

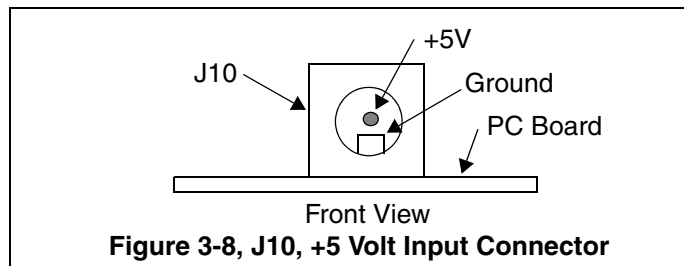
The DM642 has the ability to drive SPDIF audio outputs from its on chip McASP when in the SPDIF mode. The output is buffered and driven to J9 as a vertically mounted RCA jack. The pinout of this connector is shown below.



3.2.10 J10, +5 Volt Input Connector

The DM642 EVM can be powered either standalone or from the PCI bus. The input supply is +5 volts only.

In the standalone mode power (+5 volts) is brought onto the TMS320DM642 EVM via connector J10. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J10 is shown below.



3.2.11 J11, J12, RS-232 Connectors

The DM642 has an on board TLC16C752 dual UART. UART A is buffered with a MAX3243 RS-232 line driver and is routed to a male 9 pin D-connector, J11. UART B is buffered with a MAX 3243 RS-232 line driver and routed to a 5 x 2 dual row header, J12. The pin positions for the P11 connector as viewed from the edge of the printed circuit board are shown below.

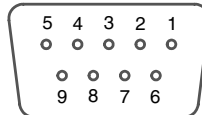


Figure 3-9, J11, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 6: J11, RS-232 Pinout

Pin #	Signal Name	Direction
1	DCD	In
2	RXD	In
3	TXD	Out
4	DTR	Out
5	GND	N/A
6	DSR	In
7	RTS	Out
8	CTS	In
9	RI	In

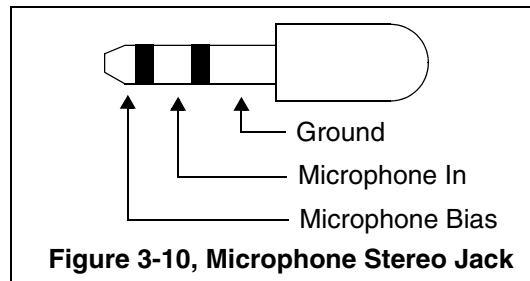
The pin numbers for J12 and their corresponding signals are shown in the table below.

Table 7: J12, 5 x 2 Pinout

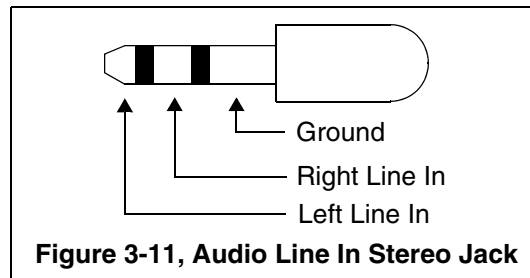
Pin #	Signal Name	Direction	Pin #	Signal Name	Direction
1	DCD	In	2	RXD	In
3	TXD	Out	4	DTR	Out
5	GND	N/A	6	DSR	In
7	RTS	Out	8	CTS	In
9	RI	In	10	Not Used	N/A

3.2.12 J13, Microphone/Audio Input Connector

Connector J13 is the audio line input and the microphone input. The microphone input is a 3.5 mm. stereo jack located at the top position of J13. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

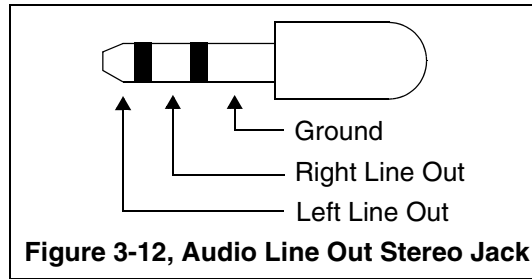


The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack located at the bottom position of J13. The signals on the mating plug are shown in the figure below.



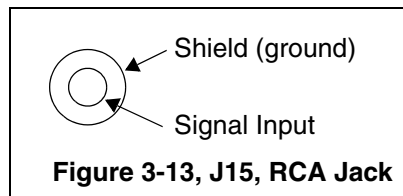
3.2.13 J14, Audio Line Output Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.



3.2.14 J15, Capture Port 1 Video Input Connector

J15 is an RCA jack used to capture composite video for capture channel 1. This connector is driven directly into the TI TVP5146 video decoder. The pinout of this connector is shown below.



3.2.15 J16, Capture Port 1 S-Video Input Connector

J16 is a four pin mini din connector which interfaces to an S-video input for capture channel 1. The connector is driven directly into the TI TVP5146 video decoder. The pin out of the connector is shown below.

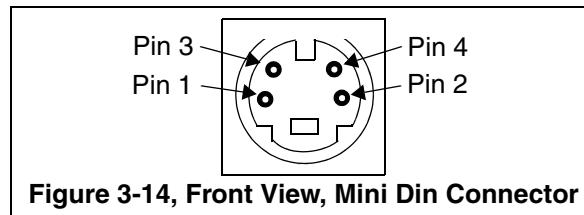
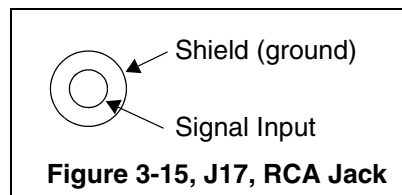


Table 8: J1, Mini Din Connector

Pin #	Signal Name
1	Ground
2	Ground
3	Luma (Y)
4	Chroma (C)

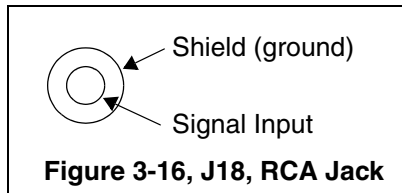
3.2.16 J17, Capture Port 2 Video Input Connector

J17 is an RCA jack used to interface composite video source to capture channel 2. This connector is driven directly into the TI TVP5150A video decoder. The pinout of this connector is shown below.



3.2.17 J18, Capture Port 2 Optional Video Input Connector

J18 is an RCA jack used to interface composite video source to capture channel 2. This connector is driven directly into the TI TVP5150A video decoder. The pinout of this connector is shown below.



3.2.18 J19, 60 Pin Emulation Connector

The 60 pin emulation connector is mounted on the bottom side of the DM642 circuit card. This connector is for advanced emulation capability. The signals on this connector are 4 columns by 15 rows as shown in the table below

Table 9: J19, 60 Pin Emulation Connector

Row #	Column A Signal Name	Column B Signal Name	Column C Signal Name	Column D Signal Name
1	Ground	IDO	ID2	Ground
2	Ground	TMS	EMU18	Ground
3	Ground	EMU17	TRSTn	Ground
4	Ground	TDI	EMU16	Ground
5	Ground	EMU14	EMU15	Ground
6	Ground	EMU12	EMU13	Ground
7	Ground	TDO	EMU11	Ground
8	TYPE0	TVD	TCLKRTN	TYPE1
9	Ground	EMU9	EMU10	Ground
10	Ground	EMU7	EMU8	Ground
11	Ground	EMU5	EMU6	Ground
12	Ground	TCLK	EMU4	Ground
13	Ground	EMU2	EMU3	Ground
14	Ground	EMU0	EMU1	Ground
15	Ground	ID1	ID3	Ground

3.2.19 J20, P2 PCI Connector

The P2 connector is a card edge PCI interface. This connector has an “A” and “B” side. Because of the card seating notches the pin numbers are not contiguous. The “B” side is the top component side. The I/O direction field is referenced from the PCI slot.

Table 10: P2, PCI Connector, “A” Side

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	TRST-		Not Used	2	+12 Volts		Not Used
3	TMS		Not Used	4	TDI	I/O	Tied to TDO
5	+5 Volts		+5 Volts Power	6	INTA	O	Interrupt Out
7	INTC	O	Interrupt Out	8	+5 Volts		+5 Volts Power
9	Rsvd		Not Used	10	+V I/O		Not Used
11	Rsvd		Not Used	12	Key		Key
13	Key		Key	14	+3.3 Volts		Not Used
15	RST	I	PCI_Resetn	16	+V I/O	O	Not Used
17	GNT-	O	Grant-	18	GND		Ground
19	PME-			20	AD30	I/O/Z	Address/Data 30
21	+3.3 Volts		Not Used	22	AD28	I/O/Z	Address/Data 28
23	AD26	I/O/Z	Address/Data 26	24	GND		
25	AD24	I/O/Z	Address/Data 24	26	IDSEL	I	Initialization Device Select
27	+3.3 Volts		Not Used	28	AD22	I/O/Z	Address/Data 22
29	AD20	I/O/Z	Address/Data 20	30	GND		Ground
31	AD18	I/O/Z	Address/Data 18	32	AD16	I/O/Z	Address/Data 16
33	+3.3 Volts		Not Used	34	FRAME-	I	Frame
35	GND		Ground	36	TRDY-	I/O/Z	Target Ready
37	GND		Ground	38	STOP-	I/O/Z	Stop Direction
39	+3.3 Volts		Not Used	40	SDONE	O	Done
41	SBO-			42	GND		Ground
43	PAR	I/O/Z	Parity	44	AD15	I/O/Z	Address/Data 15
45	+3.3 Volts		Not Used	46	AD13	I/O/Z	Address/Data 13
47	AD11	I/O/Z	Address/Data 11	48	GND		Ground
49	AD9	I/O/Z	Address/Data 9	50	Key		Key
51	Key		Key	52	C/BE0		Command/Byte Enable0
53	+3.3 Volts		Not Used	54	AD6	I/O/Z	Address/Data 6
55	AD4	I/O/Z	Address/Data 4	56	GND		Ground
57	AD2	I/O/Z	Address/Data 2	58	AD0	I/O/Z	Address/Data 0
59	+V I/O		Not Used	60	REQ64-		Not Used
61	+5 Volts		+5 Volts Power	62	+5 Volts		+5 Volts Power

The signals on the “B” side of the connector are shown in the table below.

Table 11: P2, PCI Connector, “B” Side

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	-12 Volts		Not Used	2	TCK	I	Not Used
3	GND		Ground	4	TDO	I	Tied to TDO
5	+5 Volts		+5 Volt Power	6	+5 Volts	I	+5 Volt Power
7	INTB-		Interrupt OUT	8	INTD-		Interrupt Out
9	PRSNT1-	O	Power Requirement	10	Rsvd		
11	PRSNT2-	O	Power Requirement	12	Key		Key
13	Key		Key	14	Rsvd		
15	GND		Ground	16	CLK		System Clock
17	GND		Ground	18	REQ-		
19	+V I/O		Not Used	20	AD31	I/O/Z	Address/Data 31
21	AD29	I/O/Z	Address/Data 29	22	GND		Ground
23	AD27	I/O/Z	Address/Data 27	24	AD25	I/O/Z	Address/Data 25
25	+3.3 Volts		Not Used	26	C/BE3	I/O/Z	Command/Byte Enable 3
27	AD23	I/O/Z	Address/Data 23	28	GND		Ground
29	AD21	I/O/Z	Address/Data 21	30	AD19	I/O/Z	Address/Data 19
31	+3.3 Volts		Not Used	32	AD17	I/O/Z	Address/Data 17
33	C/BE2	I/O/Z	Command/Byte Enable 2	34	GND		Ground
35	IRDY-	I	Initiator Ready	36	+3.3 Volts		Not Used
37	DEVSEL-	I/O/Z	Device Select	38	GND		Ground
39	LOCK-	I	Resource Locked	40	PERR	I/O/Z	Parity Error
41	+3.3 Volts		Not Used	42	SERR	O	System Error
43	+3.3 Volts		Not Used	44	C/BE1	I/O/Z	Command/Byte Enable 1
45	AD14	I/O/Z	Address/Data 14	46	GND		Ground
47	AD12	I/O/Z	Address/Data 12	48	AD10	I/O/Z	Address/Data 10
49	M66EN	O	66 Mhz Enable	50	Key		Key
51	Key		Key	52	AD8	I/O/Z	Address/Data 8
53	AD7	I/O/Z	Address/Data 7	54	+3.3 Volts		Not Used
55	AD5	I/O/Z	Address/Data 5	56	AD3	I/O/Z	Address/Data 3
57	GND		Ground	58	AD1	I/O/Z	Address/Data 1
59	+V I/O		Not Used	60	ACK64-		Not Used
61	+5 Volts		+5 Volt Power	62	+5 Volts		+5 Volt Power

3.2.20 DC_P1, Video Port 2/Expansion

Table 12: DC_P1, Video Port 2/Expansion

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	DSP_GPIO_3	I/O/Z	DSP GPIO3	2	DSP_EXTINT4	I/O/Z	DSP Interrupt 4
3	GND		System Ground	4	DSP_EXTINT5	I/O/Z	DSP Interrupt 5
5	DSP_NMI#	I	DSP NMI Interrupt	6	GND		System Ground
7	GND		System Ground	8	DSP_TINP1	I	DSP Timer In 1
9	DSP_TINP0	I	DSP Timer In 0	10	DSP_TOUT1	I/O/Z	DSP Timer Out 1
11	DSP_TOUT0	I/O/Z	DSP Timer Out 0	12	GND		System Ground
13	GND		System Ground	14	EXP_DISPLAY_EN#	I	Disable On Board Display
15	VP2CLK1	I/O/Z	Video Port 2 Clock 1	16	GND		System Ground
17	GND		System Ground	18	GND		System Ground
19	VP2D18	I/O/Z	Video Port 2 D18	20	VP2D19	I/O/Z	Video Port 2 D19
21	VP2D16	I/O/Z	Video Port 2 D16	22	VP2D17	I/O/Z	Video Port 2 D17
23	VP2D14	I/O/Z	Video Port 2 D14	24	VP2D15	I/O/Z	Video Port 2 D15
25	GND		System Ground	26	GND		System Ground
27	VP2D12	I/O/Z	Video Port 2 D12	28	VP2D13	I/O/Z	Video Port 2 D13
29	VP2D10	I/O/Z	Video Port 2 D10	30	VP2D11	I/O/Z	Video Port 2 D11
31	GND		System Ground	32	GND		System Ground
33	VP2D8	I/O/Z	Video Port 2 D8	34	VP2D9	I/O/Z	Video Port 2 D9
35	VP2D6	I/O/Z	Video Port 2 D6	36	VP2D7	I/O/Z	Video Port 2 D7
37	VP2D4	I/O/Z	Video Port 2 D4	38	VP2D5	I/O/Z	Video Port 2 D5
39	GND		System Ground	40	GND		System Ground
41	VP2D2	I/O/Z	Video Port 2 D2	42	VP2D3	I/O/Z	Video Port 2 D3
43	VP2D0	I/O/Z	Video Port 2 D0	44	VP2D1	I/O/Z	Video Port 2 D1
45	GND		System Ground	46	GND		System Ground
47	VP2CLK0	I/O/Z	Video Port 2 Clock 0	48	GND		System Ground
49	GND		System Ground	50	GND		System Ground
51	VP2CTL0	I/O/Z	Video Port 2 Control 0	52	VP2CTL1	I/O/Z	Video Port 2 Control 1
53	VP2CTL2	I/O/Z	Video Port 2 Control 2	54	GND		System Ground
55	GND		System Ground	56	GND		System Ground
57	DSP_SCL0	O/Z	I ² C Clock	58	USER_GPIO_7	I/O	FPGA User I/O 7
59	DSP_SDA0	I/O/Z	I ² C Data	60	USER_GPIO_6	I/O	FPGA User I/O 6
61	GND		System Ground	62	GND		System Ground
63	USER_GPIO_4	I/O	FPGA User I/O 4	64	USER_GPIO_5	I/O	FPGA User I/O 5
65	USER_GPIO_2	I/O	FPGA User I/O 2	66	USER_GPIO_3	I/O	FPGA User I/O 3
67	USER_GPIO_0	I/O	FPGA User I/O 0	68	USER_GPIO_1	I/O	FPGA User I/O 1
69	GND		System Ground	70	GND		System Ground
71	GND		System Ground	72	GND		System Ground
73	VCC3.3	O	Power +3.3 Volts	74	VCC3.3	O	Power +3.3 Volts
75	VCC3.3	O	Power +3.3 Volts	76	VCC3.3	O	Power +3.3 Volts
77	VCC3.3	O	Power +3.3 Volts	78	VCC3.3	O	Power +3.3 Volts
79	GND		System Ground	80	GND		System Ground
81	GND		System Ground	82	GND		System Ground
83	GND		System Ground	84	GND		System Ground
85	VCC5	O	Power +5 Volts	86	VCC5	O	Power +5 Volts
87	VCC5	O	Power +5 Volts	88	VCC5	O	Power +5 Volts
89	VCC5	O	Power +5 Volts	90	VCC5	O	Power +5 Volts

3.2.21 DC_P2, Video Port0 and Video Port 1 Expansion

Table 13: DC_P2, Video Port0 and Video Port1 Expansion

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	SYSTEM RESET#	O	Reset	2	EXP_CAPTURE1_EN#	I	Disable On Board Capture 1
3	EXP_AUDIO_EN#	I	Disable On Board Audio	4	EXP_CAPTURE2_EN#	I	Disable On Board Capture 2
5	GND		System Ground	6	GND		System Ground
7	VP0D0	I/O/Z	Video Port 0 D0	8	VP0D1	I/O/Z	Video Port 0 D1
9	VP0D2	I/O/Z	Video Port 0 D2	10	VP0D3	I/O/Z	Video Port 0 D3
11	GND		System Ground	12	GND		System Ground
13	VP0D4	I/O/Z	Video Port 0 D4	14	VP0D5	I/O/Z	Video Port 0 D5
15	VP0D6	I/O/Z	Video Port 0 D6	16	VP0D7	I/O/Z	Video Port 0 D7
17	VP0D8	I/O/Z	Video Port 0 D8	18	VP0D9	I/O/Z	Video Port 0 D9
19	GND		System Ground	20	GND		System Ground
21	VP0D10	I/O/Z	Video Port 0 D10	22	VP0D11	I/O/Z	Video Port 0 D11
23	VP0D12	I/O/Z	Video Port 0 D12	24	VP0D13	I/O/Z	Video Port 0 D13
25	GND		System Ground	26	GND		System Ground
27	VP0D14	I/O/Z	Video Port 0 D14	28	VP0D15	I/O/Z	Video Port 0 D15
29	VP0D16	I/O/Z	Video Port 0 D16	30	VP0D17	I/O/Z	Video Port 0 D17
31	VP0D18	I/O/Z	Video Port 0 D18	32	VP0D19	I/O/Z	Video Port 0 D19
33	GND		System Ground	34	GND		System Ground
35	VP0CTL2	I/O/Z	Video Port 0 Control 2	36	GND		System Ground
37	GND		System Ground	38	VP0CTL0	I/O/Z	Video Port 0 Control 0
39	VP0CTL1	I/O/Z	Video Port 0 Control 1	40	GND		System Ground
41	GND		System Ground	42	GND		System Ground
43	GND		System Ground	44	VP0CLK1	I/O/Z	Video Port 0 Clock 1
45	VP0CLK0	I/O/Z	Video Port 0 Clock 0	46	GND		System Ground
47	GND		System Ground	48	GND		System Ground
49	GND		System Ground	50	VP1CLK1	I/O/Z	Video Port 1 Clock 1
51	VP1CLK0	I/O/Z	Video Port 1 Clock 0	52	GND		System Ground
53	GND		System Ground	54	VP1CTL0	I/O/Z	Video Port 0 Control 0
55	VP01CTL1	I/O/Z	Video Port 0 Control 1	56	GND		System Ground
57	GND		System Ground	58	VP1CTL1	I/O/Z	Video Port 1 Control 1
59	GND		System Ground	60	GND		System Ground
61	VP1D18	I/O/Z	Video Port 1 D18	62	VP1D19	I/O/Z	Video Port 1 D19
63	VP1D16	I/O/Z	Video Port 1 D16	64	VP1D17	I/O/Z	Video Port 1 D17
65	VP1D14	I/O/Z	Video Port 1 D14	66	VP1D15	I/O/Z	Video Port 1 D15
67	GND		System Ground	68	GND		System Ground
69	VP1D12	I/O/Z	Video Port 1 D12	70	VP1D13	I/O/Z	Video Port 1 D13
71	VP1D10	I/O/Z	Video Port 1 D10	72	VP1D11	I/O/Z	Video Port 1 D11
73	GND		System Ground	74	GND		System Ground
75	VP1D8	I/O/Z	Video Port 1 D8	76	VP1D9	I/O/Z	Video Port 1 D9
77	VP1D6	I/O/Z	Video Port 1 D6	78	VP1D7	I/O/Z	Video Port 1 D7
79	VP1D4	I/O/Z	Video Port 1 D4	80	VP1D5	I/O/Z	Video Port 1 D5
81	GND		System Ground	82	GND		System Ground
83	VP1D2	I/O/Z	Video Port 1 D2	84	VP1D3	I/O/Z	Video Port 1 D3
85	VP1D0	I/O/Z	Video Port 1 D0	86	VP1D1	I/O/Z	Video Port 1 D1
87	GND		System Ground	88	GND		
89	DCARD_STCLK	O		90	GND		

3.2.22 DC_P3, EMIF Expansion

Table 14: DC_P3, EMIF Expansion (all signals are buffered)

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	GND	O	System Ground	2	GND		System Ground
3	DC_D31	I	EMIF Data D31	4	DC_D30	I/O/Z	EMIF Data D30
5	DC_D29		EMIF Data D29	6	DC_D28	I/O/Z	EMIF Data D28
7	DC_D27	I/O/Z	EMIF Data D27	8	DC_D26	I/O/Z	EMIF Data D26
9	DC_D25	I/O/Z	EMIF Data D25	10	DC_D24	I/O/Z	EMIF Data D24
11	GND		System Ground	12	GND		System Ground
13	DC_D23	I/O/Z	EMIF Data D23	14	DC_D22	I/O/Z	EMIF Data D22
15	DC_D21	I/O/Z	EMIF Data D21	16	DC_D20	I/O/Z	EMIF Data D20
17	DC_D19	I/O/Z	EMIF Data D19	18	DC_D18	I/O/Z	EMIF Data D18
19	DC_D17	I/O/Z	EMIF Data D17	20	DC_D16	I/O/Z	EMIF Data D16
21	GND		System Ground	22	GND		System Ground
23	DC_D15	I/O/Z	EMIF Data D15	24	DC_D14	I/O/Z	EMIF Data D14
25	DC_D13	I/O/Z	EMIF Data D13	26	DC_D12	I/O/Z	EMIF Data D12
27	DC_D11	I/O/Z	EMIF Data D11	28	DC_D10	I/O/Z	EMIF Data D10
29	DC_D9	I/O/Z	EMIF Data D9	30	DC_D8	I/O/Z	EMIF Data D8
31	GND		System Ground	32	GND		System Ground
33	DC_D7	I/O/Z	EMIF Data D7	34	DC_D6	I/O/Z	EMIF Data D6
35	DC_D5	I/O/Z	EMIF Data D5	36	DC_D4	I/O/Z	EMIF Data D4
37	DC_D3	I/O/Z	EMIF Data D3	38	DC_D2	I/O/Z	EMIF Data D2
39	DC_D1	I/O/Z	EMIF Data D1	40	DC_D0	I/O/Z	EMIF Data D0
41	GND		System Ground	42	GND		System Ground
43	Reserved			44	DC_ECLKOUT2	O	EMIF CLKOUT2
45	GND		System Ground	46	GND		System Ground
47	DC_BE3#	O	EMIF Byte Strobe	48	DC_BE2#	O	EMIF Byte Strobe2
49	DC_BE1#	O	EMIF Byte Strobe1	50	DC_BE0#	O	EMIF Byte Strobe0
51	GND		System Ground	52	GND		System Ground
53	DC_CE3#	O	EMIF Chip Enable 3	54	DC_CE2#	O	EMIF Chip Select 2
55	GND		System Ground	56	GND		System Ground
57	DC_ARE#	O	EMIF Read Strobe	58	DC_AOE#	O	EMIF Output Enable
59	DC_AWE#	O	EMIF Write Strobe	60	DC_ARDY	I	EMIF Ready
61	GND		System Ground	62	GND		System Ground
63	DC_A22	O	EMIF Address A22	64	DC_A21	O	EMIF Address A21
65	DC_A20	O	EMIF Address A20	66	DC_A19	O	EMIF Address A19
67	DC_A18	O	EMIF Address A18	68	DC_A17	O	EMIF Address A17
69	DC_A16	O	EMIF Address A16	70	DC_A15	O	EMIF Address A15
71	GND		System Ground	72	GND		System Ground
73	DC_A14	O	EMIF Address A14	74	DC_A13	O	EMIF Address A13
75	DC_A12	O	EMIF Address A12	76	DC_A11	O	EMIF Address A11
77	DC_A10	O	EMIF Address A10	78	DC_A9		EMIF Address A9
79	GND		System Ground	80	GND		System Ground
81	DC_A8	O	EMIF Address A8	82	DC_A7	O	EMIF Address A7
83	DC_A6	O	EMIF Address A6	84	DC_A5	O	EMIF Address A5
85	DC_A4	O	EMIF Address A4	86	DC_A3	O	EMIF Address A3
87	GND		System Ground	88	GND		System Ground
89	Reserved			90	Reserved		

3.3 User LEDs

The TMS320DM642 EVM has eight user LEDs (DS1-DS8). The state of the LEDs are controlled by the FPGA LED Register at location 0x9008 0017. The color and function of these LEDs are shown in the table below.

Table 15: DM642 LEDs

LED Number	Color	Function
DS1	Green	Programmable via FPGA LED Register D0
DS2	Green	Programmable via FPGA LED Register D1
DS3	Green	Programmable via FPGA LED Register D2
DS4	Green	Programmable via FPGA LED Register D3
DS5	Green	Programmable via FPGA LED Register D4
DS6	Green	Programmable via FPGA LED Register D5
DS7	Green	Programmable via FPGA LED Register D6
DS8	Green	Programmable via FPGA LED Register D7

3.4 System Status LEDs

The TMS320DM642 EVM has five System Status LEDs (DS9-DS13). The LEDs give visual feedback to various states of EVM function as shown in the table below.

Table 16: System Status LEDs

LED Number	Color	Function
DS9	Yellow	FPGA Programming Complete
DS10	Green	Decoder 1 Lock
DS11	Yellow	Reset
DS12	Green	Input Power
DS13	Green	Decoder 2 Lock

3.5 Reset Switch - S3

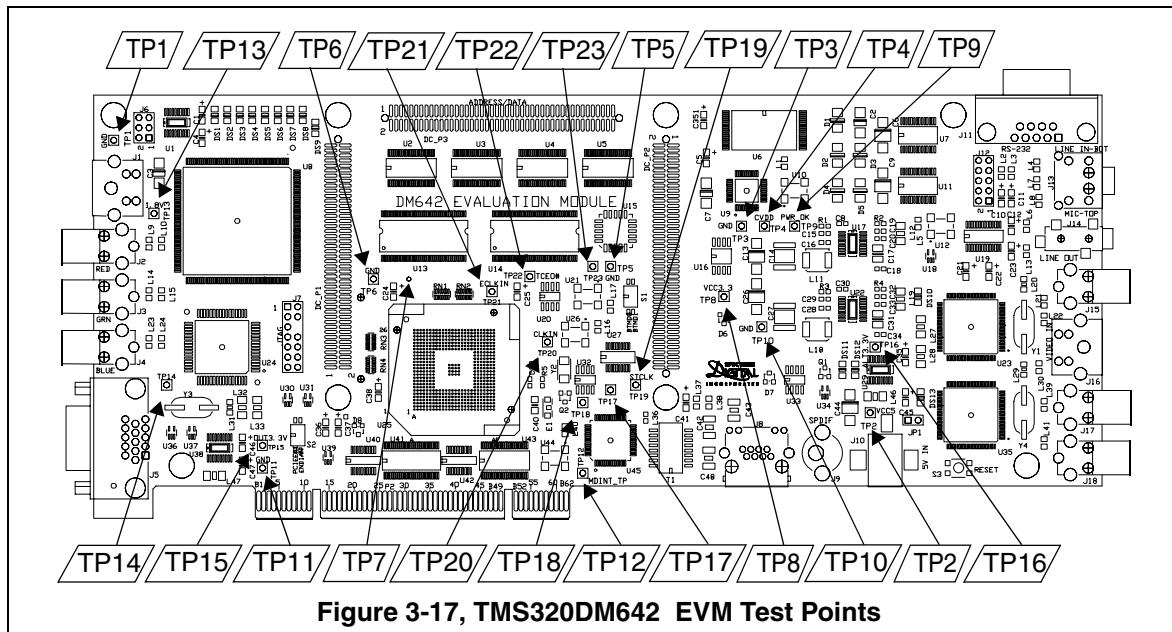
There are three sources for reset on the TMS320DM642 EVM. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320DM642.

The second source is the push button Reset switch, S3. When this button is pressed the EVM is put through the reset state.

There is also an optional 2 pin Reset header, JP1, which is connected in parallel to the Reset switch, S3. When this header is shorted the EVM is put into reset

3.6 Test Points

The TMS320DM642 EVM has 23 test points. Their position are shown in the figure below.



The test points and the signals present on them are shown in the table below.

Table 17: DM642 EVM Test Points

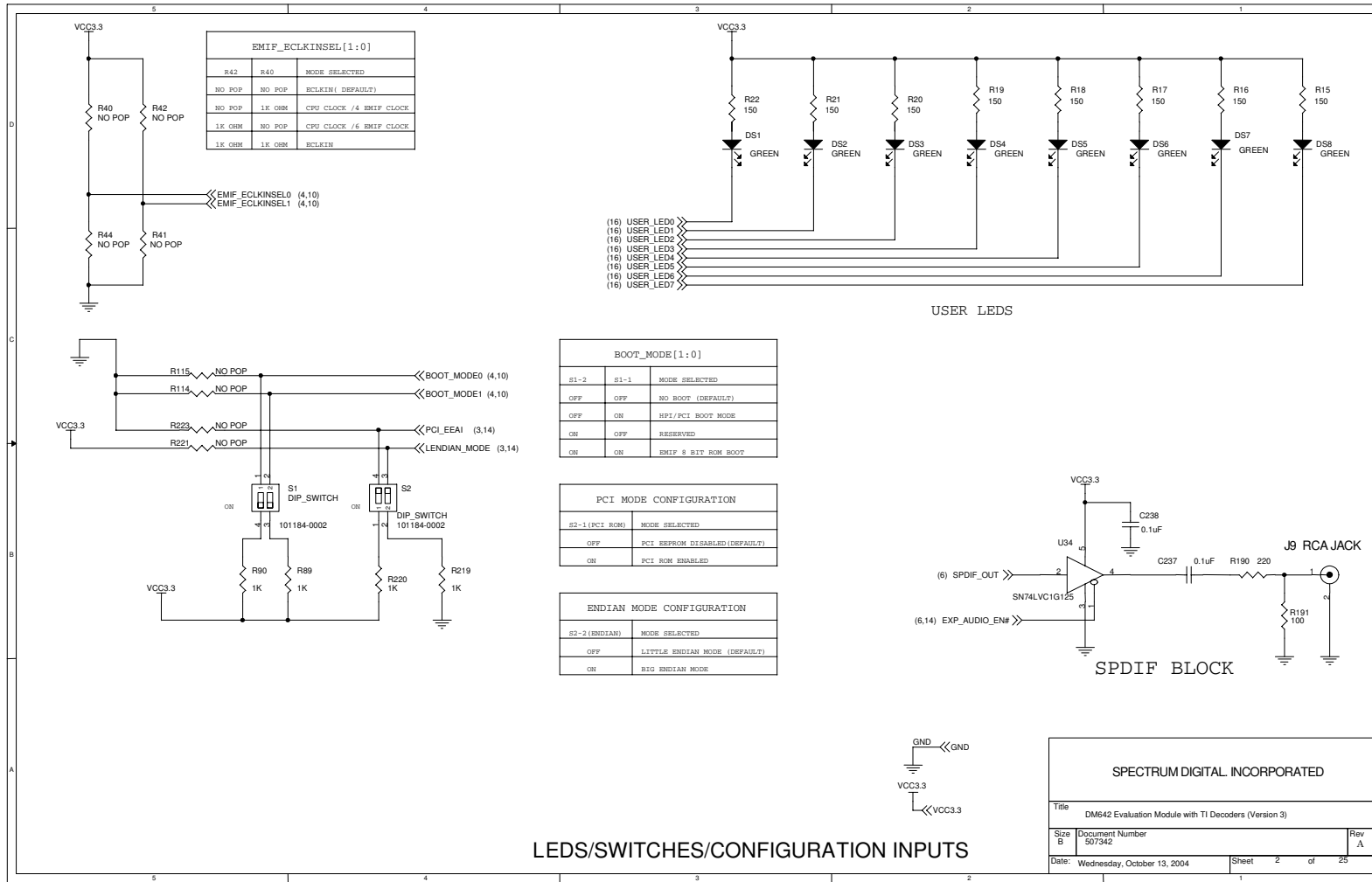
Test Point	Name	Signal Function
TP1	GND	Ground
TP2	VCC5	+5.0 Volts, Power Input
TP3	GND	Ground
TP4	CVDD	+1.4 Volts Core Power
TP5	GND	Ground
TP6	GND	Ground
TP7	TDPT#	DM642 DPT Pin
TP8	VCC3.3	I/O & Main +3.3 Volt Power
TP9	PWR OK	I/O & Core Power In Range
TP10	GND	Ground
TP11	GND	Ground
TP12	MDINT_TP	PHY Status Interrupt
TP13	+1.8 Volts	FPGA Core power
TP14	RESET	System Reset
TP15	OUT3	Encoder +3.3 Volts
TP16	1.8V DEC	Decoder +1.8 Volts
TP17	VICTP	VIC IF Test Point
TP18	VDAC	DM642 VDAC Output Pin
TP19	STCLK	VIC STCLK Input
TP20	CLKIN	CPU Input Clock
TP21	ECLKIN	EMIF Input Clock
TP22	TCEO#	Chip Enable 0
TP23	TCE1#	Chip Enable 1

Appendix A

Schematics

This appendix contains the schematics for the TMS320DM642 EVM.

1	2	3	4	5																																																																																																																					
<p>NOTES, UNLESS OTHERWISE SPECIFIED:</p> <ol style="list-style-type: none"> RESISTANCE VALUES IN OHMS. CAPACITANCE VALUES IN MICROFARADS. REFERENCE DESIGNATORS USED: 		<table border="1"> <thead> <tr> <th>REV</th> <th>DESCRIPTION</th> <th>DATE</th> <th>APPROVED</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>Initial schematic ready for layout.</td> <td>01/07/04</td> <td>RRP</td> </tr> <tr> <td>B</td> <td>Sheet3: Added AND gate U49 to support optional emulator reset. Sheet05: Add quick switch on JTAG to provide some ESD protection to EMU pins on DM642. Added optional emulator reset from pin A15. Sheet16: Added series termination resistors between FPGA and encoder Sheet20: HD Filters used on encoder outputs as shipped</td> <td>10/01/04</td> <td>RRP</td> </tr> </tbody> </table>			REV	DESCRIPTION	DATE	APPROVED	A	Initial schematic ready for layout.	01/07/04	RRP	B	Sheet3: Added AND gate U49 to support optional emulator reset. Sheet05: Add quick switch on JTAG to provide some ESD protection to EMU pins on DM642. Added optional emulator reset from pin A15. Sheet16: Added series termination resistors between FPGA and encoder Sheet20: HD Filters used on encoder outputs as shipped	10/01/04	RRP																																																																																																									
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B	Sheet3: Added AND gate U49 to support optional emulator reset. Sheet05: Add quick switch on JTAG to provide some ESD protection to EMU pins on DM642. Added optional emulator reset from pin A15. Sheet16: Added series termination resistors between FPGA and encoder Sheet20: HD Filters used on encoder outputs as shipped	10/01/04	RRP																																																																																																																						
<ol style="list-style-type: none"> ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR. OBSERVE THE FOLLOWING LAYOUT NOTES: BOARD PROPERTIES <ol style="list-style-type: none"> ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE 50 +/- 5 OHM MATCHED IMPEDANCE OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING INNER LAYERS 1.0 OZ CU FPGA BOARD MATERIAL MINIMUM TRACE WIDTH/SPACING 4 MILS MINIMUM VIA SIZE 10/19 MIL LAYER STACKUP: <ol style="list-style-type: none"> TOP - SIGNAL ROUTING GROUND PLANE INNER1 - SIGNAL ROUTING VCC3 PLANE (3.3V BOARD) INNER2 - SIGNAL ROUTING INNER3 - SIGNAL ROUTING VCC PLANE 2 INNER4 - SIGNAL ROUTING GROUND PLANE BOTTOM - SIGNAL ROUTING 		<p>SCHEMATIC INDEX</p> <ol style="list-style-type: none"> DM642 EVM Notes and Contents User Options/Config DM642 Clocks, Reset, Interrupts, Timers, and IIC DM642 EMIF Emulation Headers DM642 Video Ports DM642 PCI/HPI/EMAC DM642 Power Pins SDRAM Expansion EMIF Buffers Flash and Dual UART RS232 Buffers Video Port Expansion Switches Video Port Daughter Card Connector EMIF Daughter Card Connector OSD FPGA OSD FPGA Power Video Decoder 1 Video Decoder 2 Video Encoder Ethernet PCI AIC23 Audio Interface Power FPGA Power/Reset Circuitry 																																																																																																																							
<table border="1"> <thead> <tr> <th colspan="10">REVISION STATUS OF SHEETS</th> </tr> <tr> <th>REV</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>9</th> <th>10</th> </tr> </thead> <tbody> <tr> <td>REV</td> <td>A</td> <td>A</td> <td>A</td> <td>A</td> <td>A</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>SR</td> <td>21</td> <td>22</td> <td>23</td> <td>24</td> <td>25</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>REV</td> <td>A</td> <td>A</td> <td>A</td> <td>A</td> <td>A</td> <td>B</td> <td>A</td> <td>A</td> <td>A</td> <td>B</td> </tr> <tr> <td>SR</td> <td>11</td> <td>12</td> <td>13</td> <td>14</td> <td>15</td> <td>16</td> <td>17</td> <td>18</td> <td>19</td> <td>20</td> </tr> <tr> <td>REV</td> <td>B</td> <td>A</td> <td>B</td> <td>A</td> <td>B</td> <td>A</td> <td>A</td> <td>A</td> <td>A</td> <td>NEXT ASSY</td> </tr> <tr> <td>SR</td> <td>1</td> <td>2</td> <td>3</td> <td>4</td> <td>5</td> <td>6</td> <td>7</td> <td>8</td> <td>9</td> <td>10</td> </tr> </tbody> </table>		REVISION STATUS OF SHEETS										REV	1	2	3	4	5	6	7	8	9	10	REV	A	A	A	A	A						SR	21	22	23	24	25						REV	A	A	A	A	A	B	A	A	A	B	SR	11	12	13	14	15	16	17	18	19	20	REV	B	A	B	A	B	A	A	A	A	NEXT ASSY	SR	1	2	3	4	5	6	7	8	9	10	<table border="1"> <thead> <tr> <th>REV</th> <th>DATE</th> </tr> </thead> <tbody> <tr> <td>DM</td> <td>R.R.P. 03/01/2004</td> </tr> <tr> <td>SR</td> <td>T.W.K. 03/01/2004</td> </tr> <tr> <td>DMR</td> <td>R.R.P. 03/01/2004</td> </tr> <tr> <td>DMR-MGR</td> <td>R.R.P. 03/01/2004</td> </tr> <tr> <td>JA</td> <td>C.M.D. 03/01/2004</td> </tr> <tr> <td>MFG</td> <td>R.R.P. 03/01/2004</td> </tr> <tr> <td>ELSE</td> <td>R.R.P. 03/01/2004</td> </tr> </tbody> </table>			REV	DATE	DM	R.R.P. 03/01/2004	SR	T.W.K. 03/01/2004	DMR	R.R.P. 03/01/2004	DMR-MGR	R.R.P. 03/01/2004	JA	C.M.D. 03/01/2004	MFG	R.R.P. 03/01/2004	ELSE	R.R.P. 03/01/2004	<p>SPECTRUM DIGITAL INCORPORATED</p> <table border="1"> <tr> <td>Title</td> <td colspan="2">DM642 Evaluation Module with TI Decoders (Version 3)</td> </tr> <tr> <td>Size</td> <td>Document Number</td> <td>Rev</td> </tr> <tr> <td>B</td> <td>507342</td> <td>B</td> </tr> <tr> <td>Date:</td> <td>Thursday, December 02, 2004</td> <td>Sheet 1 of 25</td> </tr> </table>		Title	DM642 Evaluation Module with TI Decoders (Version 3)		Size	Document Number	Rev	B	507342	B	Date:	Thursday, December 02, 2004	Sheet 1 of 25
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EMIF_ECLKINSEL[1:0]		
R42	R40	MODE SELECTED
NO POP	NO POP	ECLKIN(DEFAULT)
NO POP	1K OHM	CPU CLOCK /4 EMIF CLOCK
1K OHM	NO POP	CPU CLOCK /6 EMIF CLOCK
1K OHM	1K OHM	ECLKIN

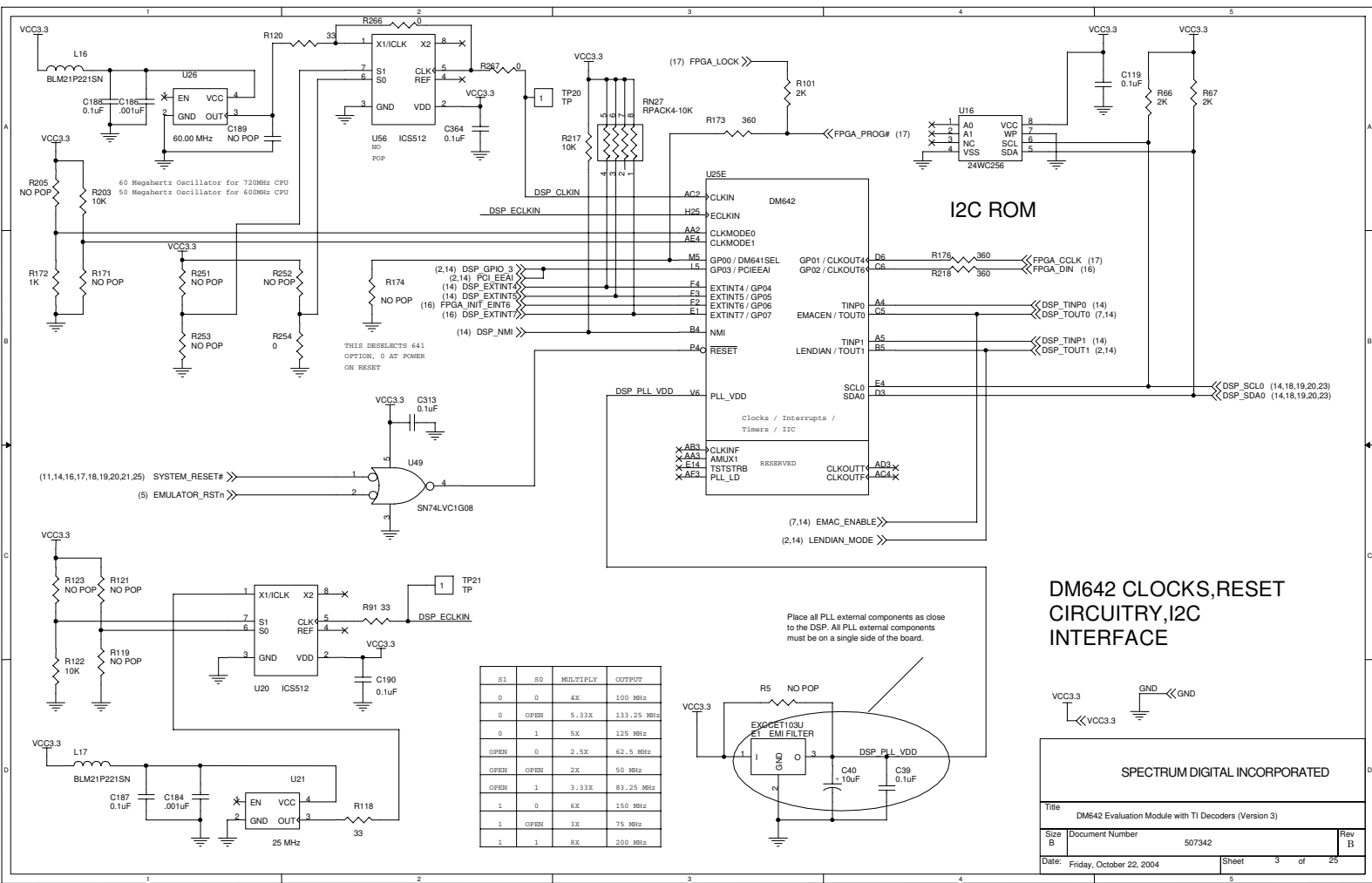
BOOT_MODE[1:0]		
S1-2	S1-1	MODE SELECTED
OFF	OFF	NO BOOT (DEFAULT)
OFF	ON	WPI/PCI BOOT MODE
ON	OFF	RESERVED
ON	ON	EMIF 8 BIT ROM BOOT

PCI MODE CONFIGURATION	
S2-1 (PCI ROM)	MODE SELECTED
OFF	PCI EEPROM DISABLED (DEFAULT)
ON	PCI ROM ENABLED

ENDIAN MODE CONFIGURATION	
S2-2 (ENDIAN)	MODE SELECTED
OFF	LITTLE ENDIAN MODE (DEFAULT)
ON	BIG ENDIAN MODE

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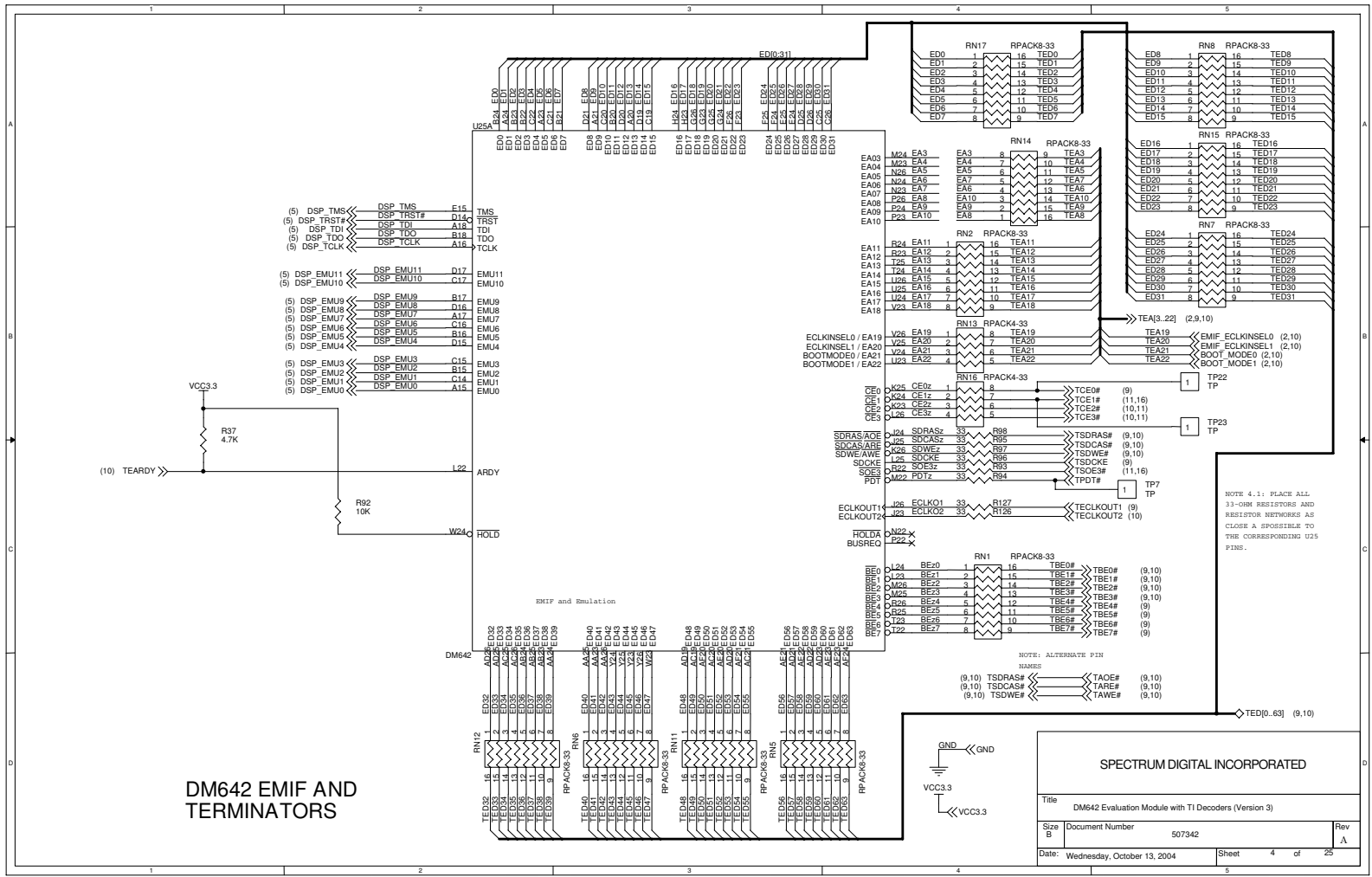
DM642 CLOCKS, RESET CIRCUITRY, I2C INTERFACE

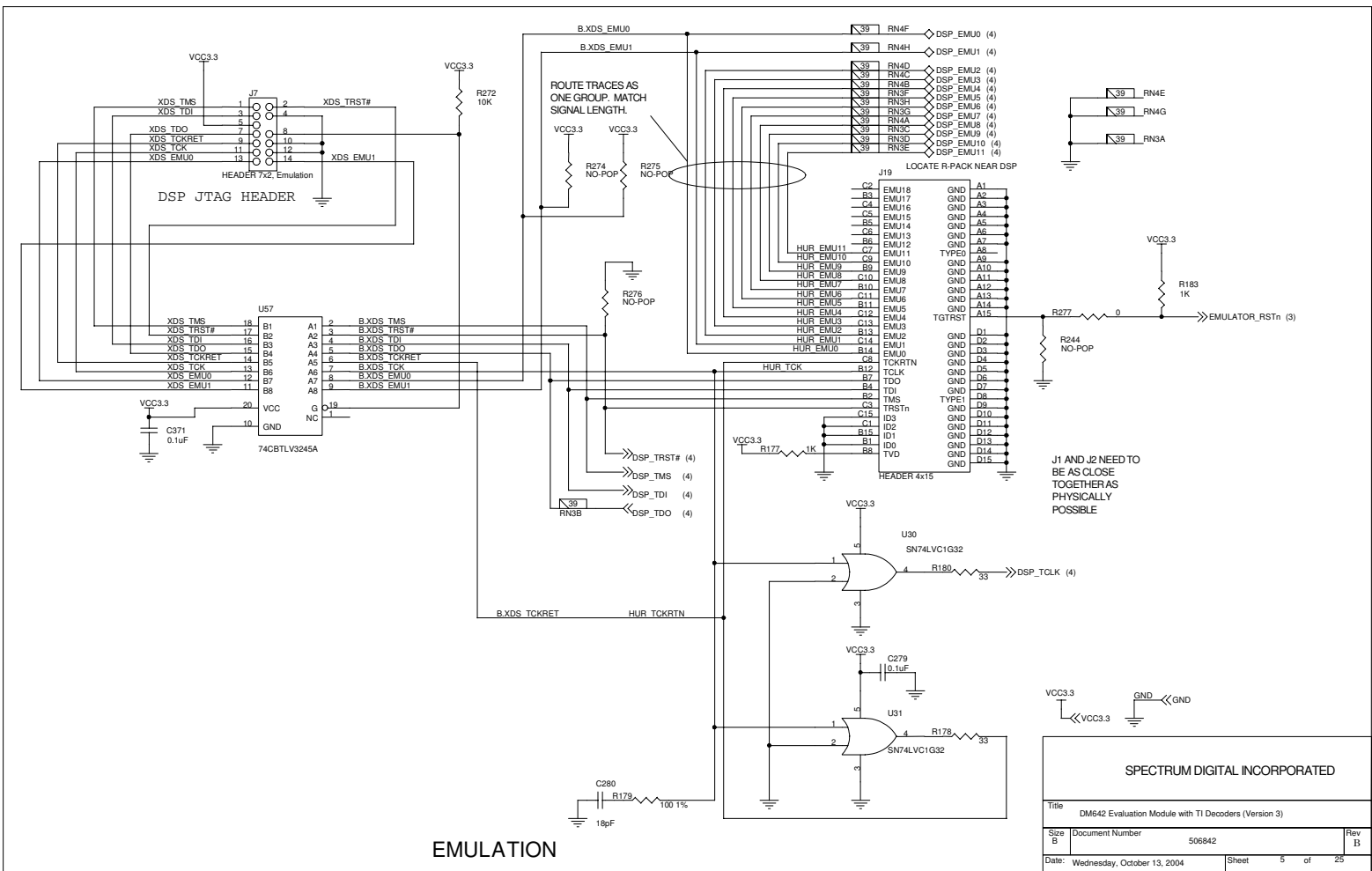
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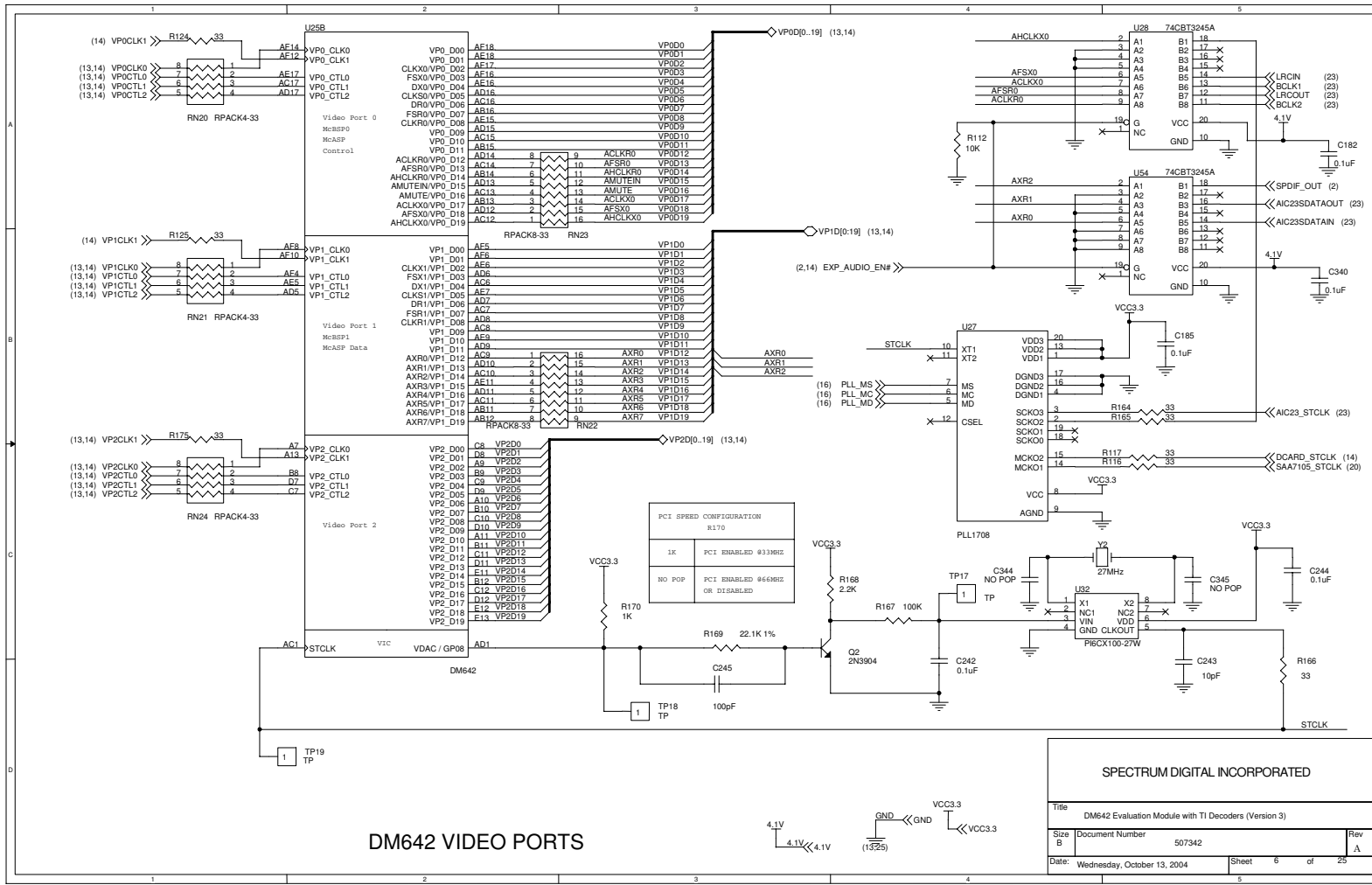
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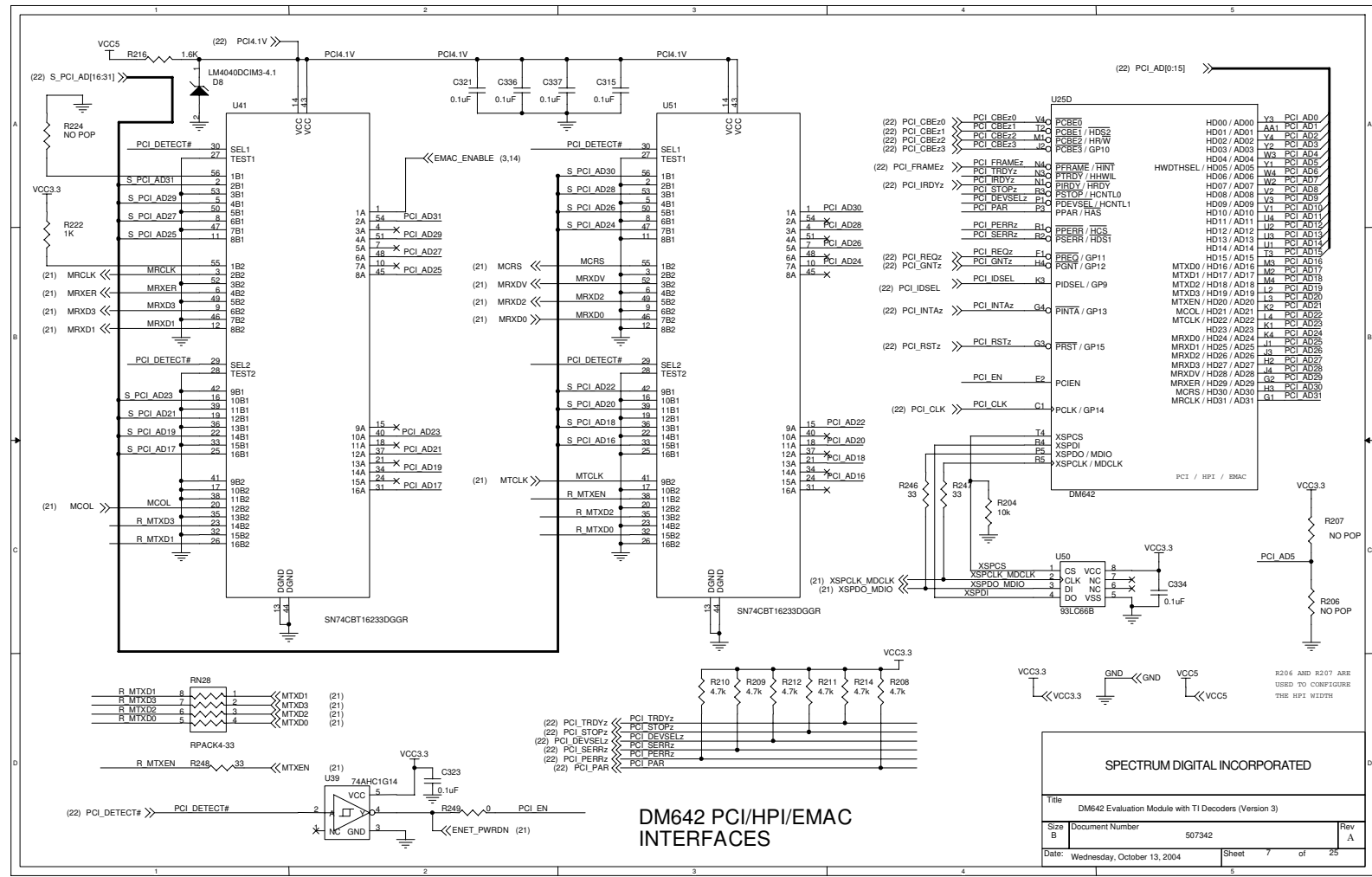
EMULATION

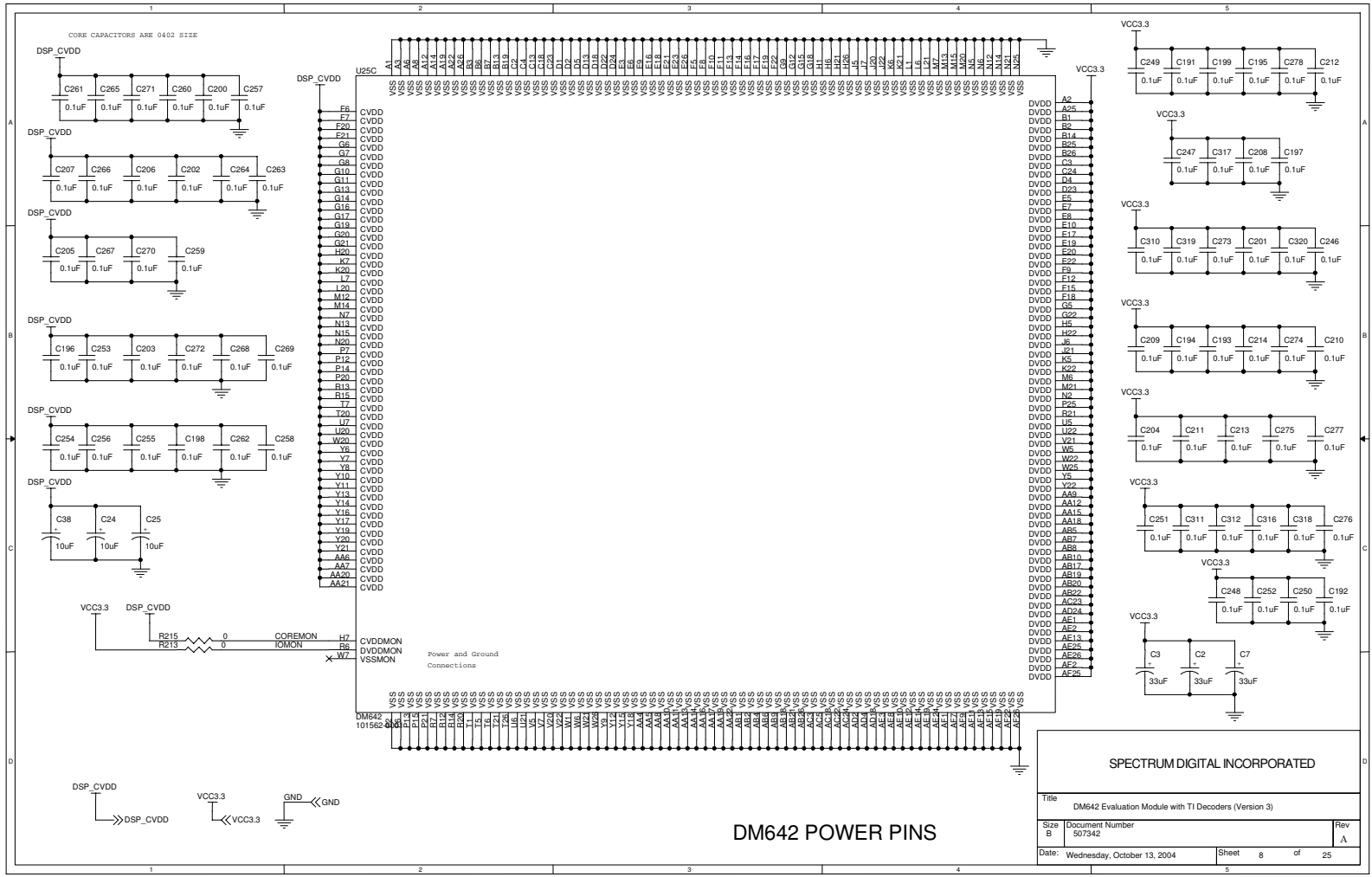
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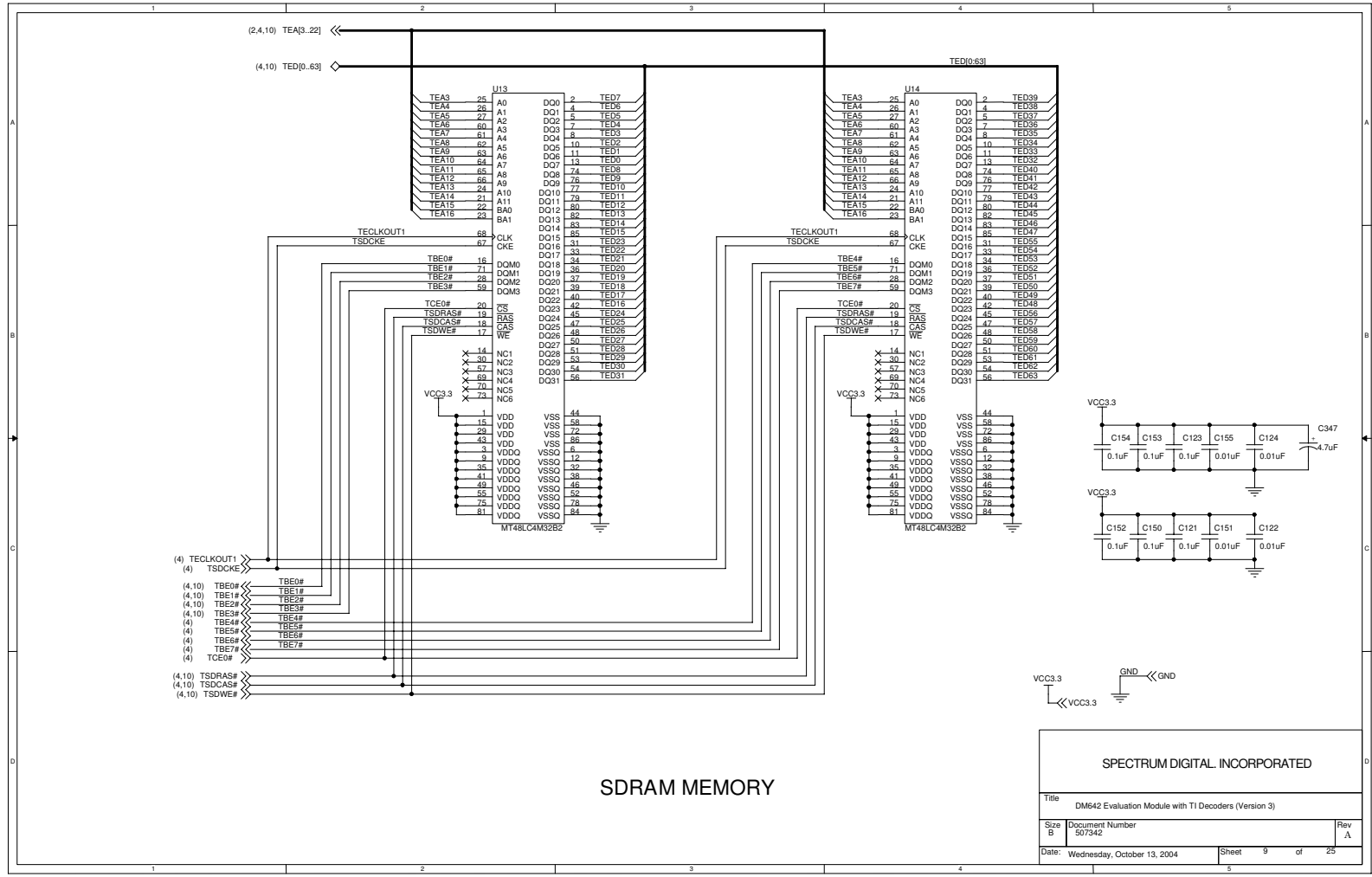
Spectrum Digital, Inc

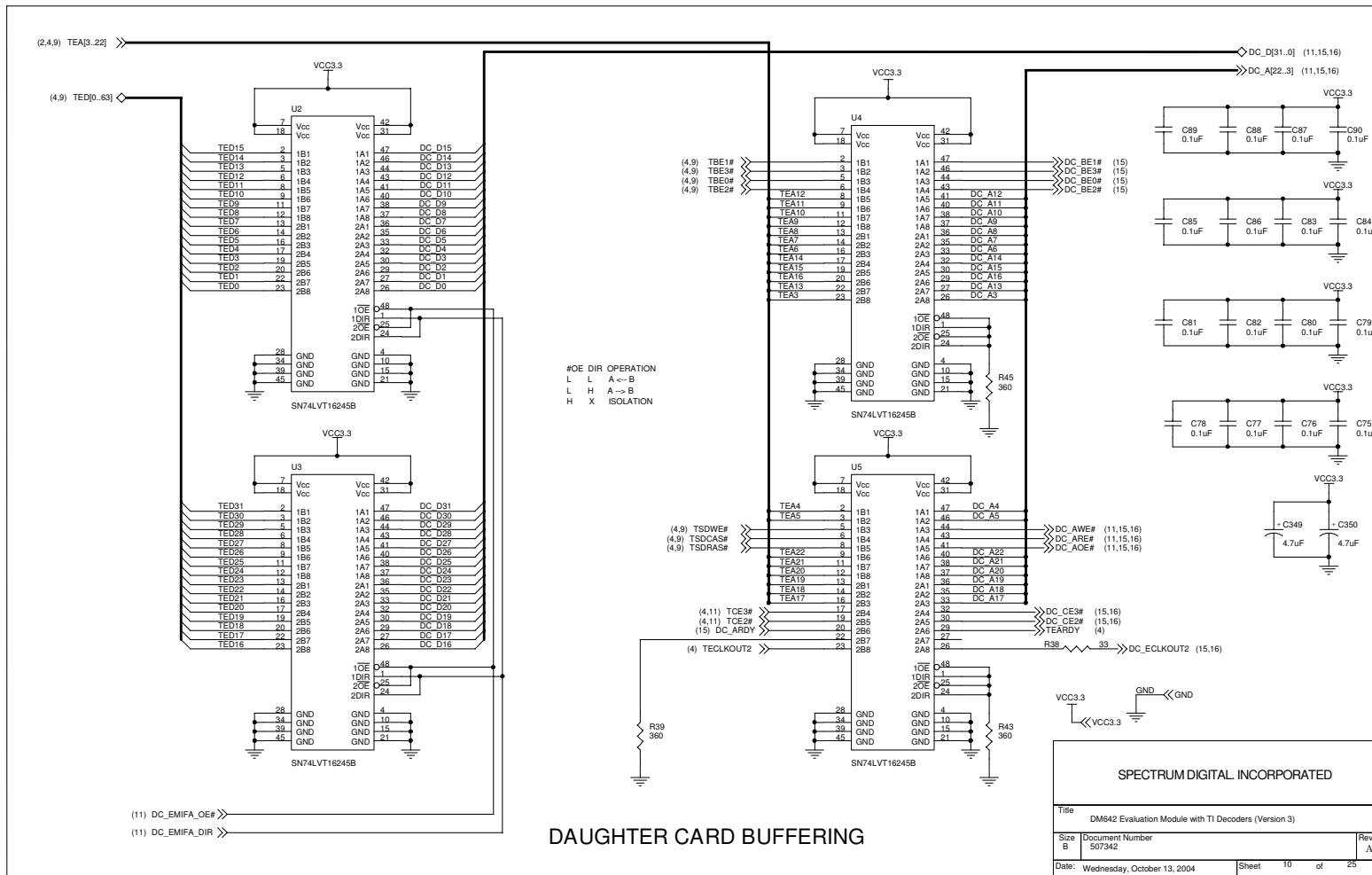




DM642 POWER PINS

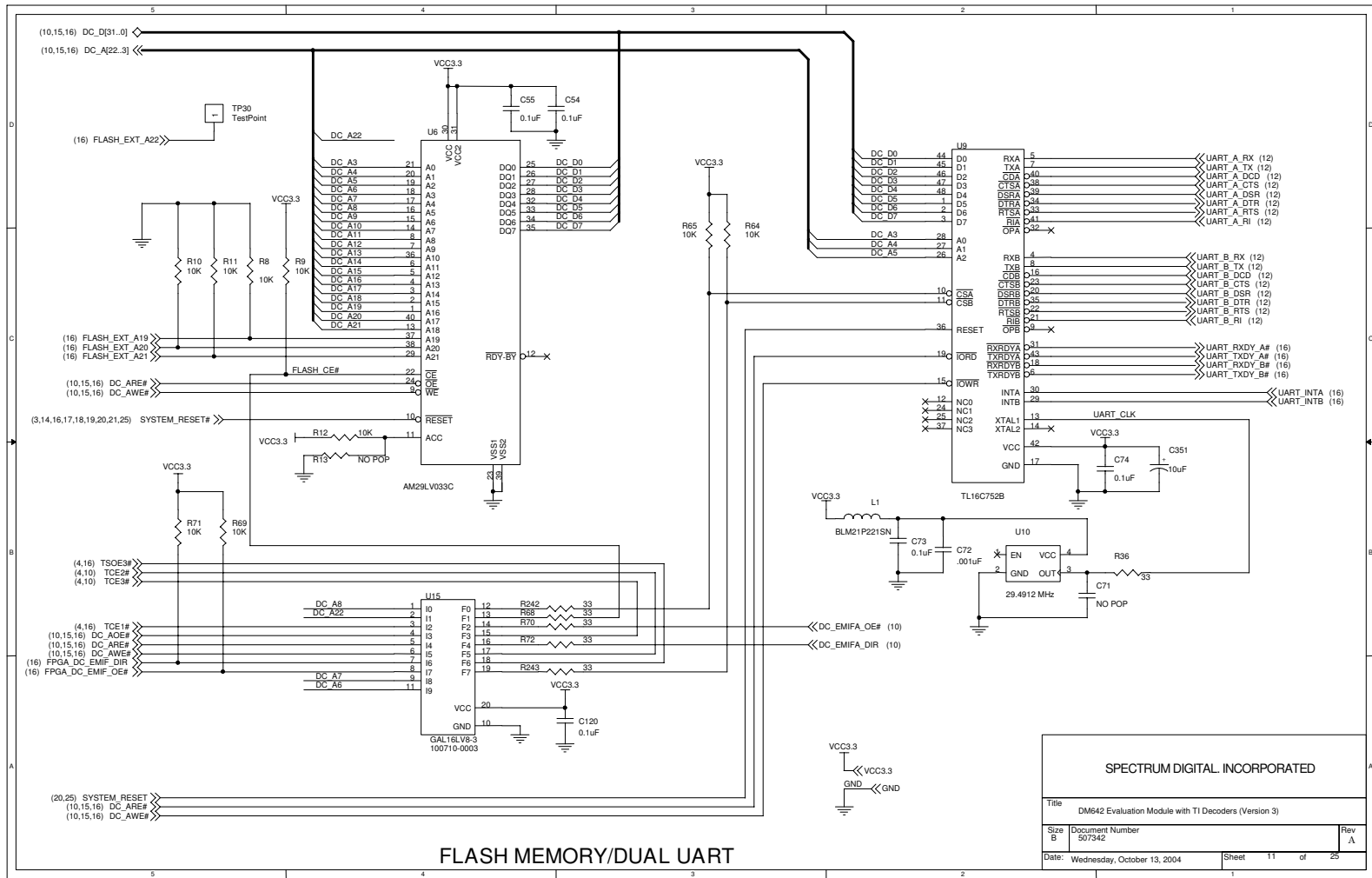
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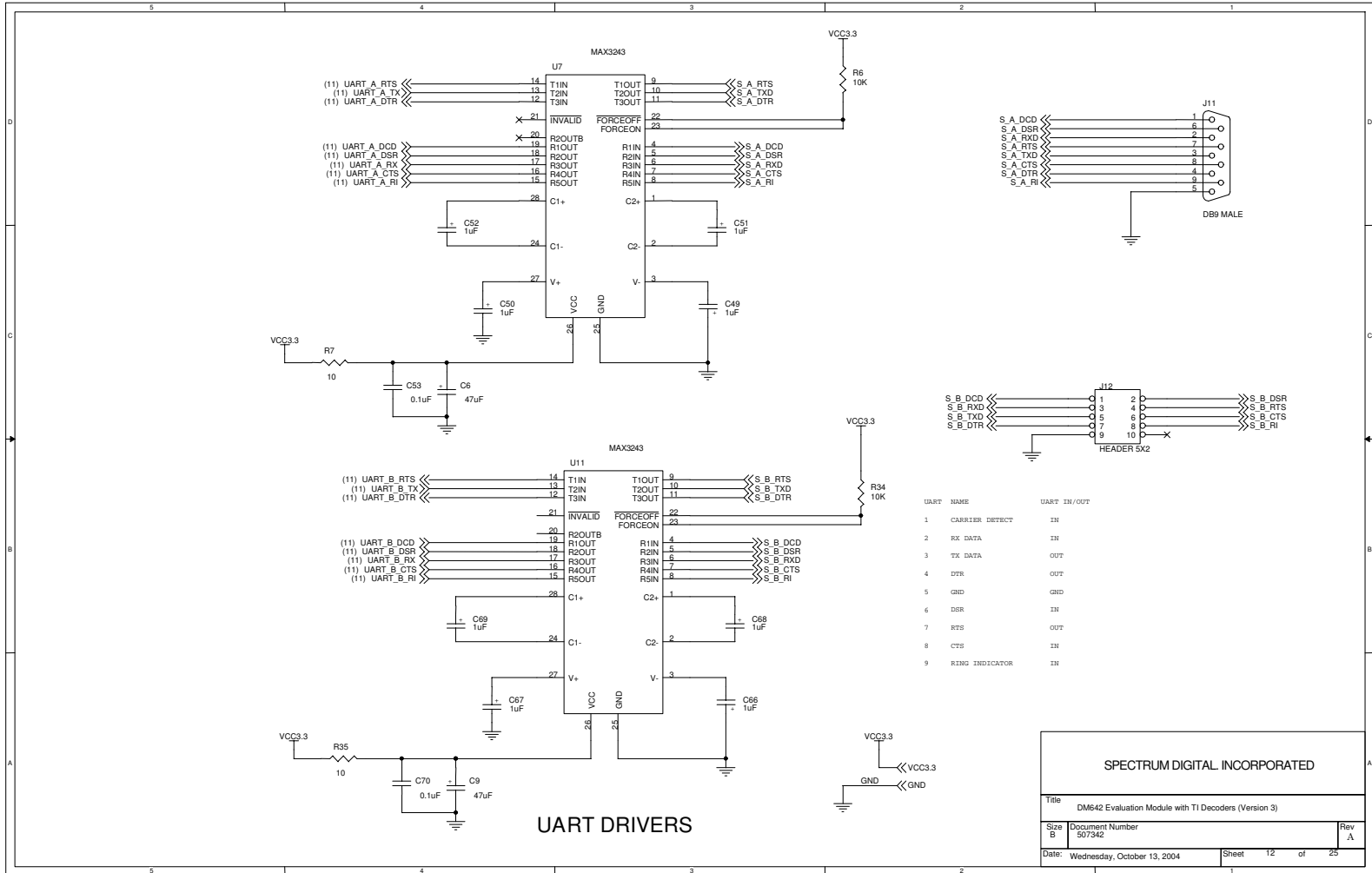


FLASH MEMORY/DUAL UART

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TMS320DM642 EVM Technical Reference

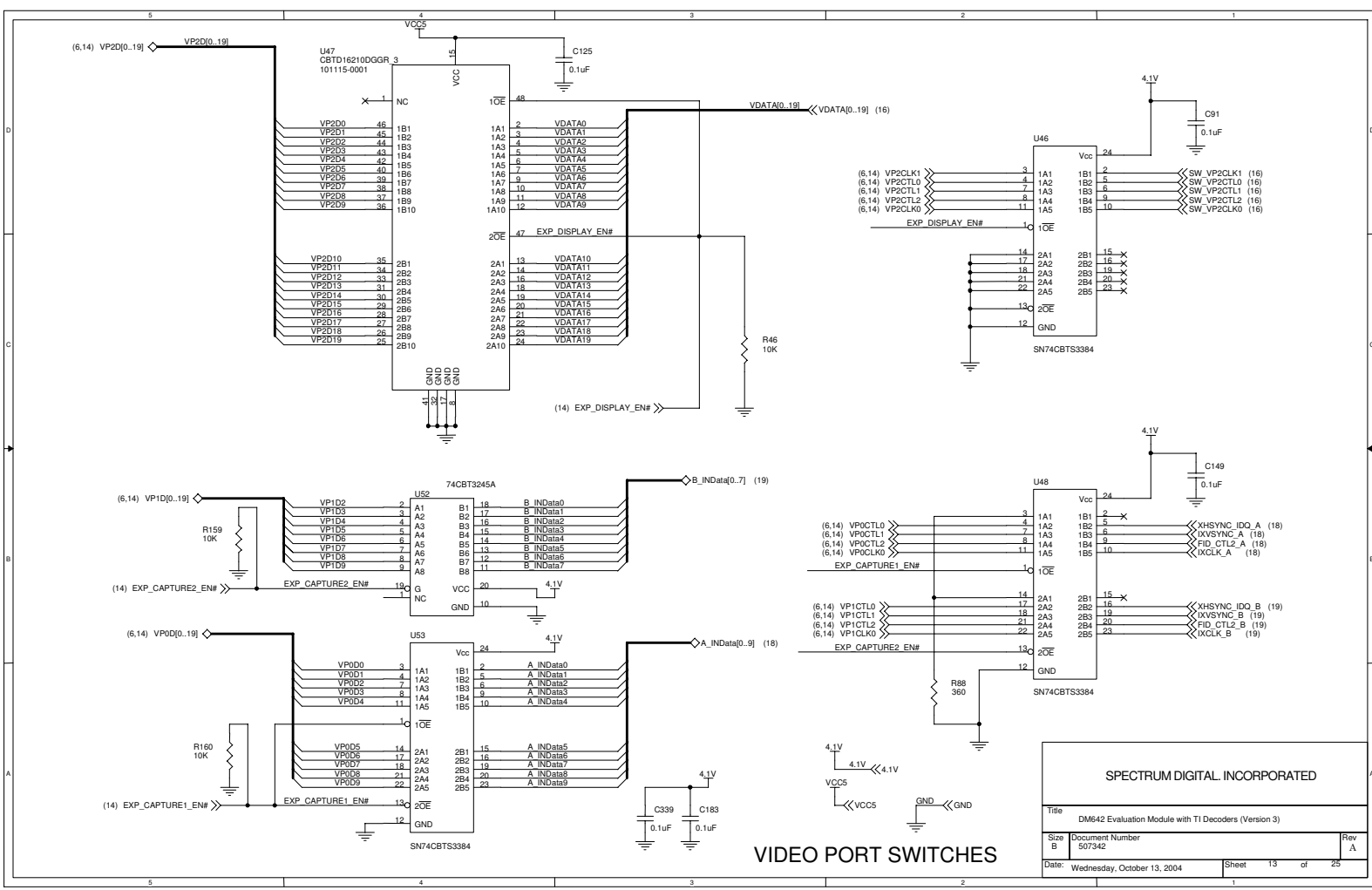


UART DRIVERS

UART NAME	UART IN/OUT
1 CARRIER DETECT	IN
2 RX DATA	IN
3 TX DATA	OUT
4 DTR	OUT
5 GND	GND
6 DSR	IN
7 RTS	OUT
8 CTS	IN
9 RING INDICATOR	IN

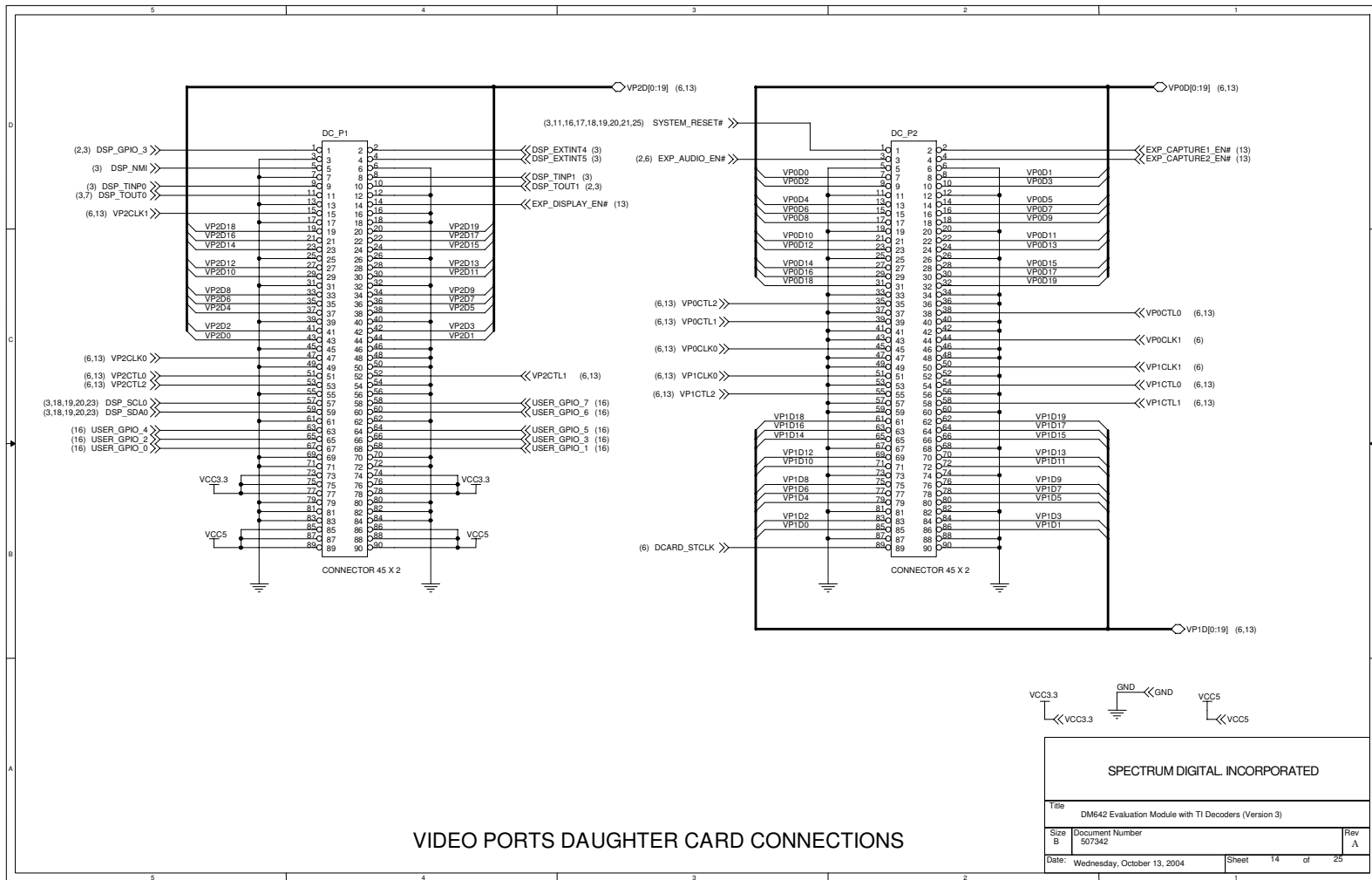
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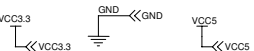


VIDEO PORT SWITCHES

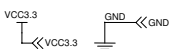
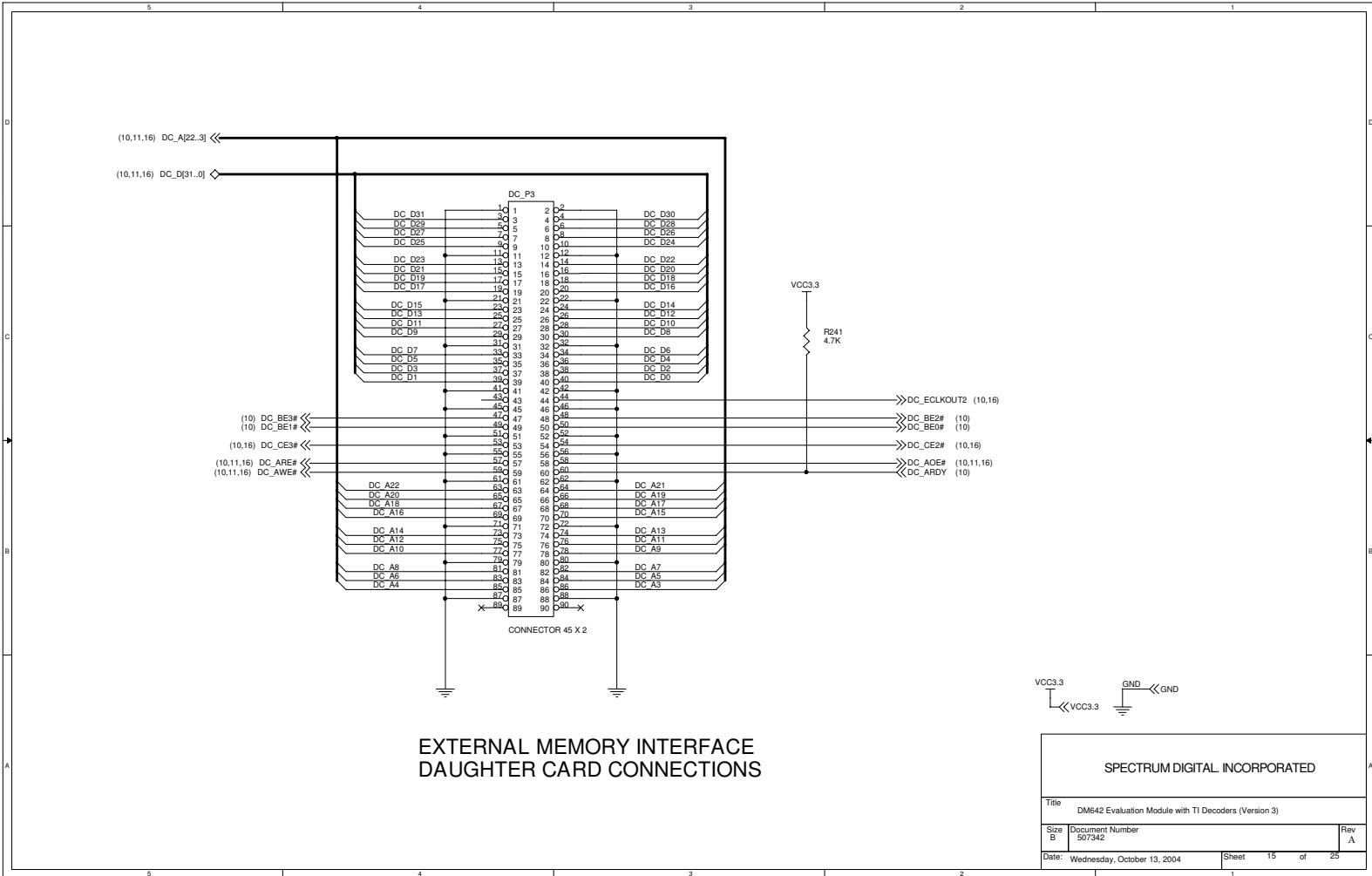
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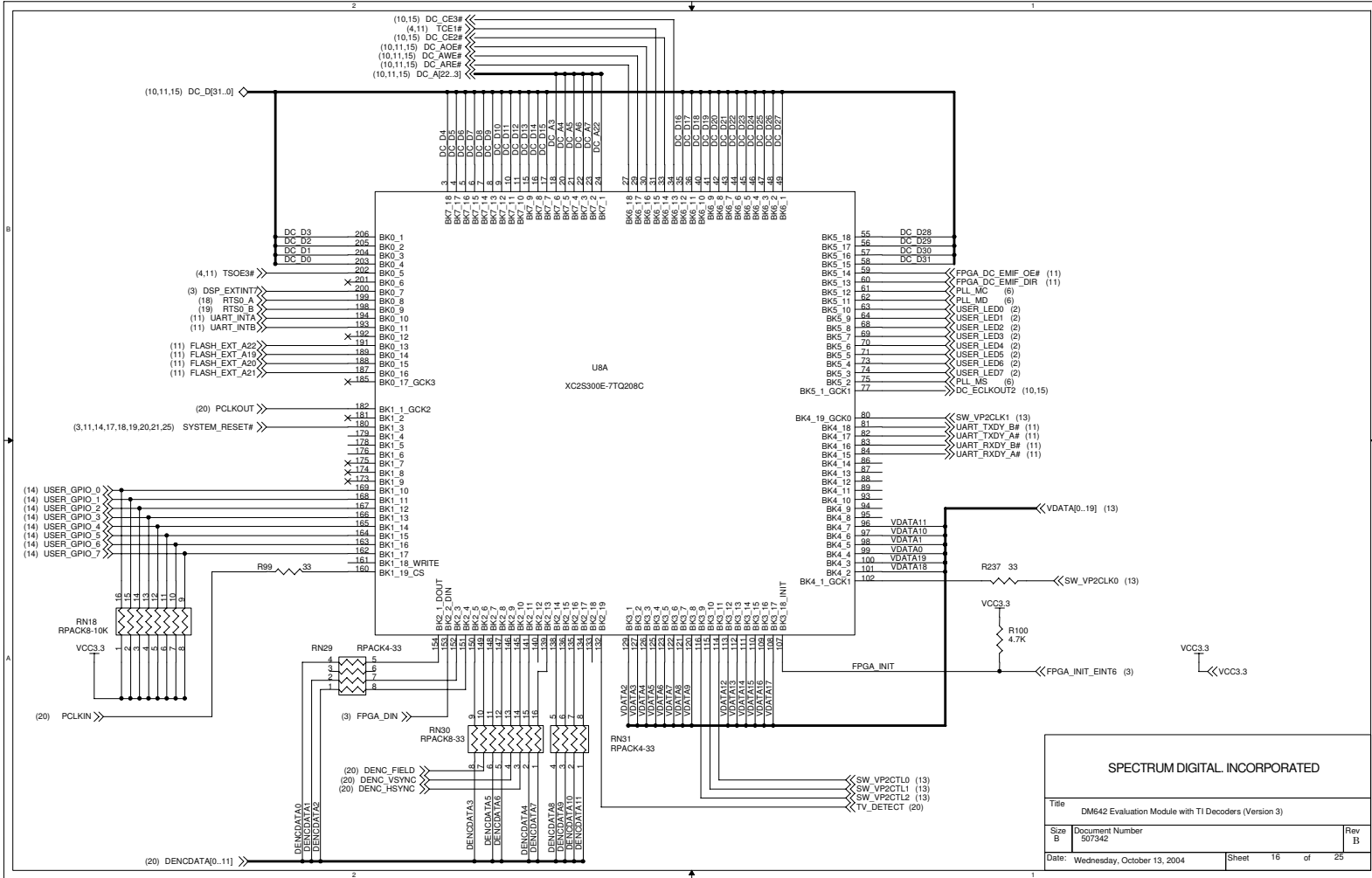
VIDEO PORTS DAUGHTER CARD CONNECTIONS



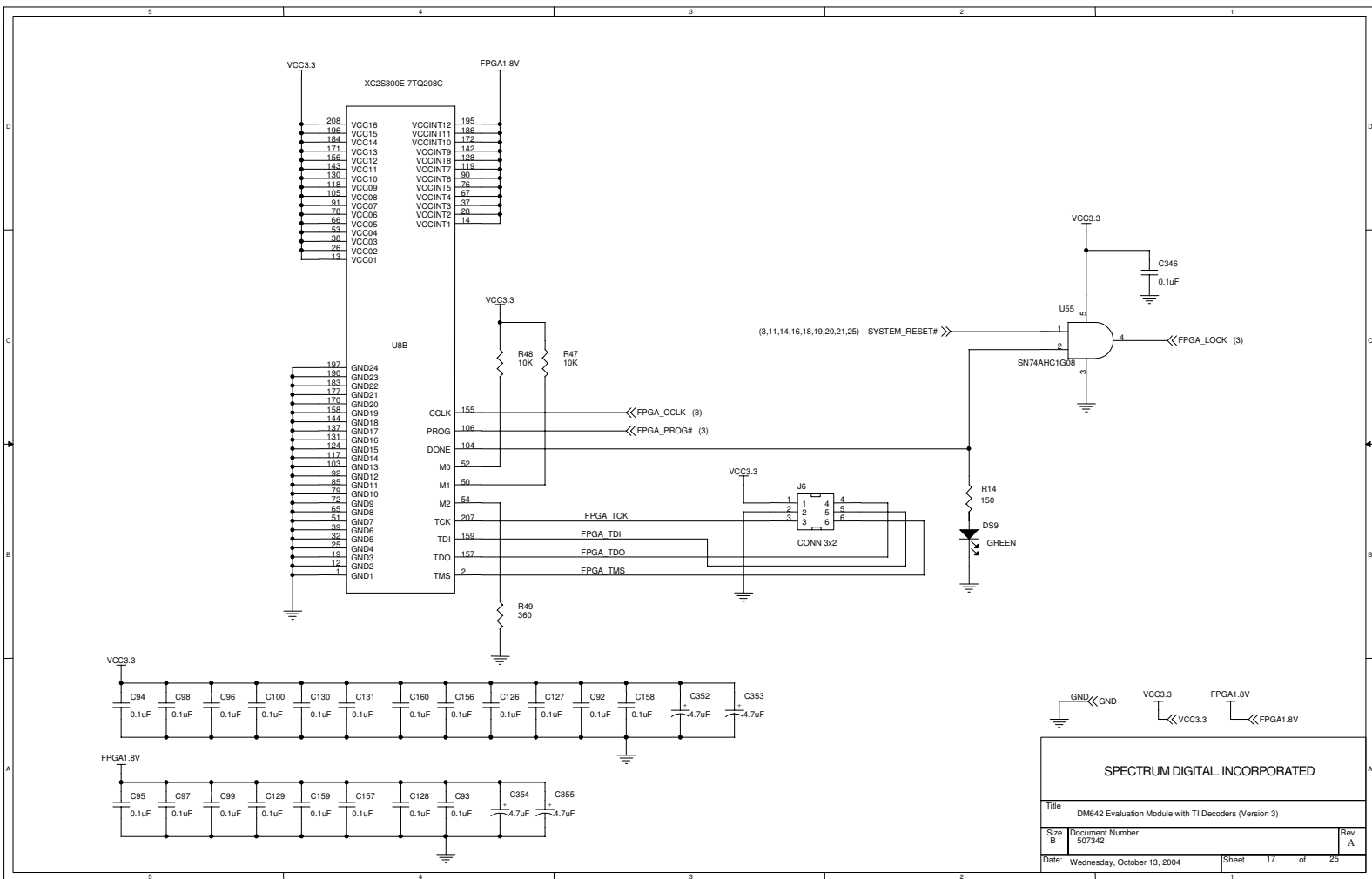
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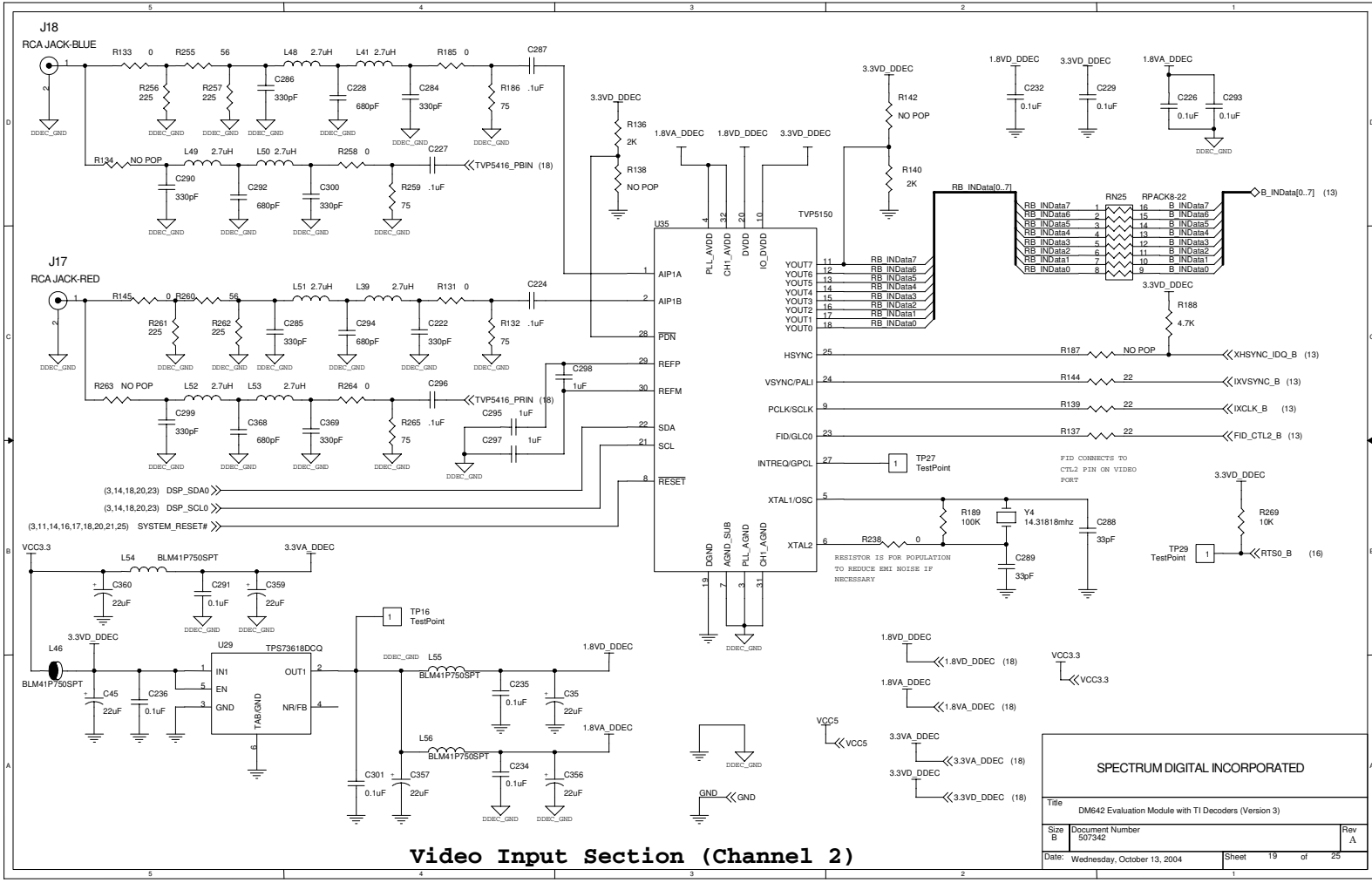


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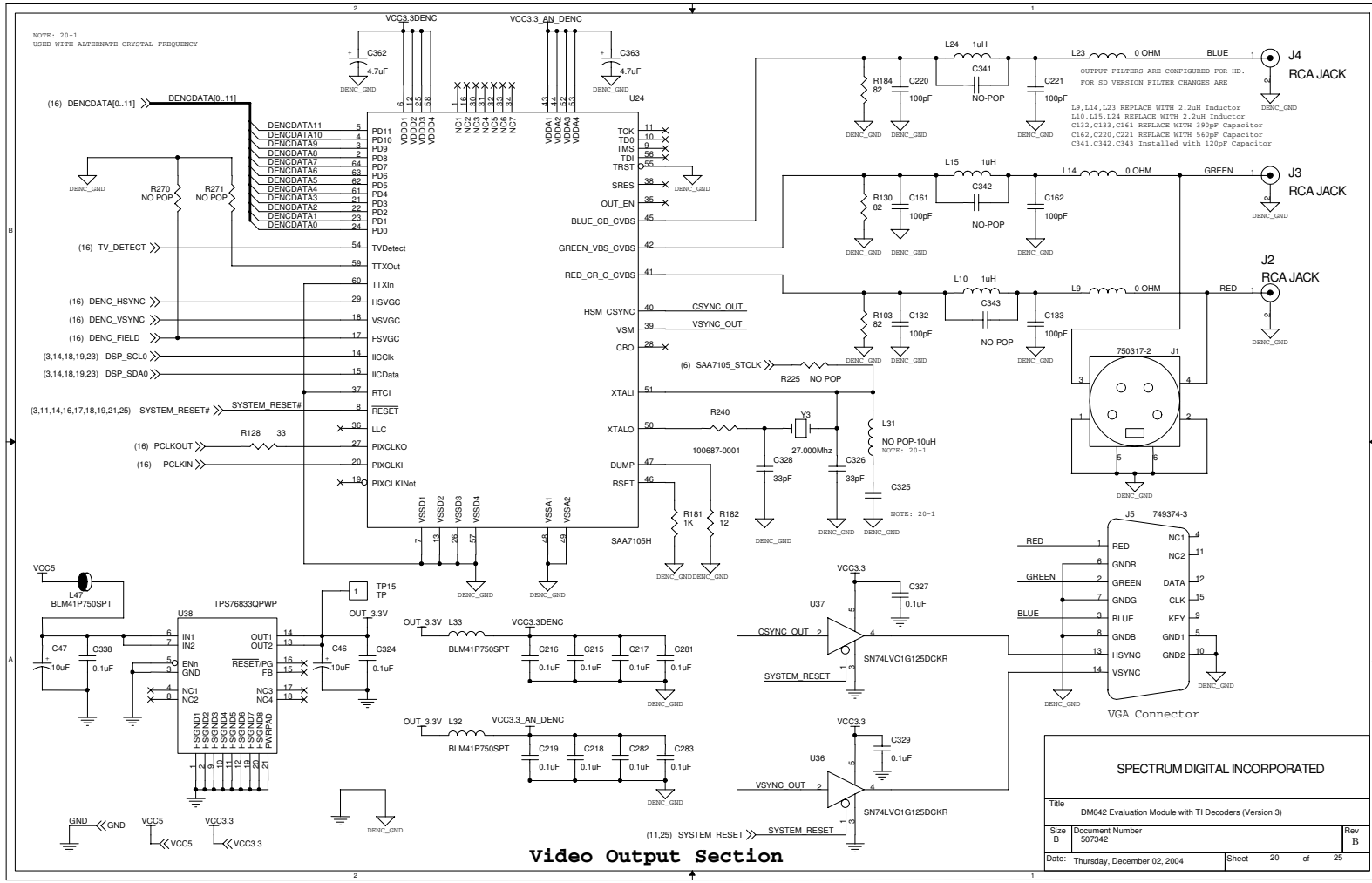
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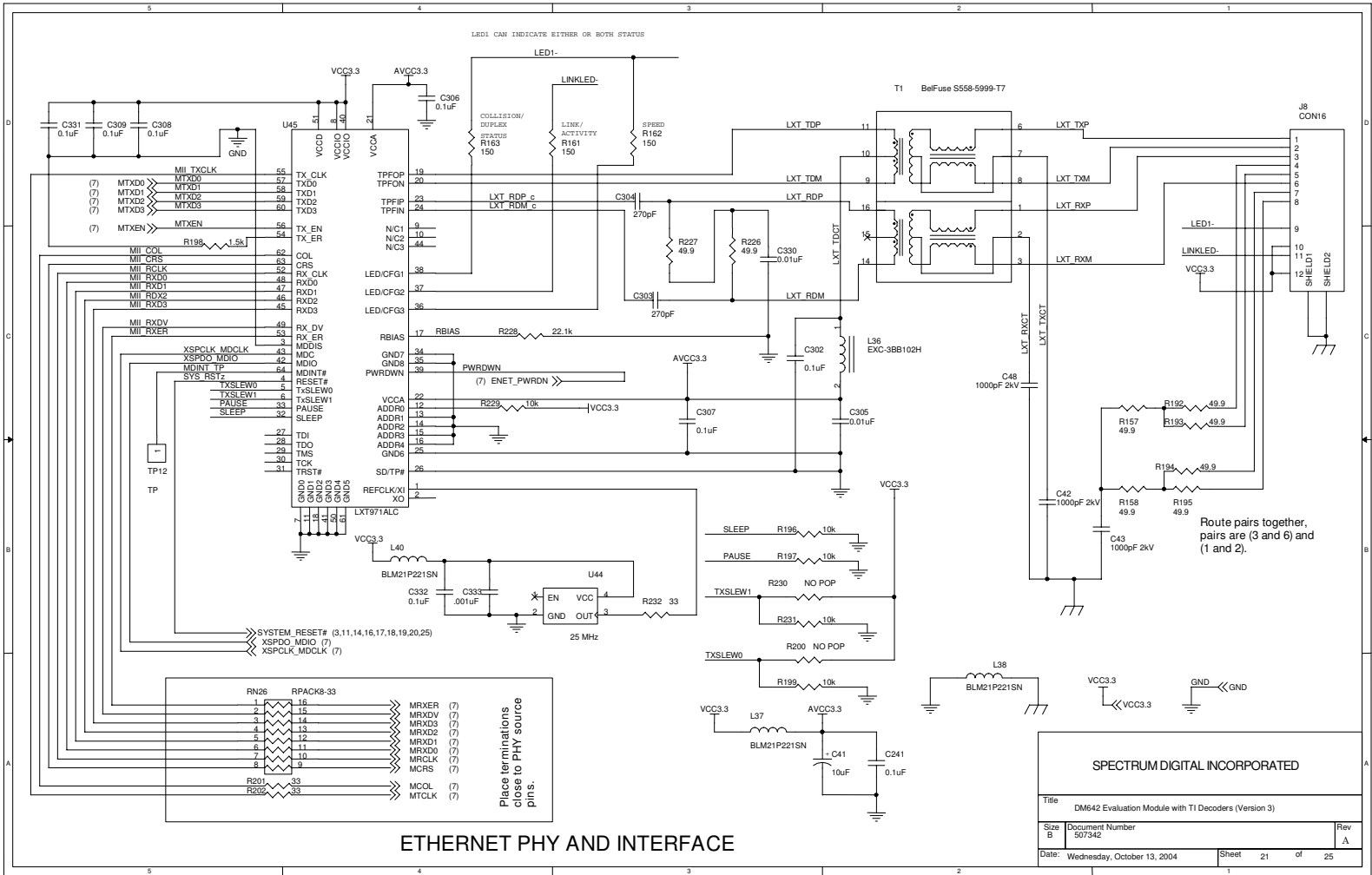
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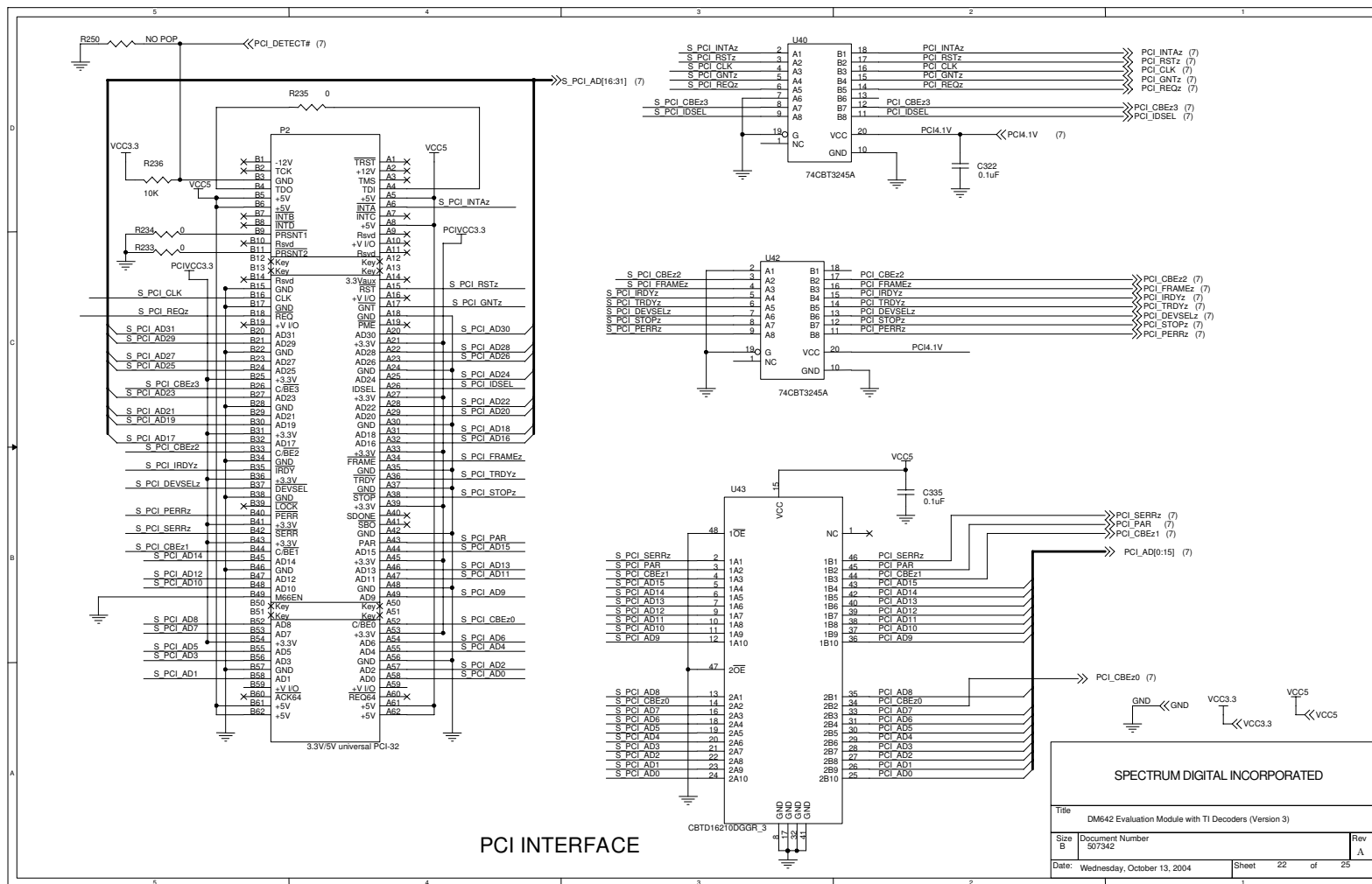


Video Input Section (Channel 2)

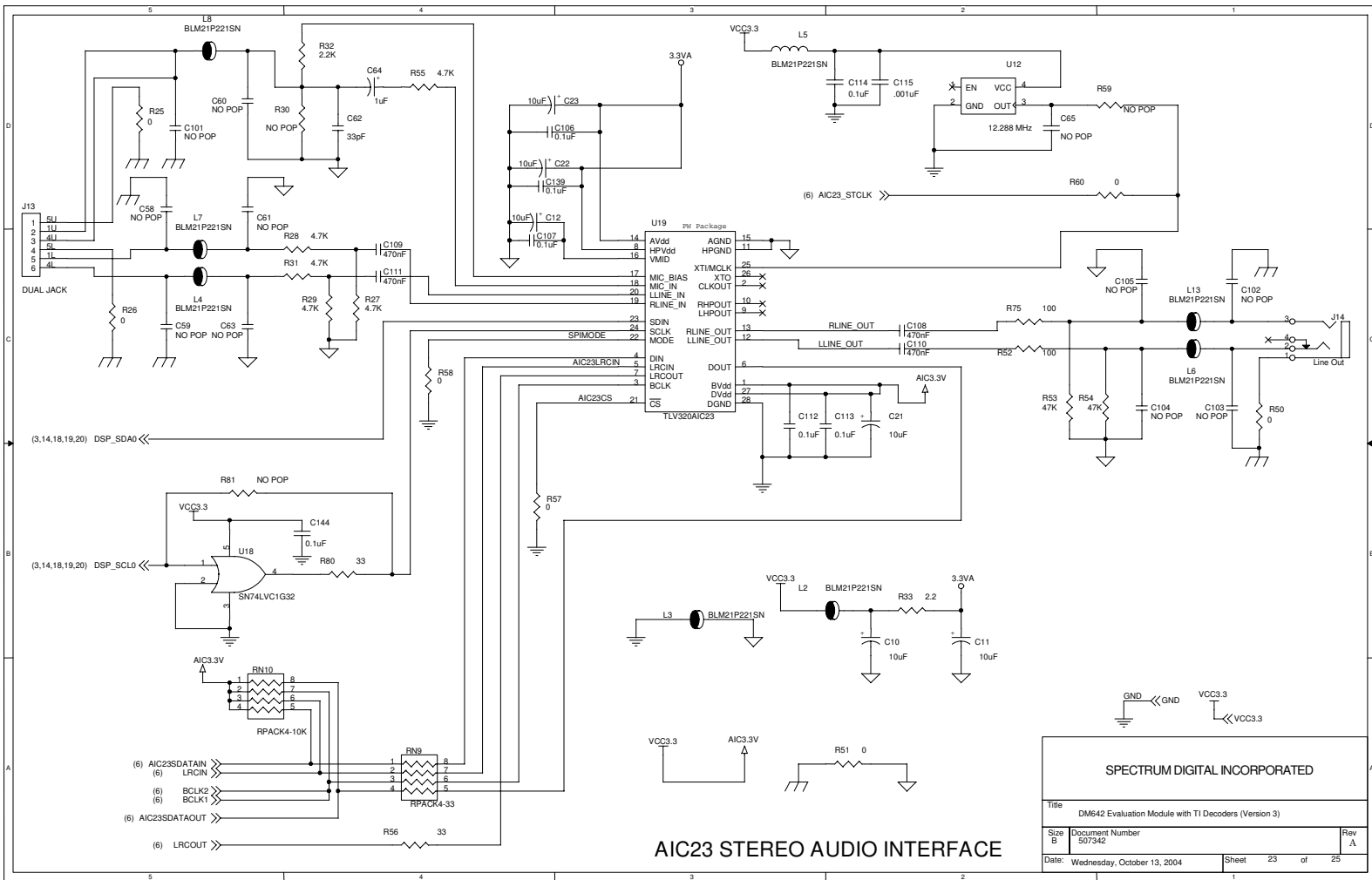
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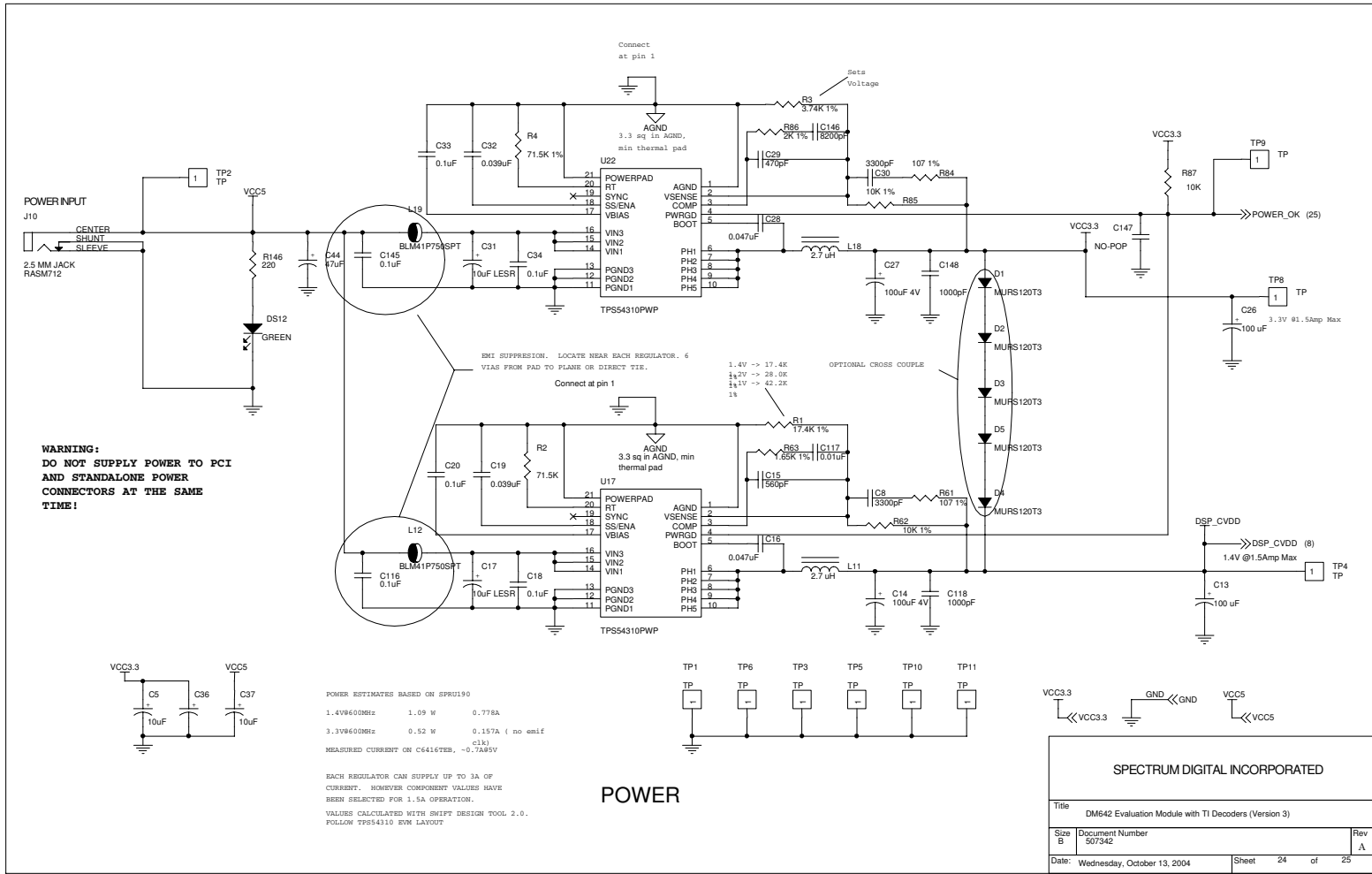


AIC23 STEREO AUDIO INTERFACE

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TMS320DM642 EVM Technical Reference



WARNING:
DO NOT SUPPLY POWER TO PCI
AND STANDALONE POWER
CONNECTORS AT THE SAME
TIME!

POWER ESTIMATES BASED ON SPRU190

1.4V@60MHz	1.09 W	0.778A
3.3V@60MHz	0.52 W	0.157A (no emif c33)

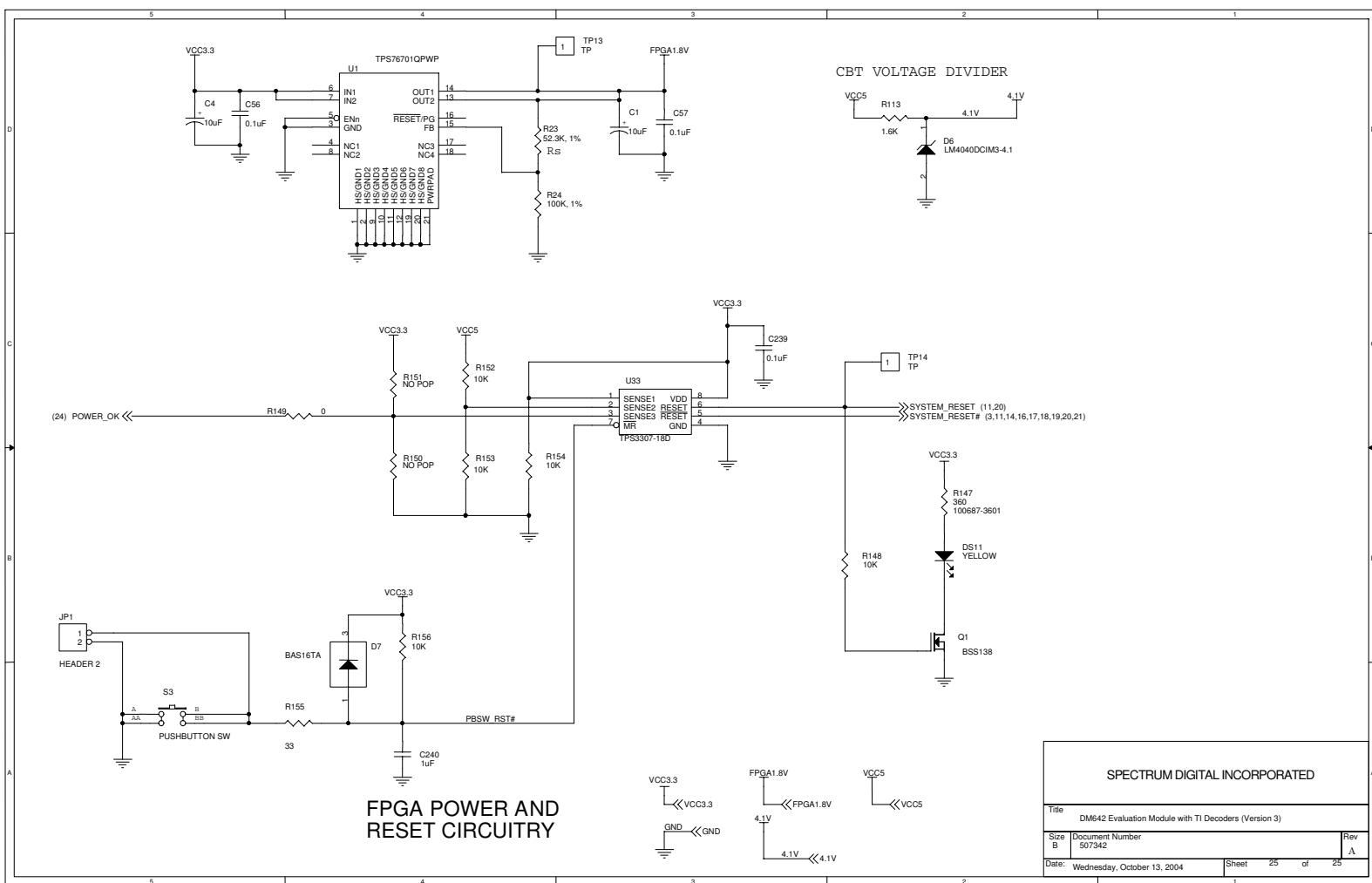
MEASURED CURRENT ON C6416TES, =0.7A@5V

EACH REGULATOR CAN SUPPLY UP TO 3A OF CURRENT. HOWEVER COMPONENT VALUES HAVE BEEN SELECTED FOR 1.5A OPERATION. VALUES CALCULATED WITH SWIFT DESIGN TOOL 2.0. FOLLOW TPS54310 EVM LAYOUT

POWER

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Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320DM642 EVM produced by Spectrum Digital.

