

## 144-pin SDRAM Modules HELIOS3 – Professional Line

SO-DIMM 256MB PC133 / 100 in COB Technique – RoHS complaint

### Options:

|         |                |
|---------|----------------|
| Grade C | 0°C to +70°C   |
| Grade E | 0°C to +85°C   |
| Grade I | -25°C to +85°C |
| Grade W | -40°C to +85°C |

### Features:

- 144-pin 64-bit Small Outline Dual-In-Line Synchronous DRAM Modules for notebook applications
- SDRAM component base:  
MICRON MT48LC16M8A2 Y15W
- Single +3.3V ( $\pm 0.3V$ ) power supply
- Programmable CAS Latency, Burst Length, and Wrap Sequence
- Auto Refresh (CBR) and Self Refresh
- 4k Refresh every 64ms
- All inputs and outputs are LVTTTL compatible
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module family is fully pin and functional compatible with the INTEL SO-DIMM specification. (see [www.intel.com](http://www.intel.com))
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

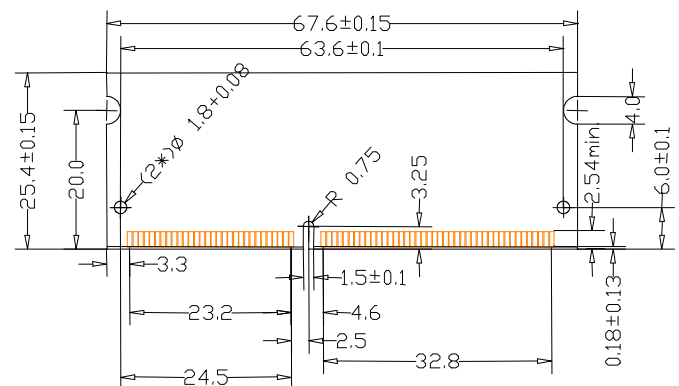


Figure 1: Mechanical Dimensions

### Environmental Requirements

|                                 |                                             |
|---------------------------------|---------------------------------------------|
| Operating Temperature (ambient) |                                             |
| Grade C                         | 0°C to +70°C                                |
| Grade E                         | 0°C to +85°C                                |
| Grade I                         | -25°C to + 85°C                             |
| Grade W                         | -40°C to +85°C                              |
| Operating Humidity              | 10% to 90% relative humidity, noncondensing |
| Operating Pressure              | 10106 PSI (up to 10000 ft.)                 |
| Storage Temperature             | -40°C to 90°C                               |
| Storage Humidity                | 5% to 95% without condensing                |
| Storage Pressure                | 1682 PSI (up to 5000 ft.) at 50°C           |

This Swissbit Germany module family are industry standard 144-pin 8-byte Synchronous SDRAM Small Outline Dual-In-line Memory Modules (SO-DIMMs) which are organized as x 64 high speed memory arrays designed for use in non parity applications. These SO-DIMMs are assembled in Chip-On-Board Technology. The passive devices and the EEPROMs are SMD components.

The DIMMs use optional serial presence detects (SPD) implemented via serial EEPROM using the two pin I<sup>2</sup>C protocol . The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit Germany SO-DIMMs provide a high performance, flexible 8-byte interface in a 67.6 mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

### Module Configuration

| Organsisation | SDRAMs used  | Row Addr. | Bank Select | Col. Addr. | Refresh | Module Dimensions        |
|---------------|--------------|-----------|-------------|------------|---------|--------------------------|
| 32M x 64      | 16 x 16M x 8 | 12        | BA0, BA1    | 10         | 4k      | 67.60 x 25.40 x 3.80 max |

### Product Spectrum

| Part Number                  | Speed Grade | Refresh/ Period | Note      |
|------------------------------|-------------|-----------------|-----------|
| SSN03264O3B32MT-70[C/E/I/W]R | 133-222     | 4k / 64ms       | PC133 CL2 |
| SSN03264O3B32MT-75[C/E/I/W]R | 133-333     | 4k / 64ms       | PC133 CL3 |
| SSN03264O3B32MT-08[C/E/I/W]R | 100-222     | 4k / 64ms       | PC100 CL2 |

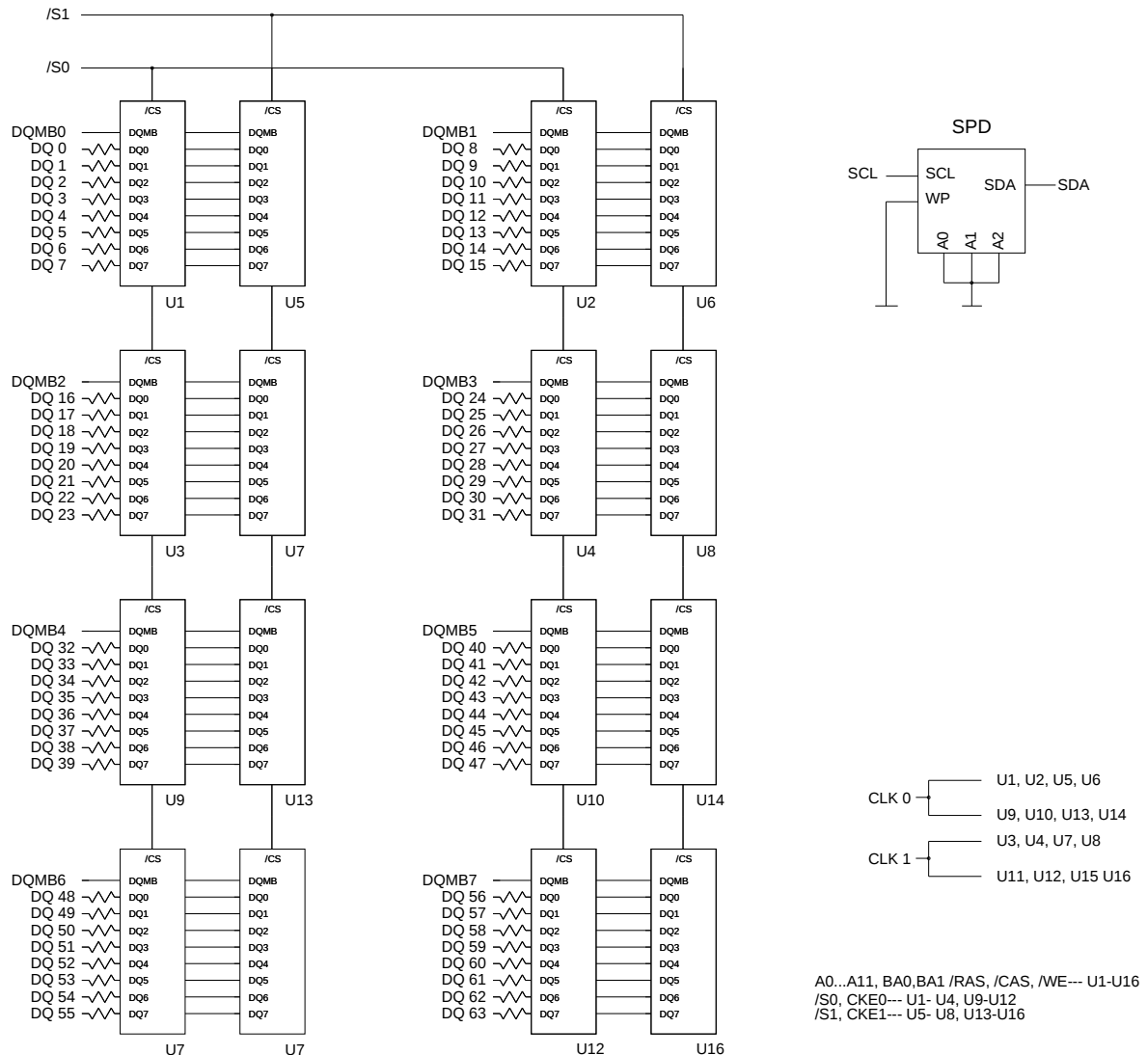
### Pin Name

|               |                                     |
|---------------|-------------------------------------|
| A0 – A12      | Address Inputs                      |
| BA0, BA1      | Bank Selects                        |
| DQ0 – DQ63    | Data Input/Output                   |
| RAS#          | Row Address Strobe                  |
| CAS#          | Column Address Strobe               |
| WE#           | Read / Write Enable                 |
| CKE0 – CKE1   | Clock Enable                        |
| CLK0 – CLK1   | Clock Input                         |
| DQMB0 – DQMB7 | Data Mask                           |
| S0#, S1#      | Chip Select                         |
| Vcc           | Power (+3.3V)                       |
| Vss           | Ground                              |
| SCL           | Clock for Presence Detect           |
| SDA           | Serial Data Out for Presence Detect |
| NC            | No Connection                       |

**Pin Configuration**

| PIN # | Front Side | PIN # | Back Side |  | PIN # | Front Side | PIN # | Back Side |
|-------|------------|-------|-----------|--|-------|------------|-------|-----------|
| 1     | Vss        | 2     | Vss       |  | 73    | NC         | 74    | CLK1      |
| 3     | DQ0        | 4     | DQ32      |  | 75    | Vss        | 76    | Vss       |
| 5     | DQ1        | 6     | DQ33      |  | 77    | NC         | 78    | NC        |
| 7     | DQ2        | 8     | DQ34      |  | 79    | NC         | 80    | NC        |
| 9     | DQ3        | 10    | DQ35      |  | 81    | Vcc        | 82    | Vcc       |
| 11    | Vcc        | 12    | Vcc       |  | 83    | DQ16       | 84    | DQ48      |
| 13    | DQ4        | 14    | DQ36      |  | 85    | DQ17       | 86    | DQ49      |
| 15    | DQ5        | 16    | DQ37      |  | 87    | DQ18       | 88    | DQ50      |
| 17    | DQ6        | 18    | DQ38      |  | 89    | DQ19       | 90    | DQ51      |
| 19    | DQ7        | 20    | DQ39      |  | 91    | Vss        | 92    | Vss       |
| 21    | Vss        | 22    | Vss       |  | 93    | DQ20       | 94    | DQ52      |
| 23    | DQMB0      | 24    | DQMB4     |  | 95    | DQ21       | 96    | DQ53      |
| 25    | DQMB1      | 26    | DQMB5     |  | 97    | DQ22       | 98    | DQ54      |
| 27    | Vcc        | 28    | Vcc       |  | 99    | DQ23       | 100   | DQ55      |
| 29    | A0         | 30    | A3        |  | 101   | Vcc        | 102   | Vcc       |
| 31    | A1         | 32    | A4        |  | 103   | A6         | 104   | A7        |
| 33    | A2         | 34    | A5        |  | 105   | A8         | 106   | BA0       |
| 35    | Vss        | 36    | Vss       |  | 107   | Vss        | 108   | Vss       |
| 37    | DQ8        | 38    | DQ40      |  | 109   | A9         | 110   | BA1       |
| 39    | DQ9        | 40    | DQ41      |  | 111   | A10        | 112   | A11       |
| 41    | DQ10       | 42    | DQ42      |  | 113   | Vcc        | 114   | Vcc       |
| 43    | DQ11       | 44    | DQ43      |  | 115   | DQMB2      | 116   | DQMB6     |
| 45    | Vcc        | 46    | Vcc       |  | 117   | DQMB3      | 118   | DQMB7     |
| 47    | DQ12       | 48    | DQ44      |  | 119   | Vss        | 120   | Vss       |
| 49    | DQ13       | 50    | DQ45      |  | 121   | DQ24       | 122   | DQ56      |
| 51    | DQ14       | 52    | DQ46      |  | 123   | DQ25       | 124   | DQ57      |
| 53    | DQ15       | 54    | DQ47      |  | 125   | DQ26       | 126   | DQ58      |
| 55    | Vss        | 56    | Vss       |  | 127   | DQ27       | 128   | DQ59      |
| 57    | NC         | 58    | NC        |  | 129   | Vcc        | 130   | Vcc       |
| 59    | NC         | 60    | NC        |  | 131   | DQ28       | 132   | DQ60      |
| 61    | CLK0       | 62    | CKE0      |  | 133   | DQ29       | 134   | DQ61      |
| 63    | Vcc        | 64    | Vcc       |  | 135   | DQ30       | 136   | DQ62      |
| 65    | RAS#       | 66    | CAS#      |  | 137   | DQ31       | 138   | DQ63      |
| 67    | WE#        | 68    | CKE1      |  | 139   | Vss        | 140   | Vss       |
| 69    | S0#        | 70    | A12       |  | 141   | SDA        | 142   | SCL       |
| 71    | S1#        | 72    | NC        |  | 143   | Vcc        | 144   | Vcc       |

# Functional Block Diagramm 256MB SODIMM SDRAM Module, 2 Ranks with 8 Components



Note All resistor values are 10 ohms unless otherwise specified

**DC Characteristics**
 $T_A = 0$  to  $70^{\circ}\text{C}$ ;  $V_{SS} = 0\text{V}$ ;  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$  (see General Notes on page 8)

| Parameter                                                                                         | Symbol     | Min. Limit | Max. Limit     | Unit          |
|---------------------------------------------------------------------------------------------------|------------|------------|----------------|---------------|
| Input high voltage                                                                                | $V_{IH}$   | 2.0        | $V_{CC} + 0.3$ | V             |
| Input low voltage                                                                                 | $V_{IL}$   | - 0.3      | 0.8            | V             |
| Output high voltage                                                                               | $V_{OH}$   | 2.4        | -              | V             |
| Output low voltage                                                                                | $V_{OL}$   | -          | 0.4            | V             |
| Input leakage current, any input<br>( $0\text{V} < V_{IN} < 3.6\text{V}$ , all other inputs = 0V) | $I_{I(L)}$ | - 5        | 5              | $\mu\text{A}$ |
| Output leakage current<br>(DQ is disabled, $0\text{V} < V_{OUT} < V_{CC}$ )                       | $I_{O(L)}$ | - 5        | 5              | $\mu\text{A}$ |

**Capacitance**
 $T_A = 0$  to  $70^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ;  $f = 1\text{MHz}$  (see General Notes on page 8)

| Parameter                                | Symbol    | Max. Limit | Unit |
|------------------------------------------|-----------|------------|------|
| Input capacitance (A0 to A11, BA0, BA1)  | $C_{I1}$  | 75         | pF   |
| Input capacitance (/RAS, /CAS, /WE,)     | $C_{I2}$  | 75         | pF   |
| Input capacitance (CLK0, CLK1)           | $C_{I3}$  | 35         | pF   |
| Input capacitance (CS0, CS1, CKE0, CKE1) | $C_{I4}$  | 40         | pF   |
| Input capacitance (DQMB0 - DQMB7)        | $C_{I5}$  | 12         | pF   |
| Input capacitance (DQ0 - DQ63)           | $C_{I10}$ | 18         | pF   |
| Input capacitance (SCL, SA0-2)           | $C_{SC}$  | 10         | pF   |
| Input/Output capacitance                 | $C_{sd}$  | 20         | pF   |

**Operating Currents**

( $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ) (see General Notes on page 8)

(Recommended Operating Conditions unless otherwise noted)

| Parameter<br>& Test Condition                                                                                                                                                                             | Symbol | 133-222          | 133-333          | 100-222          | Unit | Note |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------------|------------------|------------------|------|------|
| Operating Current*)<br>trc=trcmin., tck=tckmin.<br>Outputs open,<br>Burst Length = 2<br>All banks operated in random access,<br>all banks operated in ping-pong manner<br>to maximize gapless data access | Icc1   | CL=2<br><br>1296 | CL=3<br><br>1216 | CL=2<br><br>1216 | mA   | 1    |
| Precharge Standby Current in<br>Power Down Mode<br>/CS = VIH (min), CKE<=VIH(min)                                                                                                                         | Icc2   | 32               | 32               | 32               | mA   | 1    |
| Precharge Standby Current in<br>Non Power Down Mode<br>CS = VIH (min),<br>CKE = Low                                                                                                                       | Icc3   | 416              | 416              | 416              | mA   | 1    |
| Burst Operating Current*)<br>tck = min.,<br>Read command cycling                                                                                                                                          | Icc4   | 1336             | 1216             | 1216             | mA   | 1,2  |
| Auto Refresh Current<br>CS; CKE = high<br>$t_{RFC} = t_{RFC(min)}$                                                                                                                                        | Icc5   | 5280             | 4960             | 4960             | mA   | 1    |
| Auto Refresh Current<br>tck = min.<br>Auto Refresh command cycling                                                                                                                                        | Icc6   | 48               | 48               | 48               | mA   | 1    |
| Self Refresh Current<br>Self Refresh Mode,<br>CKE< = 0.2V                                                                                                                                                 | Icc7   | 32               | 32               | 32               | mA   | 1    |

\*)Value calculated as one module rank in this operating condition, and all other module ranks in ICC2 (CKE LOW) mode

**Notes:**

- 1 These parameters depend on the cycle rate. These values are measured at 133MHz for -7 and 100MHz for -8 parts. Input signals are changed once during tck excepts for Icc6 and Icc7.
- 2 These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed.

**AC Characteristics**
 $T_A = 0$  to  $70^\circ\text{C}$ ;  $V_{SS} = 0\text{V}$ ;  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ;  $t_T = 1\text{ns}$  (see General Notes on page 8)

| Parameter                           | Symbol                                                  | Limit Values |     |         |     |         |     | Unit |   |
|-------------------------------------|---------------------------------------------------------|--------------|-----|---------|-----|---------|-----|------|---|
|                                     |                                                         | 133-222      |     | 133-333 |     | 100-222 |     |      |   |
|                                     |                                                         | min          | max | min     | max | min     | max |      |   |
| Clock and Clock Enable              |                                                         |              |     |         |     |         |     |      |   |
| Clock cycle time                    | t <sub>CK</sub>                                         |              |     |         |     |         |     | ns   |   |
| CAS Latency = 3                     |                                                         | 7.0          | -   | 7.5     | -   | 8.0     | -   |      |   |
| CAS Latency = 2                     |                                                         | 7.5          | -   | 10.0    | -   | 10.0    | -   |      |   |
| Clock Frequency                     | f <sub>CK</sub>                                         |              |     |         |     |         |     | MHz  |   |
| CAS Latency = 3                     |                                                         | -            | 143 | -       | 133 | -       | 125 |      |   |
| CAS Latency = 2                     |                                                         | -            | 133 | -       | 100 | -       | 100 |      |   |
| Access Time from Clock              | t <sub>AC</sub>                                         |              |     |         |     |         |     | ns   |   |
| CAS Latency = 3                     |                                                         | -            | 5.4 | -       | 5.4 | -       | 6.0 |      |   |
| CAS Latency = 2                     |                                                         | -            | 5.4 | -       | 6.0 | -       | 6.0 |      |   |
| Clock low-level width               | t <sub>CL</sub>                                         | 2.5          | -   | 2.5     | -   | 2.5     | -   | ns   |   |
| Clock high-level width              | t <sub>CH</sub>                                         | 2.5          | -   | 2.5     | -   | 2.5     | -   | ns   |   |
| Transition Time                     | t <sub>T</sub>                                          | 0.3          | 1.2 | 0.3     | 1.2 | 0.3     | 1.2 | ns   |   |
| Setup and Hold Times                |                                                         |              |     |         |     |         |     |      |   |
| Setup Times                         | t <sub>AS</sub> , t <sub>CKS</sub> , t <sub>CMS</sub> , | 1.5          |     | 1.5     |     | 2.0     |     | ns   |   |
| t <sub>DS</sub>                     |                                                         | 0.8          |     | 0.8     |     | 1.0     |     | ns   |   |
| Hold Times                          | t <sub>AH</sub> , t <sub>CKH</sub> , t <sub>CMH</sub> , |              |     |         |     |         |     |      |   |
| t <sub>DH</sub>                     |                                                         |              |     |         |     |         |     |      |   |
| Common Parameters                   |                                                         |              |     |         |     |         |     |      |   |
| Active to Precharge                 | t <sub>RAS</sub>                                        | 37           |     | 44      |     | 50      |     | ns   |   |
| (Row Active Time)                   |                                                         |              | 120 |         | 120 |         | 120 | ms   |   |
| Active to Active Command Period     | t <sub>RC</sub>                                         | 60           |     | 66      |     | 70      |     | ns   | 1 |
| (Row Cycle Time)                    |                                                         |              |     |         |     |         |     |      |   |
| Active to Read or Write             | t <sub>RCD</sub>                                        | 15           |     | 20      |     | 20      |     | ns   |   |
| (Row to Column Delay Time)          |                                                         |              |     |         |     |         |     |      |   |
| Precharge to Active                 | t <sub>RP</sub>                                         | 15           |     | 20      |     | 20      |     | ns   | 1 |
| (Row Precharge Time)                |                                                         |              |     |         |     |         |     |      |   |
| Active A to Active B Command Period | t <sub>RRD</sub>                                        | 14           |     | 15      |     | 20      |     | ns   |   |
| Read / Write Cmd to Read / Write    | t <sub>CCD</sub>                                        | 1            |     | 1       |     | 1       |     | CLK  |   |
| (CAS A to CAS B Cmd Period)         |                                                         |              |     |         |     |         |     |      |   |
| Write Recovery                      | t <sub>WR</sub>                                         |              |     |         |     |         |     |      |   |
| Auto Precharge Mode                 |                                                         | + 7.0        |     | + 7.5   |     | + 7.0   |     | ns   | 2 |
| Precharge Mode                      |                                                         | 14           |     | 15      |     | 15      |     | ns   |   |
| Last Data-In to Precharge           | t <sub>RDL</sub>                                        | 2            |     | 2       |     | 2       |     | CLK  |   |

| Parameter                                               | Symbol            | Limit Values |     |         |     |         |     | Unit |   |
|---------------------------------------------------------|-------------------|--------------|-----|---------|-----|---------|-----|------|---|
|                                                         |                   | 133-222      |     | 133-333 |     | 100-222 |     |      |   |
|                                                         |                   | min          | max | min     | max | min     | max |      |   |
| Refresh Cycle                                           |                   |              |     |         |     |         |     |      |   |
| Refresh Period<br>(Standard Refresh)                    |                   |              | 64  |         | 64  |         | 64  | ms   |   |
| Exit Self Refresh to Active<br>(Self Refresh Exit Time) | t <sub>XSR</sub>  | 67           |     | 75      |     | 80      |     | ns   | 3 |
| Auto Refresh Period                                     | t <sub>RFC</sub>  | 66           |     | 66      |     | 70      |     | ns   |   |
| Power On / Down                                         |                   |              |     |         |     |         |     |      |   |
| CKE to Clock disable or Power Down entry                | t <sub>CKED</sub> | 1            |     | 1       |     | 1       |     | CLK  |   |
| CKE to Clock enable or Power Down exit                  | t <sub>PED</sub>  | 1            |     | 1       |     | 1       |     | CLK  |   |
| Load Mode Register to Active                            | t <sub>MRD</sub>  | 2            |     | 2       |     | 2       |     | CLK  |   |

#### Notes

- 1 at the same bank
- 2 after 1 Clock
- 3 Clock active

#### General Notes

An initial pause of 100µs with stable clock is required after power-up, then a Precharge All Bank command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.

AC timing tests have  $V_{il} = 0.4V$  and  $V_{ih} = 2.4V$  with timing referenced to the 1.4V crossover point. The transition time is measured between  $V_{ih}$  and  $V_{il}$ . All AC measurements assume  $t_T = 1ns$ .

Specified  $t_{ac}$  parameters are measured with a 50pF load only.

Self Refresh Exit is a synchronous operation and begins on the 2<sup>nd</sup> positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to  $t_{RC}$  is satisfied once the Self Refresh Exit command is registered.

Values for AC timing,  $I_{CC}$ , and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

**SPD Table**

| Byte # | Description                                      |                   | 133-222 | 133-333 | 100-222 |
|--------|--------------------------------------------------|-------------------|---------|---------|---------|
| 0      | Number of SPD bytes                              |                   | 0x80    |         |         |
| 1      | Total bytes in SPD                               |                   | 0x08    |         |         |
| 2      | Memory Type                                      |                   | 0x04    |         |         |
| 3      | Number of Rows                                   |                   | 0x0c    |         |         |
| 4      | Number of Columns                                |                   | 0x0a    |         |         |
| 5      | Number of DIMM Banks                             |                   | 0x02    |         |         |
| 6      | Module Data Width                                |                   | 0x40    |         |         |
| 7      | Module Data Width cont.                          |                   | 0x00    |         |         |
| 8      | Module Interface Level                           |                   | 0x01    |         |         |
| 9      | SDRAM Cycle Time at CL=3                         |                   | 0x70    | 0x75    | 0x80    |
| 10     | SDRAM Access Time from CLK at CL=3               |                   | 0x54    | 0x54    | 0x60    |
| 11     | DIMM Configuration                               |                   | 0x00    |         |         |
| 12     | Refresh Rate / Type                              |                   | 0x80    |         |         |
| 13     | SDRAM width, Primary                             |                   | 0x08    |         |         |
| 14     | Error Checking SDRAM data width                  |                   | 0x00    |         |         |
| 15     | Min. clk delay for back to back rand. col. Addr. |                   | 0x01    |         |         |
| 16     | Burst Length supported                           |                   | 0x8f    |         |         |
| 17     | Number of SDRAM banks                            |                   | 0x04    |         |         |
| 18     | Supported CAS Latencies                          |                   | 0x06    |         |         |
| 19     | CS Latencies                                     |                   | 0x01    |         |         |
| 20     | WE Latencies                                     |                   | 0x01    |         |         |
| 21     | SDRAM DIMM attributes                            |                   | 0x00    |         |         |
| 22     | SDRAM Device Attributes                          |                   | 0x0e    |         |         |
| 23     | SDRAM Cycle Time at CL=2                         |                   | 0x75    | 0xa0    | 0xa0    |
| 24     | SDRAM Access Time from Clk at CL=2               |                   | 0x54    | 0x60    | 0x60    |
| 25     | SDRAM Cycle Time at CL=1                         |                   | 0x00    |         |         |
| 26     | SDRAM Access Time from Clk at CL=1               |                   | 0x00    |         |         |
| 27     | Min. Row Precharge Time                          | t <sub>RP</sub>   | 0x0f    | 0x14    | 0x14    |
| 28     | Min. Row Active to Row Active delay              | t <sub>R RD</sub> | 0x0e    | 0x0f    | 0x14    |
| 29     | Min. RAS to CAS delay                            | t <sub>R CD</sub> | 0x0f    | 0x14    | 0x14    |
| 30     | Min. RAS Pulse Width                             | t <sub>R AS</sub> | 0x25    | 0x2d    | 0x32    |
| 31     | Module Bank Density                              |                   | 0x20    |         |         |
| 32     | SDRAM Input setup time                           | t <sub>AS</sub>   | 0x15    | 0x15    | 0x20    |
| 33     | SDRAM input hold time                            | t <sub>AH</sub>   | 0x08    | 0x08    | 0x10    |
| 34     | SDRAM data input setup time                      | t <sub>DS</sub>   | 0x15    | 0x15    | 0x20    |
| 35     | SDRAM data input hold time                       | t <sub>DH</sub>   | 0x08    | 0x08    | 0x10    |
| 36-61  | Superset information                             |                   |         |         |         |
| 62     | SPD Revision                                     |                   | 0x12    |         |         |
| 63     | Checksum for bytes 0 - 62                        |                   | 0x61    | 0xb0    | 0x17    |
| 64     | MANUFACTURER' S JEDEC ID CODE                    |                   | 7F      |         |         |
| 65     | MANUFACTURER' S JEDEC ID CODE                    |                   | 7F      |         |         |
| 66     | MANUFACTURER' S JEDEC ID CODE                    |                   | 7F      |         |         |
| 67     | MANUFACTURER' S JEDEC ID CODE (continued)        |                   | DA      |         |         |
| 126    | Frequency Specification                          |                   | 0x64    |         |         |
| 127    | Details                                          |                   | 0xcf    |         |         |