144-pin SDRAM Modules HELIOS3 – Professional Line

SO-DIMM 128MB PC133 / 100 in COB Technique - RoHS complaint

Options:

Grade C	**0℃ to +70℃**
Grade E	**0℃ to +85℃**
Grade I	**-25℃ to +85℃**
Grade W	**-40℃ to +85℃**

Features:

- 144-pin 64-bit Small Outline Dual-In-Line Synchronous DRAM Modules for industrial applications
- SDRAM component base: MICRON MT48LC16M8A2 Y15W
- Single +3.3V (±0.3V) power supply
- Programmable CAS Latency, Burst Length, and Wrap Sequence
- Auto Refresh (CBR) and Self Refresh
- 4k Refresh every 64ms
- All inputs and outputs are LVTTL compatible
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module family is fully pin and functional compatible with the INTEL SO-DIMM specification. (see www.intel.com)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

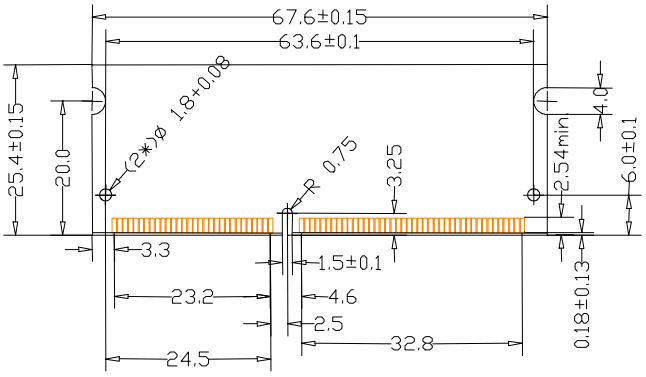


Figure 1: Mechanical Dimensions

Environmental Requirements

Operating Temperature (ambient) Grade C Grade E Grade I Grade W	 0℃ to +70℃ 0℃ to +85℃ -25℃ to + 85℃ -40℃ to +85℃
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10106 PSI (up to 10000 ft.)
Storage Temperature	-40℃ to 70℃
Storage Humidity	5% to 95% without condensing
Storage Pressure	1682 PSI (up to 5000 ft.) at 50℃

This Swissbit Germany module family are industry standard 144-pin 8-byte Synchronous SDRAM Small Outline Dual-In-line Memory Modules (SO-DIMMs) which are organized as x 64 high speed memory arrays designed for use in nonparity applications that requires no ECC function. These SO-DIMMs are assembled in Chip-On-Board Technology. The passive devices and the EEPROMs are SMD components.

The DIMMs use optional serial presence detects (SPD) implemented via serial EEPROM using the two pin I^2C protocol . The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit Germany SO-DIMMs provide a high performance, flexible 8-byte interface in a 67.6 mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

Module Configuration

Organsisation	SDRAMs used	Row Addr.	Bank Select	Col. Addr.	Refresh	Module Dimensions
16M x 64	8 x 16M x 8	12	BA0, BA1	10	4k	67.60 x 25,40 x 3.80 max

Product Spectrum

Part Number	Speed Grade	Refresh/ Period	Note
SSN01664O3B31MT-70[C/E/I/W]R	133-222	4k / 64ms	PC133 CL2
SSN01664O3B31MT -75[C/E/I/W]R	133-333	4k / 64ms	PC133 CL3
SSN01664O3B31MT -08[C/E/I/W]R	100-222	4k / 64ms	PC100 CL2

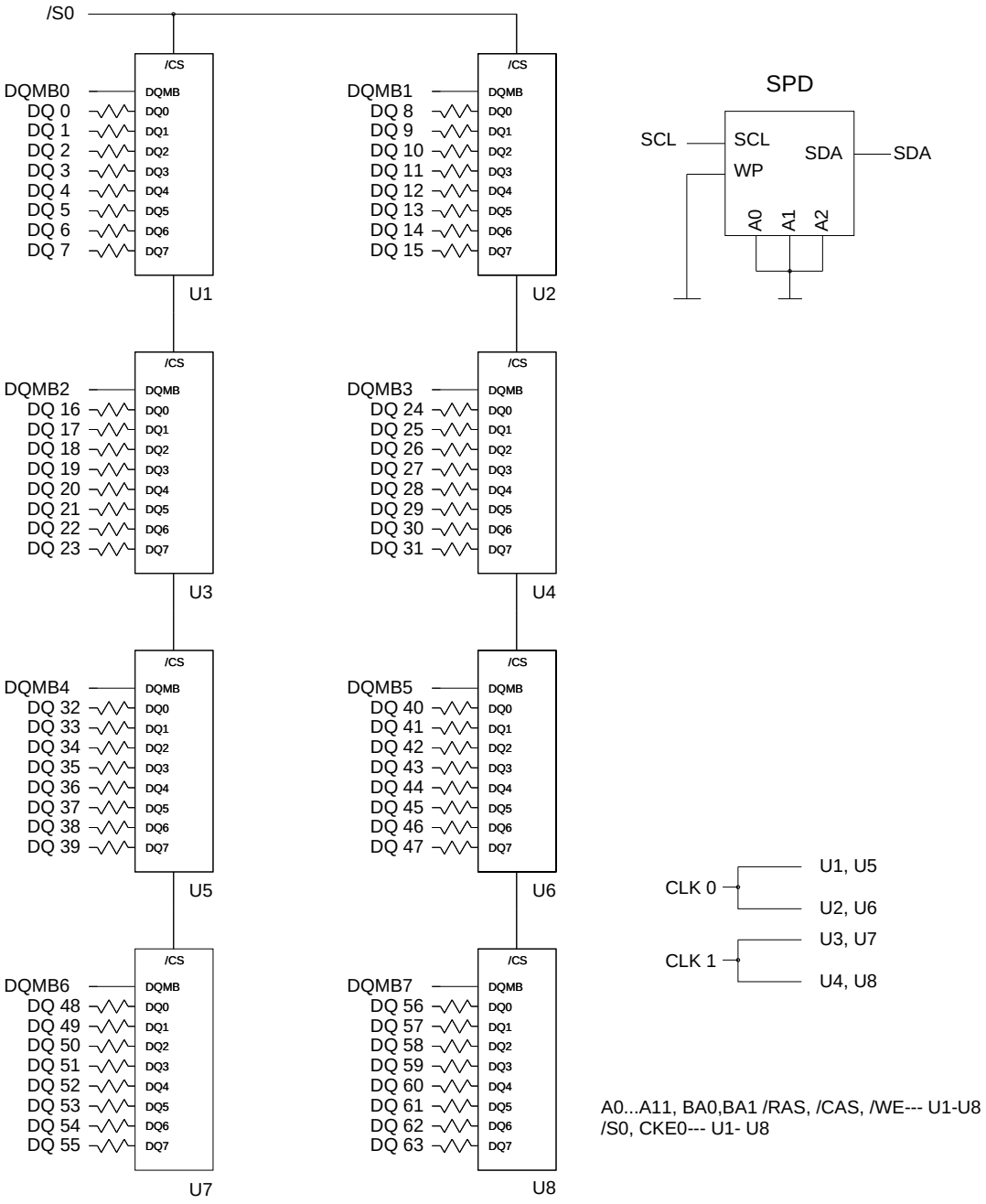
Pin Name

A0 - A11	Address Inputs
BA0, BA1	Bank Selects
DQ0 - DQ63	Data Input/Output
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Read / Write Enable
CKE0 – CKE1	Clock Enable
CLK0 – CLK1	Clock Input
DQMB0 - DQMB7	Data Mask
/S0, /S1	Chip Select
Vcc	Power (+3.3V)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

Pin Configuration

PIN #	Front Side	PIN #	Back Side		PIN #	Front Side	PIN #	Back Side
1	Vss	2	Vss		73	NC	74	CK1
3	DQ0	4	DQ32		75	Vss	76	Vss
5	DQ1	6	DQ33		77	CB2	78	CB6
7	DQ2	8	DQ34		79	CB3	80	CB7
9	DQ3	10	DQ35		81	VDD	82	VDD
11	VDD	12	VDD		83	DQ16	84	DQ48
13	DQ4	14	DQ36		85	DQ17	86	DQ49
15	DQ5	16	DQ37		87	DQ18	88	DQ50
17	DQ6	18	DQ38		89	DQ19	90	DQ51
19	DQ7	20	DQ39		91	Vss	92	Vss
21	Vss	22	Vss		93	DQ20	94	DQ52
23	DQMB0	24	DQMB4		95	DQ21	96	DQ53
25	DQMB1	26	DQMB5		97	DQ22	98	DQ54
27	VDD	28	VDD		99	DQ23	100	DQ55
29	A0	30	A3		101	VDD	102	VDD
31	A1	32	A4		103	A6	104	A7
33	A2	34	A5		105	A8	106	BA0
35	Vss	36	Vss		107	Vss	108	Vss
37	DQ8	38	DQ40		109	A9	110	BA1
39	DQ9	40	DQ41		111	A10	112	A11
41	DQ10	42	DQ42		113	VDD	114	VDD
43	DQ11	44	DQ43		115	DQMB2	116	DQMB6
45	VDD	46	VDD		117	DQMB3	118	DQMB7
47	DQ12	48	DQ44		119	Vss	120	Vss
49	DQ13	50	DQ45		121	DQ24	122	DQ56
51	DQ14	52	DQ46		123	DQ25	124	DQ57
53	DQ15	54	DQ47		125	DQ26	126	DQ58
55	Vss	56	Vss		127	DQ27	128	DQ59
57	CB0	58	CB4		129	VDD	130	VDD
59	CB1	60	CB5		131	DQ28	132	DQ60
61	CK0	62	CKE0		133	DQ29	134	DQ61
63	VDD	64	VDD		135	DQ30	136	DQ62
65	RAS	66	CAS		137	DQ31	138	DQ63
67	WE	68	CKE1		139	Vss	140	Vss
69	S0	70	A12		141	SDA	142	SCL
71	S1	72	NC		143	VDD	144	VDD

Functional Block Diagramm 128MB SODIMM SDRAM Modules,
1 rank and 8 components



Note All resistor values are 10 ohms unless otherwise specified

DC Characteristicts

T_A = 0 to 65℃; Vss = 0V; Vcc = 3.3V +/- 0.3V

Parameter	Symbol	Min. Limit	Max. Limit	Unit
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V
Input low voltage	V_{IL}	- 0.3	0.8	V
Output high voltage	V_{OH}	2.4	-	V
Output low voltage	V_{OL}	-	0.4	V
Input leakage current, any input (0V < V_{IN} < 3.6V, all other inputs = 0V)	$I_{I(L)}$	- 5	5	µA
Output leakage current (DQ is disabled, 0V < V_{OUT} < Vcc)	$I_{O(L)}$	- 5	5	µA

Capacitance

T_A = 0 to 65℃; Vcc = 3.3V +/- 0.3V; f = 1MHz

Parameter	Symbol	Max. Limit	Unit
Input capacitance (A0 to A11, BA0, BA1)	C_{I1}	75	pF
Input capacitance (/RAS, /CAS, /WE,)	C_{I2}	75	pF
Input capacitance (CLK0, CLK1)	C_{I3}	35	pF
Input capacitance (CS0, CS1, CKE0, CKE1)	C_{I4}	40	pF
Input capacitance (DQMB0 - DQMB7)	C_{I5}	12	pF
Input capacitance (DQ0 - DQ63)	C_{IO}	18	pF
Input capacitance (SCL, SA0-2)	C_{SC}	10	pF
Input/Output capacitance	C_{sd}	20	pF

Operating Currents (T_A = 0 to 65℃; Vcc = 3.3V +/- 0.3V)

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition	Symbol	133-222	133-333	100-222	Unit	Note
Operating Current*) trc=trc(min.), tck=tck(min.) Outputs open, Burst Length = 2 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	Icc1	CL=2 1280	CL=3 1200	CL=2 1200	mA	1
Precharge Standby Current in Power Down Mode*) /CS = VIH (min), CKE <= VIH(min)	Icc2	16	16	16	mA	1
Precharge Standby Current in Non Power Down Mode CS = VIH (min), CKE = Low	Icc3	400	400	400	mA	1
Burst Operating Current*) Read command cycling	Icc4	1320	1200	1200	mA	1,2
Auto Refresh Current CS, CKE = high $t_{RFC} = t_{RFC(min)}$	Icc5	2640	2480	2480	mA	1
Auto Refresh Current t_{RFC} = 7.81µs Auto Refresh command cycling	Icc6	24	24	24	mA	1
Self Refresh Current Self Refresh Mode, CKE< = 0.2V	Icc7	16	16	16	mA	1

Notes:

1 These parameters depend on the cycle rate. These values are measured at 133MHz for -7x and 100MHz for -08 parts. Input signals are changed once during tck excepts for Icc6 and Icc7.

2 These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed.

AC Characteristics

T_A = 0 to 65℃; Vss = 0V; Vcc = 3.3V +/- 0.3V; t_T = 1ns

Parameter	Symbol	Limit Values						Unit	
		133-222		133-333		100-222			
		min	max	min	max	min	max		
Clock and Clock Enable									
Clock cycle time	t_{CK}							ns	
CAS Latency = 3		7.0	-	7.5	-	8.0	-		
CAS Latency = 2		7.5	-	10.0	-	10.0	-		
Clock Frequency	f_{CK}							MHz	
CAS Latency = 3		-	143	-	133	-	125		
CAS Latency = 2		-	133	-	100	-	100		
Access Time from Clock	t_{AC}							ns	
CAS Latency = 3		-	5.4	-	5.4	-	6.0		
CAS Latency = 2		-	5.4	-	6.0	-	6.0		
Clock low-level width	t_{CL}	2.5	-	2.5	-	2.5	-	ns	
Clock high-level width	t_{CH}	2.5	-	2.5	-	2.5	-	ns	
Transition Time	t_T	0.3	1.2	0.3	1.2	0.3	1.2	ns	
Setup and Hold Times									
Setup Times	t_{AS}, t_{CKS}, t_{CMS}, t_{DS}	1.5		1.5		2.0		ns	
Hold Times	t_{AH}, t_{CKH}, t_{CMH}, t_{DH}	0.8		0.8		1.0		ns	
Common Parameters									
Active to Precharge	t_{RAS}	37		44		50		ns	
(Row Active Time)			120		120		120	ms	
Active to Active Command Period (Row Cycle Time)	t_{RC}	60		66		70		ns	1
Active to Read or Write (Row to Column Delay Time)	t_{RCD}	15		20		20		ns	
Precharge to Active (Row Precharge Time)	t_{RP}	15		20		20		ns	1
Active A to Active B Command Period	t_{RRD}	14		15		20		ns	
Read / Write Cmd to Read / Write (CAS A to CAS B Cmd Period)	t_{CCD}	1		1		1		CLK	
Write Recovery	t_{WR}								
Auto Precharge Mode		+ 7.0		+ 7.5		+ 7.0		ns	2
Precharge Mode		14		15		15		ns	
Last Data-In to Precharge	t_{RDL}	2		2		2		CLK	

Parameter	Symbol	Limit Values						Unit	
		133-222		133-333		100-222			
		min	max	min	max	min	max		
Refresh Cycle									
Refresh Period (Standard Refresh)	t_{REF}		64		64		64	ms	
Exit Self Refresh to Active (Self Refresh Exit Time)	t_{XSR}	67		75		80		ns	3
Auto Refresh Period	t_{RFC}	66		66		70		ns	
Power On / Down									
CKE to Clock disable or Power Down entry	t_{CKED}	1		1		1		CLK	
CKE to Clock enable or Power Down exit	t_{PED}	1		1		1		CLK	
Load Mode Register to Active	t_{MRD}	2		2		2		CLK	

Notes

1 at the same bank

2 after 1 Clock

3 Clock active

General Notes

An initial pause of 100µs with stable clock is required after power-up, then a Precharge All Bank command must be given followed by 8 Auto Refesh (CBR) cycles before the Mode Register Set Operation can begin.

AC timing tests have V_{il} = 0.4V and V_{ih} = 2.4V with timing referenced to the 1.4V crossover point.
The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T = 1ns.

Specified t_{ac} parameters are measured with a 50pF load only.

Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the
Self Refresh Exit command is registered .

SPD Table

Byte #	Description		133-222	133-333	100-222
0	Number of SPD bytes		0x80		
1	Total bytes in SPD		0x08		
2	Memory Type		0x04		
3	Number of Rows		0x0c		
4	Number of Columns		0x0a		
5	Number of DIMM Banks		0x01		
6	Module Data Width		0x40		
7	Module Data Width cont.		0x00		
8	Module Interface Level		0x01		
9	SDRAM Cycle Time at CL=3		0x70	0x75	0xa0
10	SDRAM Access Time from CLK at CL=3		0x54	0x54	0x60
11	DIMM Configuration		0x00		
12	Refresh Rate / Type		0x80		
13	SDRAM width, Primary		0x08		
14	Error Checking SDRAM data width		0x00		
15	Min. clk delay for back to back rand. col. Addr.		0x01		
16	Burst Length supported		0x8f		
17	Number of SDRAM banks		0x04		
18	Supported CAS Latencies		0x06		
19	CS Latencies		0x01		
20	WE Latencies		0x01		
21	SDRAM DIMM attributes		0x00		
22	SDRAM Device Attributes		0x0e		
23	SDRAM Cycle Time at CL=2		0x75	0xa0	0xa0
24	SDRAM Access Time from Clk at CL=2		0x54	0x60	0x60
25	SDRAM Cycle Time at CL=1		0x00		
26	SDRAM Access Time from Clk at CL=1		0x00		
27	Min. Row Precharge Time	t_{RP}	0x0f	0x14	0x14
28	Min. Row Active to Row Active delay	t_{RRD}	0x0e	0x0f	0x14
29	Min. RAS to CAS delay	t_{RCD}	0x0f	0x14	0x14
30	Min. RAS Pulse Width	t_{RAS}	0x25	0x2d	0x32
31	Module Bank Density		0x20		
32	SDRAM Input setup time	t_{AS}	0x15	0x15	0x20
33	SDRAM input hold time	t_{AH}	0x08	0x08	0x10
34	SDRAM data input setup time	t_{DS}	0x15	0x15	0x20
35	SDRAM data input hold time	t_{DH}	0x08	0x08	0x10
36-61	Superset information				
62	SPD Revision		0x12		
63	Checksum for bytes 0 - 62		0x60	0xaf	0x16
64	MANUFACTURER' S JEDEC ID CODE		7F		
65	MANUFACTURER' S JEDEC ID CODE		7F		
66	MANUFACTURER' S JEDEC ID CODE		7F		
67	MANUFACTURER' S JEDEC ID CODE		DA		
126	Frequency Specification		0x64		
127	Details		0xcf		