2GB ECC DDR2 – SDRAM DIMM

240 Pin ECC DIMM

SEU02G72T1BH2MT-25R

2GB PC2-6400 in FBGA Technique

RoHS compliant

Options:

- Frequency / Latency — Marking
  - DDR2 800 MHz CL5 — -2A
  - DDR2 800 MHz CL6 — -25
  - DDR2 667 MHz CL5 — -30
  - DDR2 533 MHz CL4 — -37
- Module densities
  2048MB with 18 dies and 2 ranks
- Standard Grade (T_A) 0℃ to 70℃
  (T_C) 0℃ to 85℃
  Grade W (T_A) -40℃ to 85℃
  (T_C) -40℃ to 95℃
-

Environmental Requirements:

- Operating temperature (case)
  Standard Grade 0℃ to 85℃
  Grade W -40℃ to 95℃
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55℃ to 100℃
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50℃

Features:

- 240-pin 72-bit Dual-In-Line Double Data Rate synchronous DRAM Module with ECC support
- DDR2 - SDRAM component base MICRON MT47H128M8 DIE Rev. H
- V_{DD} = 1.8V ±0.2V, V_{DDQ} 1.8V ±0.2V
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- 1.8V I/O (SSTL_18 compatible)
- Serial Presence Detect with EEPROM
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

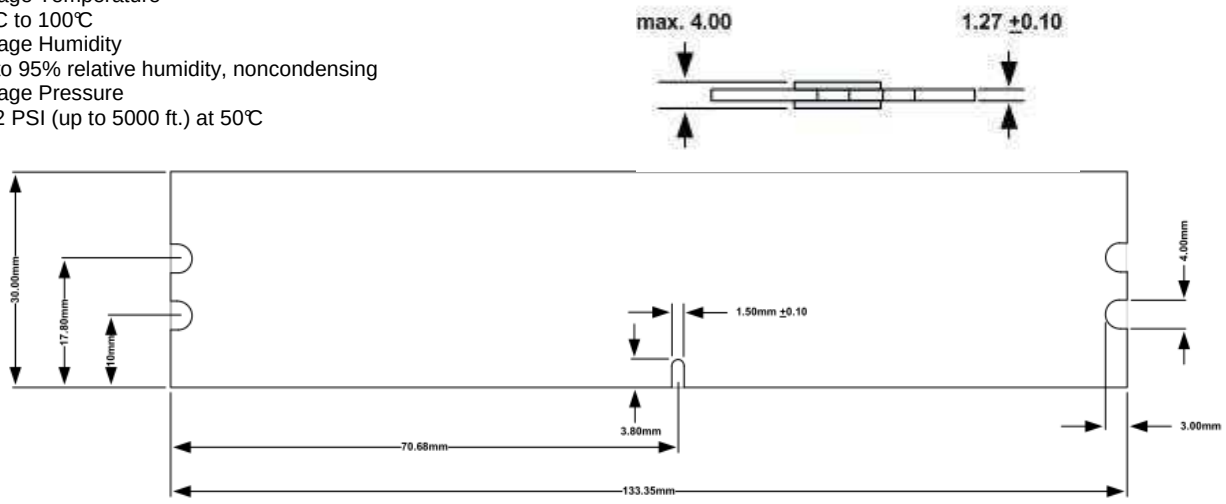


Figure: mechanical dimensions[1]

[1] if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 240-pin 8-byte DDR2 SDRAM Dual-In-line Memory Module (DIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured quad-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.
The DDR2 SDRAM module uses the optional serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Select	Col. Addr.	Refresh	Module Bank Select
256M x 72bit	18 x 128M x 8bit (1Gbit)	14	BA0, BA1,BA2	10	8k	S0#, S1#

Module Dimensions in mm
133.35 (long) x 30(high) x 4 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SEU02G72T1BH2MT-2A[W]R	2048 MB	6.4 GB/s	2.0ns/800MT/s	6400-555
SEU02G72T1BH2MT-25[W]R	2048 MB	6.4 GB/s	2.5ns/800MT/s	6400-666
SEU02G72T1BH2MT-30[W]R	2048 MB	5.3 GB/s	3.0ns/667MT/s	5300-555
SEU02G72T1BH2MT-37[W]R	2048 MB	4.26 GB/s	3.75ns/533MT/s	4200-444

Pin Name

A0-9, A11 – A13	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0, BA1	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK2	Clock Inputs, positive line
CK0# – CK2#	Clock Inputs, negative line

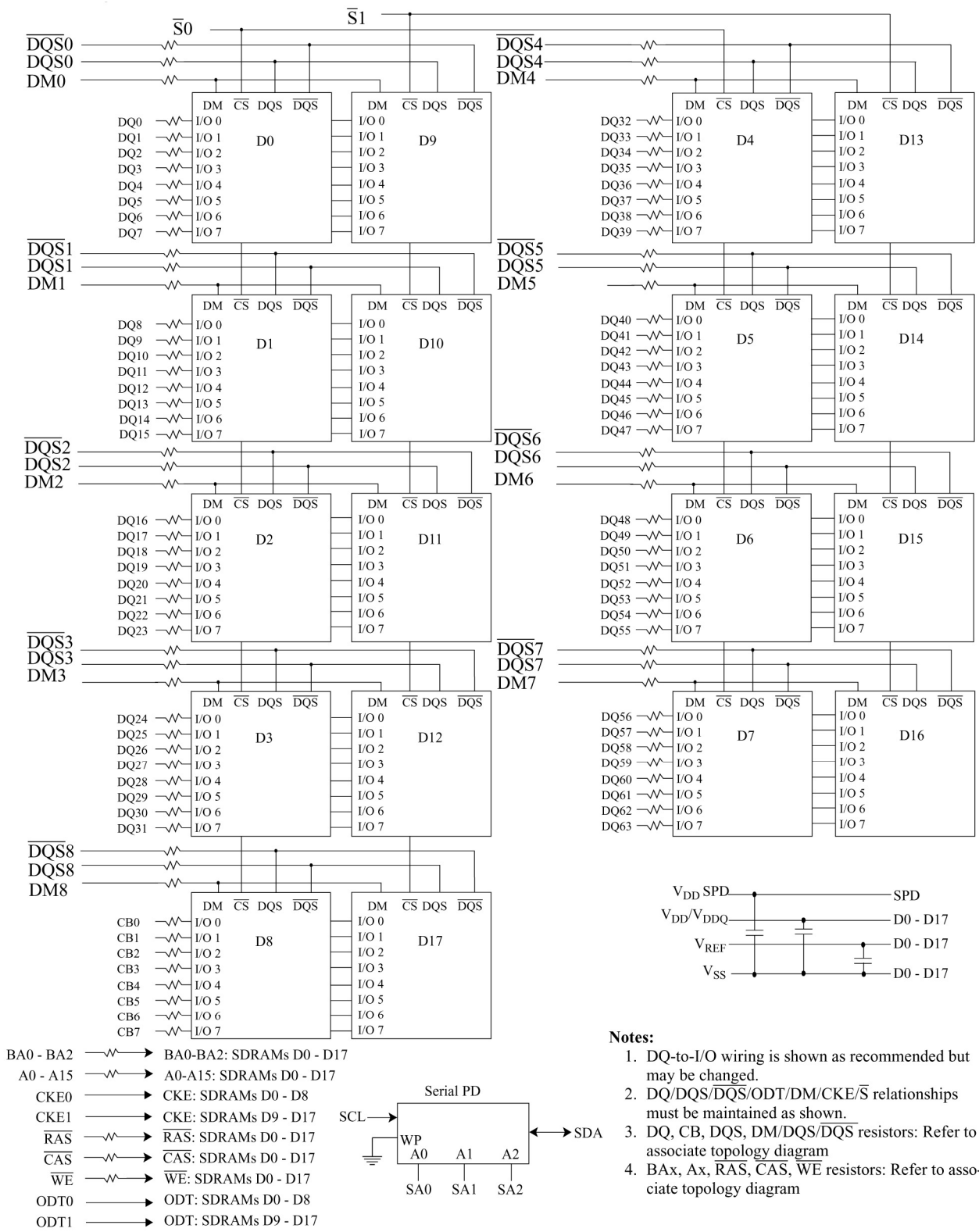
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0#, S1#	Chip Select
V_{DD}	Supply Voltage (1.8V± 0.1V)
V_{REF}	Input / Output Reference
V_{SS}	Ground
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	121	VSS	61	A4	181	VDD
2	VSS	122	DQ4	62	VDD	182	A3
3	DQ0	123	DQ5	63	A2	183	A1
4	DQ1	124	VSS	64	VDD	184	VDD
5	VSS	125	DM0	65	VSS	185	CK0
6	DQS0#	126	NC	66	VSS	186	CK0#
7	DQS0	127	VSS	67	VDD	187	VDD
8	VSS	128	DQ6	68	NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDD
12	DQ8	132	DQ13	72	VDD	192	RAS#
13	DQ9	133	VSS	73	WE#	193	CS0#
14	VSS	134	DM1	74	CAS#	194	VDD
15	DQS1#	135	NC	75	VDD	195	ODT0
16	DQS1	136	VSS	76	CS1#	196	A13
17	VSS	137	CK1	77	ODT1	197	VDD
18	NC	138	CK1#	78	VDD	198	VSS
19	NC	139	VSS	79	VSS	199	DQ36
20	VSS	140	DQ14	80	DQ32	200	DQ37
21	DQ10	141	DQ15	81	DQ33	201	VSS
22	DQ11	142	VSS	82	VSS	202	DM4
23	VSS	143	DQ20	83	DQS4#	203	NC
24	DQ16	144	DQ21	84	DQS4	204	VSS
25	DQ17	145	VSS	85	VSS	205	DQ38
26	VSS	146	DM2	86	DQ34	206	DQ39
27	DQS2#	147	NC	87	DQ35	207	VSS
28	DQS2	148	VSS	88	VSS	208	DQ44
29	VSS	149	DQ22	89	DQ40	209	DQ45
30	DQ18	150	DQ23	90	DQ41	210	VSS
31	DQ19	151	VSS	91	VSS	211	DM5
32	VSS	152	DQ28	92	DQS5#	212	NC

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
33	DQ24	153	DQ29	93	DQS5	213	VSS
34	DQ25	154	VSS	94	VSS	214	DQ46
35	VSS	155	DM3	95	DQ42	215	DQ47
36	DQS3#	156	NC	96	DQ43	216	VSS
37	DQS3	157	VSS	97	VSS	217	DQ52
38	VSS	158	DQ30	98	DQ48	218	DQ53
39	DQ26	159	DQ31	99	DQ49	219	VSS
40	DQ27	160	VSS	100	VSS	220	CK2
41	VSS	161	NC	101	SA2	221	CK2#
42	NC	162	NC	102	NC	222	VSS
43	NC	163	VSS	103	VSS	223	DM6
44	VSS	164	NC	104	DQS6#	224	NC
45	NC	165	NC	105	DQS6	225	VSS
46	NC	166	VSS	106	VSS	226	DQ54
47	VSS	167	NC	107	DQ50	227	DQ55
48	NC	168	NC	108	DQ51	228	VSS
49	NC	169	VSS	109	VSS	229	DQ60
50	VSS	170	VDD	110	DQ56	230	DQ61
51	VDD	171	CKE1	111	DQ57	231	VSS
52	CKE0	172	VDD	112	VSS	232	DM7
53	VDD	173	NC	113	DQS7#	233	NC
54	NC	174	NC	114	DQS7	234	VSS
55	NC	175	VDD	115	VSS	235	DQ62
56	VDD	176	A12	116	DQ58	236	DQ63
57	A11	177	A9	117	DQ59	237	VSS
58	A7	178	VDD	118	VSS	238	VDDSPD
59	VDD	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

FUNCTIONAL BLOCK DIAGRAMM 2048MB DDR2 SDRAM ECC DIMM, 2 RANKS AND 18 COMPONENTS



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{\text{DQS}}$/ODT/DM/CKE/$\overline{\text{S}}$ relationships must be maintained as shown.
3. DQ, CB, DQS, DM/DQS/$\overline{\text{DQS}}$ resistors: Refer to associate topology diagram
4. BAx, Ax, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ resistors: Refer to associate topology diagram

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{DD}	-1.0	2.3	V
I/O Supply Voltage		$V_{DD}Q$	-0.5	2.3	V
$V_{DD}L$ Supply Voltage		$V_{DD}L$	-0.5	2.3	V
Voltage on any pin relative to V_{SS}		V_{in}, V_{out}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)		I_I			µA
	Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
	CK, CK#		-20	20	
	DM		-5	5	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)		I_{OZ}	-5	5	µA
	DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level		I_{VREF}	-16	16	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	$V_{DD}Q$	1.7	1.8	1.9	V
$V_{DD}L$ Supply Voltage	$V_{DD}L$	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.50 x $V_{DD}Q$	0.51x $V_{DD}Q$	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.125		$V_{DD}Q$ + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.125	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.25	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.25	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition		Symbol	max. 6400-555	max. 6400-666	max. 5300-555	max. 4200-444	Unit
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DDO}	873	873	828	693	mA
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	1053	1053	963	918	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2P}	126	126	126	126	mA
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	900	900	720	720	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	900	900	720	720	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast PDN Exit MR[12] = 0	I_{DD3P}	720	720	540	540	mA
	Slow PDN Exit MR[12] = 1		180	180	180	180	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	1080	1080	990	810	mA

Parameter & Test Condition	Symbol	max.				Unit
		6400-555	6400-666	5300-555	4200-444	
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4R}	1503	1503	1278	1188	mA
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	1503	1503	1278	1188	mA
BURST REFRESH CURRENT: t_{CK} = t_{CK} (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	4230	4230	3870	3780	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	126	126	126	126	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); t_{CK} = t_{CK} (I_{DD}), t_{RC} = t_{RC} (I_{DD}), t_{RRD} = t_{RRD} (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	3078	3078	2583	2493	mA

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS					
SYMBOL	**6400-555**	**6400-666**	**5300-555**	**4200-444**	**Unit**
CL (I_{DD})	5	6	5	4	t_{CK}
t_{RCD} (I_{DD})	12.5	15	15	15	ns
t_{RC} (I_{DD})	57.5	60	60	60	ns
t_{RRD} (I_{DD})	7.5	7.5	7.5	7.5	ns
t_{CK} (I_{DD})	2.5	2.5	3.0	3.75	ns
t_{RAS} MIN (I_{DD})	45	45	45	45	ns
t_{RAS} MAX (I_{DD})	70,000	70,000	70,000	70,000	ns
t_{RP} (I_{DD})	12.5	15	15	15	ns
t_{RFC} (I_{DD})	105	105	105	105	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS			6400-555		6400-666		5300-555		4200-444		Unit
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Clock cycle time	CL = 6	t_{CK} (6)	-	-	2.5	8.0	-	+	-	-	ps
	CL = 5	t_{CK} (5)	2.5	8.0	3.0-	8.0-	3.0	8.0	-	-	ps
	CL = 4	t_{CK} (4)	3.75	8.0	3.75	8.0	3.75	8.0	3.75	8.0	ps
	CL = 3	t_{CK} (3)	5.0	8.0	-	-	5.0	8.0	5.0	8.0	ps
CK high-level width		t_{CH}	0.48	0.52	0.48	0.52	0.45	0.55	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.48	0.52	0.48	0.52	0.45	0.55	0.45	0.55	t_{CK}
Half clock period		t_{HP}	min (t_{CH}, t_{CL})		min (t_{CH}, t_{CL})		min (t_{CH}, t_{CL})		min (t_{CH}, t_{CL})		ps
Access window (output) of DQ_S from CK/CK#		t_{AC}	-0.40	+0.40	-0.40	+0.40	-0.45	+0.45	-0.50	+0.50	ns
Data-out high-impedance window from CK/CK#		t_{HZ}		t_{AC} max		t_{AC} max		+0.45 (= t_{AC} max)		+0.50 (= t_{AC} max)	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	t_{AC} min	t_{AC} max	t_{AC} min	t_{AC} max	-0.45 (= t_{AC} min)	+0.45 (= t_{AC} max)	-0.50 (= t_{AC} min)	+0.50 (= t_{AC} max)	ns
DQ and DM input setup time relative to DQS		t_{DS}	0.05		0.05		0.10		0.10		ns
DQ and DM input hold time relative to DQS		t_{DH}	0.125		0.125		0.30		0.35		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		0.35		0.35		t_{CK}
Data hold skew factor		t_{QHS}		0.3		0.3		0.34		0.4	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns
Data valid output window		t_{DVW}	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		0.35		t_{CK}
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		0.2		0.2		t_{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.2		0.2		0.24		0.30	ns
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
DQS write preamble		t_{WPRE}	0.35		0.35		0.35		0.25		t_{CK}
DQS write preamble setup time		t_{WPRES}	0		0		0		0		ns
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Write command to first DQS latching transition			WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	0.6		0.6		0.6		0.6		t_{CK}
Address and control input setup time		t_{ISa}	0.175		0.175		0.4		0.5		ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-555		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	Min	Max	Min	Max	MIN	MAX	MIN	MAX	
Address and control input hold time	t_{IH}	0.25		0.25		0.4		0.5		ns
CAS# to CAS# command delay	t_{CCD}	2		2		2		2		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	57.5		60		55		55		ns
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	7.5		7.5		7.5		7.5		ns
ACTIVE to READ or WRITE delay	t_{RCD}	12.5		15		15		15		ns
Four bank Activate period	t_{FAW}	37.5		37.5		37.5		37.5		ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	40	70,000	40	70,000	ns
Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		7.5		ns
Write recovery time	t_{WR}	15		15		15		15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		7.5		7.5		ns
PRECHARGE command period	t_{RP}	12.5		15		15		15		ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
LOAD MODE command cycle time	t_{MRD}	2		2		2		2		t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	105	70,000	105	70,000	105	70,000	105	70,000	ns
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8		7.8	µs
Exit SELF REFRESH to non-READ command	t_{XSNR}	t_{RFC}(min) + 10		t_{RFC}(min) + 10		t_{RFC}(min) + 10		t_{RFC}(min) + 10		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		200		t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}		t_{IS}		t_{IS}		t_{IS}		ps
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	t_{AC}(min)	t_{AC}(max) + 1,000	t_{AC}(min)	t_{AC}(max) + 1,000	t_{AC}(min)	t_{AC}(max) + 1,000	t_{AC}(min)	t_{AC}(max) + 1,000	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	ps
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT to power-down entry latency	t_{ANPD}	3		3		3		3		t_{CK}

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0℃ ≤ T_{CASE} ≤ + 85℃; $V_{DD}Q$ = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-555		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	MIN	MAX	Min	Max	MIN	MAX	MIN	MAX	
ODT power-down exit latency	t_{AXPD}	8		8		8		8		t_{CK}
ODT enable from MRS command	T_{MOD}	12		12		12		12		ns
Exit active power-down to READ command, MR [bit 12 = 0]	t_{XARD}	2		2		2		2		t_{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t_{XARDS}	8 – AL		8 – AL		7 – AL		6 – AL		t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2		2		2		2		t_{CK}
CKE minimum high/low time	t_{CKE}	3		3		3		3		t_{CK}

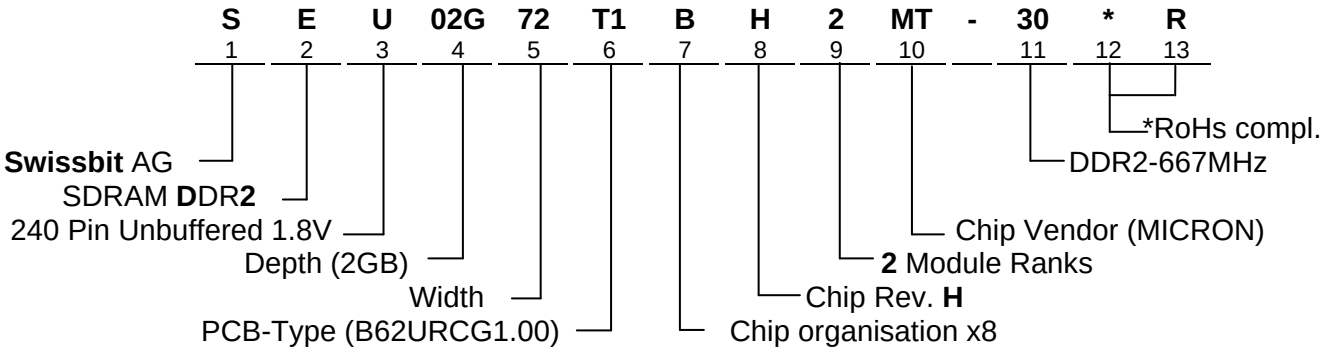
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	6400-555	6400-666	5300-555	4200-444
0	NUMBER OF SPD BYTES USED	0x80			
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08			
2	FUNDAMENTAL MEMORY TYPE	0x08			
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0E			
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A			
5	DIMM HIGHT AND MODULE RANKS	0x61			
6	MODULE DATA WIDTH	0x48			
7	MODULE DATA WIDTH (continued)	0x00			
8	MODULE VOLTAGE INTERFACE LEVELS ($V_{DD}Q$)	0x05			
9	SDRAM CYCLE TIME, (t_{CK}) [max CL] CAS LATENCY = 5 (5300), CL = 4 (4200)	0x25		0x30	0x3D
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) [max CL] CAS LATENCY = 5 (5300); CL = 4 (4200)	0x40		0x45	0x50
11	MODULE CONFIGURATION TYPE	0x02			
12	REFRESH RATE / TYPE	0x82			
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08			
14	ERROR- CHECKING SDRAM DATA WIDTH	0x08			
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00			
16	BURST LENGTHS SUPPORTED	0x0C			
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08			
18	CAS LATENCIES SUPPORTED	0x30	0x70	0x38	0x18
19	MODULE THICKNESS	0x01			
20	DDR2 DIMM TYPE	0x02			
21	SDRAM MODULE ATTRIBUTES	0x00			
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x03			0x01
23	SDRAM CYCLE TIME, (t_{CK}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x3D	0x30	0x3D	0x50
24	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x40		0x45	0x50
25	SDRAM CYCLE TIME, (t_{CK}) [max CL – 2] CAS LATENCY = 3 (5300)	0x00	0x3D	0x50	0x00
26	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 2] CAS LATENCY = 3 (5300)	0x00	0x40	0x45	0x00
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x32	0x3C		
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x1E			
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x32	0x3C		
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x2D			
31	MODULE BANK DENSITY	0x01			

SERIAL PRESENCE-DTECT MATRIX (continued)

BYTE	DESCRIPTION	6400-555	6400-666	5300-555	4200-444
32	ADDRESS AND COMMAND SETUP TIME, (t_{ISb})	0x17		0x20	0x25
33	ADDRESS AND COMMAND HOLD TIME, (t_{IHb})	0x25		0x27	0x37
34	DATA / DATA MASK INPUT SETUP TIME, (t_{DSb})	0x05		0x10	
35	DATA / DATA MASK INPUT HOLD TIME, (t_{DHb})	0x12		0x17	0x22
36	WRITE RECOVERY TIME, (t_{WR})	0x3C			
37	WRITE to READ Command Delay, (t_{WTR})	0x1E			
38	READ to PRECHARGE Command Delay, (t_{RTP})	0x1E			
39	Mem Analysis Probe	0x00			
40	Extension for Bytes 41 and 42	0x36	0x06		
41	MIN ACTIVE AUTO REFRESH TIME, (t_{RC})	0x39	0x3C		
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t_{RFC})	0x7F			
43	SDRAM DEVICE MAX CYCLE TIME, (t_{CKMAX})	0x80			
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t_{DQSQ})	0x14		0x18	0x1E
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t_{QHS})	0x1E		0x22	0x28
46	PLL Relock Time	0x00			
47-61	Optional Features, not supported	0x00			
62	SPD REVISION	0x13			
63	CHECKSUM FOR BYTES 0-62	0x44	0xDB	0x00	0xAB
64-66	MANUFACTURER`S JEDEC ID CODE	0x7F			
67	MANUFACTURER`S JEDEC ID CODE (continued)	0xDA			
68-71	RESERVED	0x00			
72	MANUFACTURING LOCATION	0x01 (Switzerland) | 0x02 (Germany) | 0x03 (USA)			
73-90	MODULE PART NUMBER (ASCII)	"SEU02G72T1BH2MT-xx"			
91	PCB IDENTIFICATION CODE	0x52			
92	IDENTIFICATION CODE (continued)	0x00			
93	YEAR OF MANUFACTURE IN BCD	x			
94	WEEK OF MANUFACTURE IN BCD	x			
95-98	MODULE SERIAL NUMBER	x			
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00			
128-255	Open for customer use	0xff			

Part Number Code



* optional / additional information

Locations

Swissbit AG
Industriestrasse 4 – 8
CH – 9552 Bronschhofen
Switzerland
Phone: +41 (0)71 913 03 03
Fax: +41 (0)71 913 03 15

Swissbit Germany GmbH
Wolfener Strasse 36
D – 12681 Berlin
Germany
Phone: +49 (0)30 93 69 54 – 0
Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.
14 Willett Avenue, Suite 301A
Port Chester, NY 10573
USA
Phone: +1 914 935 1400
Fax: +1 914 935 9865

Swissbit NA, Inc.
3913 Todd Lane, Suite – 307
Austin, TX 78744
USA
Phone: +1 512 302 9001
Fax: +1 512 302 4808

Swissbit Japan, Inc.
3F Core Koenji,
2-1-24 Koenji-Kita, Suginami-Ku,
Tokyo 166-0002
Japan
Phone: +81 3 5356 3511
Fax: +81 3 5356 3512