

This Swissbit module family is industry standard 184-pin 8-byte Double Data rate synchronous SDRAM Dual-In-line Memory Modules (DIMMs), which are organized as x72 high speed memory arrays designed for use in server applications. These DIMMs are assembled in FBGA Technology. The passive devices and the EEPROM are SMD components.

The DIMMs use serial presence detects (SPD) implemented via serial EEPROM using the two-pin-I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit DIMMs provide a high performance, flexible 8-byte interface in a 133,35mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

Module Configuration

Organization	DDR SDRAMs used	Row Addr.	Bank Select	Col. Addr.	Refresh	Module Dimensions in mm
64M x 72	9 x 64M x 8	14	BA0, BA1	12	8k	133,35 max

Product Spectrum

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SDR06472D1B61MT-50R	512MB	3.2 GB/s	5.0ns/400MT/s	3200-333
SDR06472D1B61MT-60R	512MB	2.7 GB/s	6.0ns/333MT/s	2700-2533

Pin Name

A0-A12	Address Inputs
BA0, BA1	Bank Selects
DQ0 – DQ63	Data Input/Output
CB0 - CB7	Check Bits
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Read / Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK2	Clock Inputs, positive line
/CK0 – /CK2	Clock Inputs, negative line
DQS0- DQS17	Data strobes

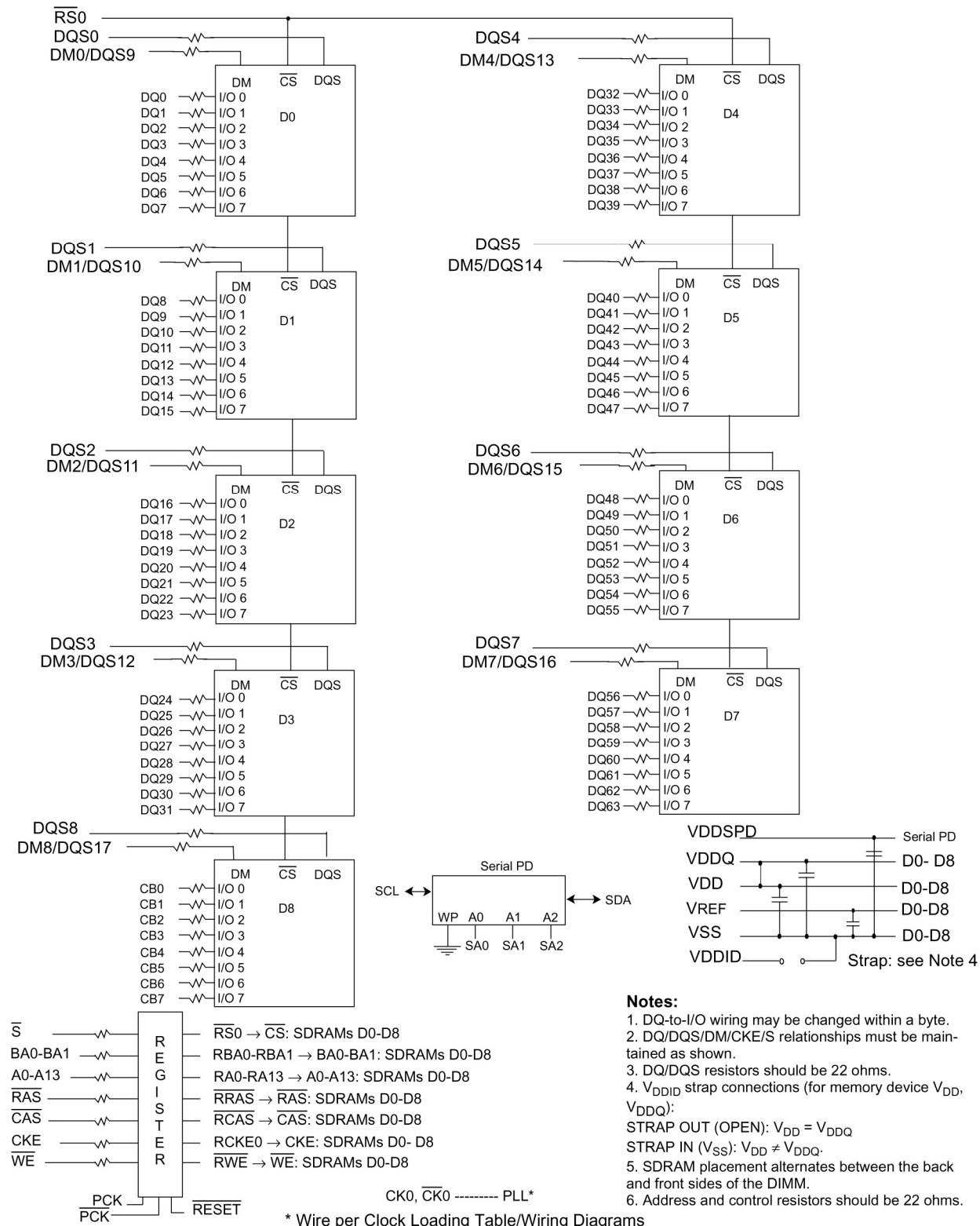
/S0, /S1	Chip Select
V _{DD}	Power (2.5V± 0.2V)
V _{DDQ}	DQ Power (2.5V±0.2V)
V _{DDSPD}	SPD Power
V _{REF}	Input/Output Reference
V _{SS}	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA2	Slave Address Select Bus for Presence Detect
NC	No Connection

Pin Configuration

Front Side				Back Side			
PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name
1	V _{REF}	47	DQS8	93	V _{SS}	139	V _{SS}
2	DQ0	48	A0	94	DQ4	140	DQS17
3	V _{SS}	49	CB2	95	DQ5	141	A10
4	DQ1	50	V _{SS}	96	V _{DDQ}	142	CB6
5	DQS0	51	CB3	97	DQS9	143	V _{DDQ}
6	DQ2	52	BA1	98	DQ6	144	CB7
7	V _{DD}	53	DQ32	99	DQ7	145	V _{SS}
8	DQ3	54	V _{DDQ}	100	V _{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	/Reset	56	DQS4	102	NC	148	V _{DD}
11	V _{SS}	57	DQ34	103	NC	149	DQS13
12	DQ8	58	V _{SS}	104	V _{DDQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V _{SS}
15	V _{DDQ}	61	DQ40	107	DQS10	153	DQ44
16	NC	62	V _{DDQ}	108	V _{DD}	154	/RAS
17	NC	63	/WE	109	DQ14	155	DQ45
18	V _{SS}	64	DQ41	110	DQ15	156	V _{DDQ}
19	DQ10	65	/CAS	111	CKE1	157	/S0
20	DQ11	66	V _{SS}	112	V _{DDQ}	158	/S1
21	CKE0	67	DQS5	113	NC	159	DQS14
22	V _{DDQ}	68	DQ42	114	DQ20	160	V _{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V _{DD}	116	V _{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC

Front Side				Back Side			
PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name	PIN #	PIN Name
26	V _{SS}	72	DQ48	118	A11	164	V _{DDQ}
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	V _{SS}	120	V _{DD}	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	V _{DDQ}	76	NC	122	A8	168	V _{DD}
31	DQ19	77	V _{DDQ}	123	DQ23	169	DQS15
32	A5	78	DQS6	124	V _{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V _{SS}	80	DQ51	126	DQ28	172	V _{DDQ}
35	DQ25	81	V _{SS}	127	DQ29	173	NC
36	DQS3	82	V _{DDID}	128	V _{DDQ}	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	V _{DD}	84	DQ57	130	A3	176	V _{SS}
39	DQ26	85	V _{DD}	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	V _{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V _{SS}	88	DQ59	134	CB4	180	V _{DDQ}
43	A1	89	V _{SS}	135	CB5	181	SA0
44	CB0	90	NC	136	V _{DDQ}	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	V _{DD}	92	SCL	138	/CK0	184	V _{DDSPD}

FUNCTIONAL BLOCK DIAGRAM 512MB 1 Rank DDR-SDRAM registered DIMM



DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{DD}	2.3	2.7	V
I/O Supply Voltage	V _{DDQ}	2.3	2.7	V
I/O Reference Voltage	V _{REF}	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V
I/O Termination Voltage (system)	V _{TT}	V _{REF} - 0.04	V _{REF} + 0.04	V
Input High (Logic 1) Voltage	V _{IH(DC)}	V _{REF} + 0.15	V _{DD} + 0.3	V
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.3	V _{REF} - 0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ V _{DD} , V _{REF} pin 0V ≤ V _{IN} ≤ 1.35V (All other pins not under test = 0V)	I _I	-10	10	µA
OUTPUT LEAKAGE CURRENT (DQ _S are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ})	I _{OZ}	-10	10	µA
OUTPUT LEVELS: High Current (V _{OUT} = V _{DDQ} -0.373V, minimum V _{REF} , minimum V _{TT})	I _{OH}	-16.8	-	mA
Low Current (V _{OUT} = 0.373V, maximum V _{REF} , maximum V _{TT})	I _{OL}	16.8	-	mA

AC INPUT OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	V _{IH(AC)}	V _{REF} + 0.310	-	V
Input Low (Logic 0) Voltage	V _{IL(AC)}	-	V _{REF} - 0.310	V
I/O Reference Voltage	V _{REF(AC)}	0.49 x V _{DDQ}	0.51 x V _{DDQ}	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C ₁₀	4.0	5.0	pF
Input Capacitance: Command and Address	C ₁₁	18.0	27.0	pF
Input Capacitance: /S 0,1	C ₁₁	18.0	27.0	pF
Input Capacitance: CK, /CK	C ₁₂	10.0	14.0	pF
Input Capacitance: CKE	C ₁₃	18.0	27.0	pF

I_{DD} Specifications AND CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

Parameter & Test Condition	Symb.	max.		Unit	
		3200-3033	2700-2533		
OPERATING CURRENT *) : One device bank; Active-Precharge; t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	1395	1170	mA	
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; Burst = 2; t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle	I _{DD1}	1665	1440	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (Min); CKE = (LOW)	I _{DD2P}	45	45	mA	
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; t _{CK} = t _{CK} (Min); CKE = HIGH; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS, and DM	I _{DD2F}	495	405	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t _{CK} = t _{CK} (Min); CKE = LOW	I _{DD3P}	405	315	mA	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; t _{RC} = t _{RAS} (Max); t _{CK} = t _{CK} (Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I _{DD3N}	540	450	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (Min); I _{OUT} = 0mA	I _{DD4R}	1710	1485	mA	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} = t _{CK} (Min); DQ, DM, and DQS inputs changing twice per clock cycle	I _{DD4W}	1755	1575	mA	
AUTO REFRESH CURRENT	t _{RC} = t _{RC} (Min)	I _{DD5}	3105	2610	mA
	t _{RC} = 7.8125μs	I _{DD6}	99	90	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V	I _{DD7}	45	45	mA	
OPERATING CURRENT*): Four device bank interleaving READs (BL = 4) with auto precharge, t _{RC} = t _{RC} (Min); t _{CK} = t _{CK} (Min); Address and control inputs change only during Active READ, or WRITE commands	I _{DD8}	4050	3645	mA	

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (0°C ≤ T_A ≤ +70°C ; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

AC CHARACTERISTICS		3200-3033		2700-2533		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
Access window of DQ _S CK/CK#	t _{AC}	-0.70	+0.70	-0.70	+0.70	ns
CK high-level width	t _{CH}	0.45	0.55	0.45	0.55	t _{CK}
CK low-level width	t _{CL}	0.45	0.55	0.45	0.55	t _{CK}
Clock cycle time	CL=2.0	t _{ck (2.0)}	7.5	13.0	7.5	13.0
	CL=2.5	t _{ck (2.5)}	6.0	13.0	6.0	13.0
	CL=3.0	t _{ck (3.0)}	5.0	13.0		ns
DQ and DM input hold time relative to DQS	t _{DH}	0.40		0.45		ns
DQ and DM input setup time relative to DQS	t _{DS}	0.40		0.45		ns
DQ and DM input pulse width (for each input)	t _{DIPW}	1.75		1.75		ns
Access window of DQS from CK/CK#	t _{DQSCK}	-0.6	+0.6	-0.6	+0.6	ns
DQS input high pulse width	t _{DQSH}	0.35		0.35		t _{CK}
DQS input low pulse width	t _{DQSL}	0.35		0.35		t _{CK}
DQS -DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}		0.40		0.45	ns
Write command to first DQS latching transition	t _{DQSS}	0.72	1.28	0.75	1.25	t _{CK}
DQS falling edge to CK rising- setup time	t _{DSS}	0.2		0.2		t _{CK}
DQS falling edge from CK rising- hold time	t _{DSH}	0.2		0.2		t _{CK}
Half clock period	t _{HP}	t _{ch} , t _{cl}		t _{ch} , t _{cl}		ns
Data-out high-impedance window from CK/CK#	t _{HZ}		+0.7		+0.7	ns
Data-out low-impedance window from CK/CK#	t _{LZ}	-0.7		-0.7		ns
Address and control input hold time (fast slew rate)	t _{IHF}	0.6		0.75		ns
Address and control input setup time (fast slew rate)	t _{ISF}	0.6		0.75		ns
Address and control input hold time (slow slew rate)	t _{IHS}	0.6		0.8		ns
Address and control input setup time (slow slew rate)	t _{ISS}	0.6		0.8		ns
LOAD MODE REGISTER command cycle time	t _{MRD}	10		12		ns
Adress and control input pulse width (for each input)	t _{IPW}	2.2		2.2		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ns
Data hold skew factor	t _{QHS}		0.5		0.6	ns

AC CHARACTERISTICS		3200-3033		2700-2533		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
ACTIVE to PRECHARGE command	t_{RAS}	40	70.000	42	70.000	ns
ACTIVE to READ with Auto precharge command	t_{RAP}	15		15		ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55		60		ns
AUTO REFRESH command period	t_{RFC}	70		72		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		15		ns
PRECHARGE command period	t_{RP}	15		15		ns
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	t_{RRD}	10		12		ns
DQS write preamble	t_{WPRE}	0.25		0.25		t_{CK}
DQS write preamble setup time	t_{WPRES}	0		0		ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time	t_{WR}	15		15		ns
Internal WRITE to READ command delay	t_{WTR}	2		1		t_{CK}
Data valid output window	na	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns
REFRESH to REFRESH command interval	t_{REFC}		70.3		70.3	μs
Average periodic refresh interval	t_{REFI}		7.8		7.8	μs
Terminating voltage delay to V_{DD}	t_{VTD}	0		0		ns
Exit SELF REFRESH to non-READ command	t_{XSNR}	70		75		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		t_{CK}

Note 1: Values for AC timing, IDD, and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

Register Timing Requirements and Switching Characteristics

Register	Symbol	Parameter	Condition	0°C ≤ TA ≤ +70°C VDD = +2.5V ±0.2V		Units	Notes
				Min	Max		
SSTL (bit pattern by JESD82-3 or JESD82-4)	f _{clock}	Clock Frequency		-	200	MHz	
	t _{pd}	Clock to Output Time	30pF to GND and 50 Ohms to VTT	1,1	2,8	ns	
	t _{PHL}	Reset To Output Time		-	5	ns	
	t _w	Pulse Duration	CK, CK# HIGH or LOW	2,5	-	ns	
	t _{act}	Differential Inputs Active Time		-	22	ns	2
	t _{inact}	Differential Inputs Inactive Time		-	22	ns	3
	t _{su}	Setup Time, Fast Slew Rate	Data Before CK HIGH, CK# LOW	0,75	-	ns	4,6
		Setup Time, Slow Slew Rate		0,9	-	ns	5,6
	t _h	Hold Time, Fast Slew Rate	Data After CK HIGH, CK# LOW	0,75	-	ns	4,6
		Hold Time, Slow Slew Rate		0,9	-	ns	5,6

NOTE:

1. The timing and switching specifications for the register listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82-4.
2. Data inputs must be low a minimum time of t_{act} max, after RESET# is taken HIGH.
3. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max, after RESET# is taken LOW.
4. For data signal input slew rate ≥ 1 V/ns.
5. For data signal input slew rate ≥ 0.5 V/ns and < 1V/ns.
6. CK, CK# signals input slew rate ≥ 1V/ns.30

PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	0°C ≤ TA ≤ +70°C VDD = +2.5V ±0.2V			Units	Notes
		Min	Nominal	Max		
Operating Clock Frequency	f _{ck}	60	-	170	MHz	2,3
Input Duty Cycle	t _{DC}	40	-	60	%	
Stabilization Time	t _{STAB}	-	-	100	ms	4
Cycle to Cycle Jitter	t _{JITTCC}	-75	-	75	ps	
Static Phase Offset	t _∅	-50	0	50	ps	5
Output Clock Skew	t _{SKo}	-	-	100	ps	
Period Jitter	t _{JITTPER}	-75	-	75	ps	6
Half-Period Jitter	t _{JITTHPER}	-100	-	100	ps	6
Input Clock Slew Rate	t _{LSi}	1,0	-	4	V/ns	
Output Clock Slew Rate	t _{LSo}	1,0	-	2	V/ns	

NOTE:

1. The timing and switching specifications for the PLL listed above are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. The PLL must be able to handle spread spectrum induced skew.
3. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
5. Static Phase Offset does not include Jitter.
6. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

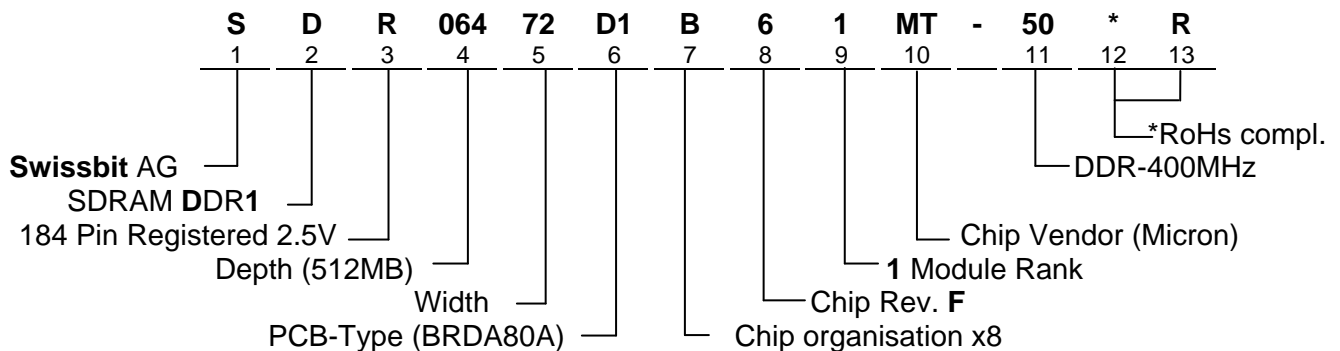
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	3200-3033	2700-2533
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x07	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0d	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0b	
5	NUMBER OF PHYSICAL BANKS ON DIMM	0x01	
6	MODULE DATA WIDTH	0x48	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V _{DDQ})	0x04	
9	SDRAM CYCLE TIME, (t _{CK}) (CAS LATENCY =2.5 (2700, 2100) ; CL=3* (3200))	0x50	0x60
10	SDRAM ACCESS FROM CLOCK, (t _{AC}) (CAS LATENCY =2.5 (2700, 2100); CL=3* (3200))	0x70	0x70
11	MODULE CONFIGURATION TYPE	0x02	
12	REFRESH RATE/ TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x08	
15	MINIMUM CLOCK DELAY, BACK- TO- BACK RANDOM COLUMN ACCESS	0x01	
16	BURST LENGTHS SUPPORTED	0x0e	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x04	
18	CAS LATENCIES SUPPORTED	0x1c	0x0c
19	CS LATENCY	0x01	
20	WE LATENCY	0x02	
21	SDRAM MODULE ATTRIBUTES	0x26	
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0xc0	
23	SDRAM CYCLE TIME, (t _{CK}) (CAS LATENCY=2(2700, 2100) CL=2,5*(3200))	0x60	0x75
24	SDRAM ACCESS FROM CK, (t _{AC}) (CAS LATENCY=2(2700, 2100) CL=2.5*(3200))	0x70	0x70
25	SDRAM CYCLE TIME, (t _{CK}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x75	0x00
26	SDRAM ACCESS FROM CK, (t _{AC}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x75	0x00
27	MINIMUM ROW PRECHARGE TIME, (t _{RP})	0x3c	0x48
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t _{RRD})	0x28	0x30
29	MINIMUM RAS# TO CAS# DELAY, (t _{RCD})	0x3c	0x48
30	MINIMUM RAS# PULSE WIDTH, (t _{RAS})	0x28	0x2a
31	MODULE BANK DENSITY	0x80	

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	3200-3033	2700-2533
32	ADDRESS AND COMMAND SETUP TIME, (t _{IS})	0x60	0x80
33	ADDRESS AND COOMAND HOLD TIME, (t _{IH})	0x60	0x80
34	DATA/DATA MASK INPUT SETUP TIME, (t _{DS})	0x40	0x45
35	DATA/DATA MASK INPUT HOLD TIME, (t _{DH})	0x40	0x45
36-40	RESERVED	0x00	
41	MIN ACTIVE AUTO REFRESH TIME (t _{RC})	0x37	0x3c
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (t _{RFC})	0x46	0x48
43	SDRAM DEVICE MAX CYCLE TIME (t _{CKMAX})	0x30	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME (t _{DQSQ})	0x28	0x2d
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR (t _{QHS})	0x50	0x60
46-61	RESERVED	0x00	
62	SPD REVISION	0x10	
63	CHECKSUM FOR BYTES 0-62	0xd7	0x8a
64	MANUFACTURER'S JEDEC ID CODE	7F	
65	MANUFACTURER'S JEDEC ID CODE	7F	
66	MANUFACTURER'S JEDEC ID CODE	7F	
67	MANUFACTURER'S JEDEC ID CODE (continued)	DA	
72	MANUFACTURING LOCATION	x	
73-90	MODULE PART NUMBER (ASCII)	"SDR06472D1B61MT-xx"	
91	PCB IDENTIFICATION CODE	x	
92	IDENTIFICATION CODE (continued)	x	
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	xx	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)		

Part Number Code



* optional / additional information

Locations

Swissbit AG

Industriestrasse 4 – 8
CH – 9552 Bronschhofen
Switzerland
Phone: +41 (0)71 913 72 66
Fax: +41 (0)71 913 74 50

Swissbit Germany GmbH

Wolfener Strasse 36
D – 12681 Berlin
Germany
Phone: +49 (0)30 93 69 54 – 0
Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.

18 Willett Avenue, Suite 203
Port Chester, NY 10573
USA
Phone: +1 914 935 1400
Fax: +1 914 935 9865

Swissbit NA, Inc.

7801 North Lamar Boulevard, Suite E – 186
Austin, TX 78752
USA
Phone: +1 512 302 9001
Fax: +1 512 302 4808