512MB DDR SDRAM SoDIMM Fox 3

200Pin SO-DIMM

SDN06464O3BK2MT-50R

512MB DDR PC-3200 in COB Technique

RoHS compliant

Options:

- Frequency / Latency — Marking
  - DDR 400 MHz CL3 — -50
  - DDR 333 MHz CL2.5 — -60
  - DDR 266 MHz CL2.5 — -75
- Module densities
  - 256MB with 8 dies and 1 rank
  - 512MB with 16 dies and 2 ranks
- Standard Grade (T_A) 0℃ to 70℃
  - Grade E (T_A) 0℃ to +85℃
  - Grade I (T_A) -25℃ to +85℃
  - Grade W (T_A) -40℃ to +85℃

Features:

- 200-pin 64-bit Small Outline Dual-In-Line. Double Data Rate synchronous DRAM Module for industrial applications
- DDR-SDRAM component base: MICRON MT46V32M8T36A
- V_{DD} 2.5V ±0.2V, V_{DDQ} 2.5V ±0.2V
- Programmable CAS Latency, Burst Length and Wrap Sequence
- Auto Refresh (CBR) and Self Refresh
- 8k Refresh every 64ms
- 2.5V I/O (SSTL_2 compatible)
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC PC3200 spec. and JEDEC- Standard MO 224. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

Environmental Requirements:

- Operating temperature (T_A)
  - Standard Grade 0℃ to 70℃
  - Grade E 0℃ to +85℃
  - Grade I -25℃ to +85℃
  - Grade W -40℃ to +85℃
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55℃ to 100℃
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50℃

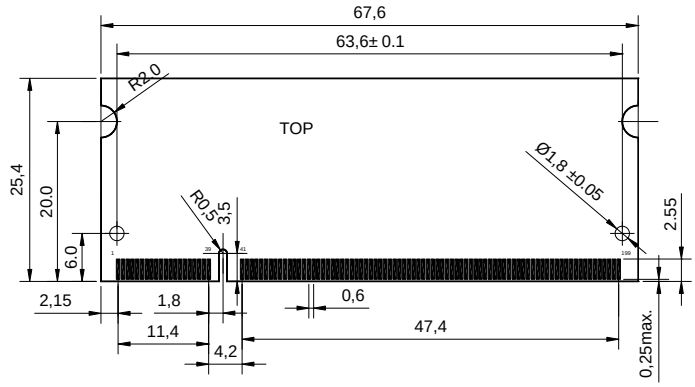


Figure: Mechanical Dimensions

This Swissbit module family is industry standard 200-pin 8-byte Double Data rate synchronous SDRAM Small Outline Dual-In-line Memory Modules (SO-DIMMs), which are organized as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs are assembled in Chip-On-Board Technology. The passive devices and the EEPROM are SMD components.
The SO-DIMMs use optional serial presence detects (SPD) implemented via serial EEPROM using the two-pin-I^2C protocol. The first 128 bytes are utilized by the SO-DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit SO-DIMMs provide a high performance, flexible 8-byte interface in a 67.6 mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

Module Configuration

Organization	DDR SDRAMs used	Row Addr.	Bank Select	Col. Addr.	Refresh	Module Dimensions in mm
64M x 64	16 x 32M x 8	13	BA0, BA1	10	8k	67.60 x 25.4 x 3.80max

Product Spectrum

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SDN06464O3BK2MT-50[E/I/W]R	512MB	3.2 GB/s	5.0ns/400MT/s	3200-3033
SDN06464O3BK2MT-60[E/I/W]R	512MB	2.7 GB/s	6.0ns/333MT/s	2700-2533
SDN06464O3BK2MT-75[E/I/W]R	512MB	2.1 GB/s	7.5ns/266MT/s	2100-2533

Pin Name

A0-9, A11 – A12	Address Inputs
A10/AP	Address Input/Autoprecharge
BA0, BA1	Bank Selects
DQ0 – DQ63	Data Input/Output
DM0-DM7	Data Masks
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Read / Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK2	Clock Inputs, positive line
/CK0 – /CK2	Clock Inputs, negative line

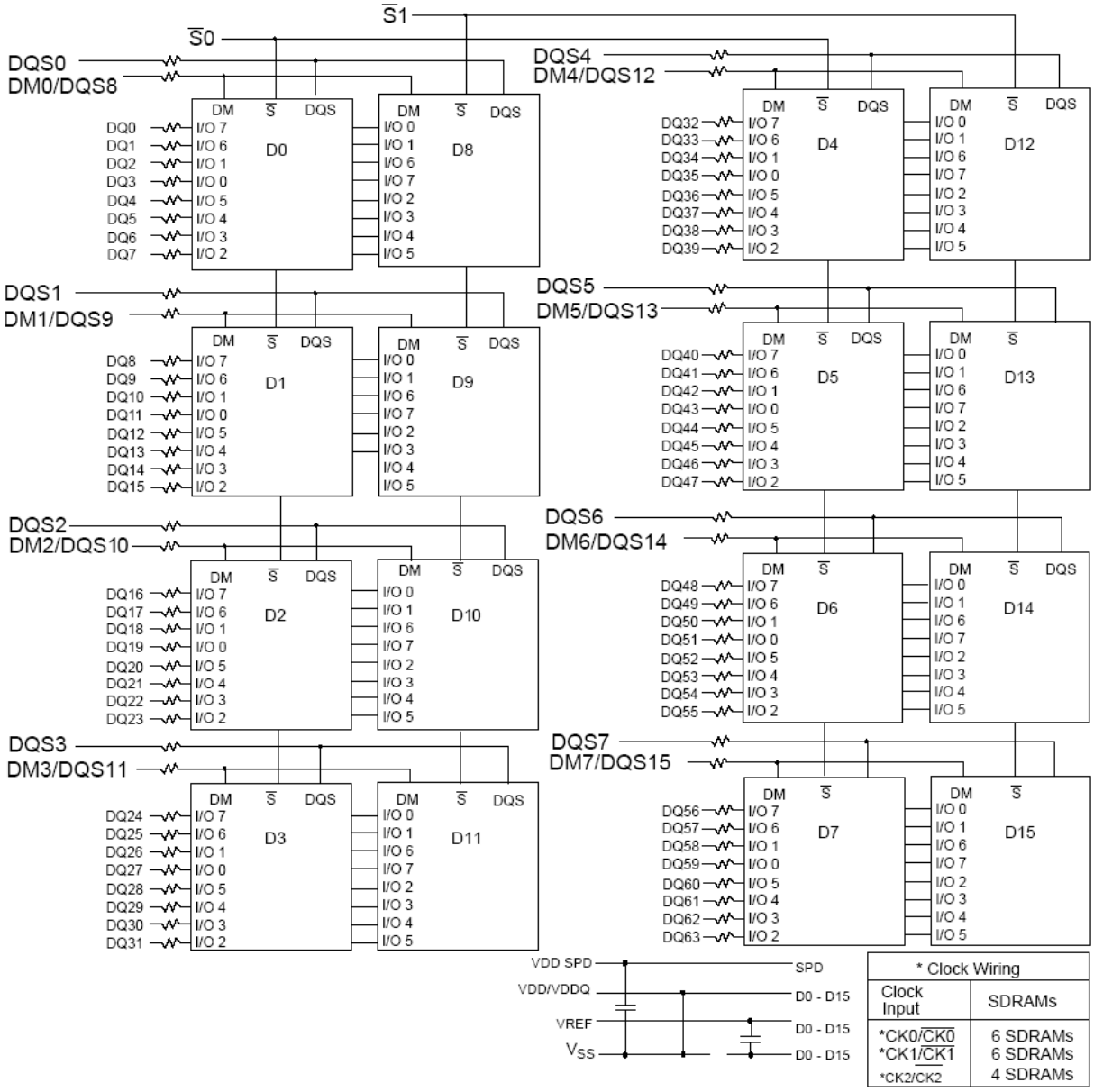
DQS0- DQS7	Data strobes
/S0, /S1	Chip Select
V_{DD}	Power (2.5V± 0.2V)
V_{DDQ}	Power (2.5V±0.2V
V_{DDID}	VDD, VDDQ level detection
V_{DDSPD}	SPD Power
V_{REF}	Input/Output Reference
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
NC	No Connection

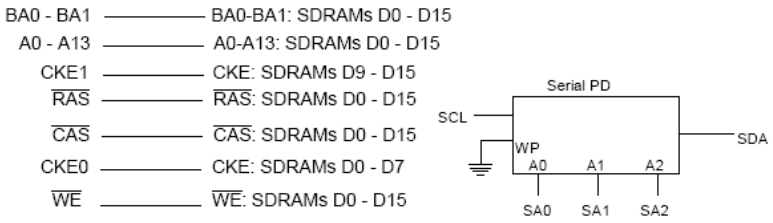
Pin Configuration

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	2	VREF	101	A9	102	A8
3	VSS	4	VSS	103	VSS	104	VSS
5	DQ0	6	DQ4	105	A7	106	A6
7	DQ1	8	DQ5	107	A5	108	A4
9	VDD	10	VDD	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	DQ2	14	DQ6	113	VDD	114	VDD
15	VSS	16	VSS	115	A10/AP	116	BA1
17	DQ3	18	DQ7	117	BA0	118	/RAS
19	DQ8	20	DQ12	119	/WE	120	/CAS
21	VDD	22	VDD	121	/S0	122	/S1
23	DQ9	24	DQ13	123	DU (A13)	124	DU
25	DQS1	26	DM1	125	VSS	126	VSS
27	VSS	28	VSS	127	DQ32	128	DQ36
29	DQ10	30	DQ14	129	DQ33	130	DQ37
31	DQ11	32	DQ15	131	VDD	132	VDD
33	VDD	34	VDD	133	DQS4	134	DM4
35	CK0	36	VDD	135	DQ34	136	DQ38
37	/CK0	38	VSS	137	VSS	138	VSS
39	VSS	40	VSS	139	DQ35	140	DQ39
41	DQ16	42	DQ20	141	DQ40	142	DQ44
43	DQ17	44	DQ21	143	VDD	144	VDD
45	VDD	46	VDD	145	DQ41	146	DQ45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	DQ18	50	DQ22	149	VSS	150	VSS
51	VSS	52	VSS	151	DQ42	152	DQ46

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
53	DQ19	54	DQ23	153	DQ43	154	DQ47
55	DQ24	56	DQ28	155	VDD	156	VDD
57	VDD	58	VDD	157	VDD	158	/CK1
59	DQ25	60	DQ29	159	VSS	160	CK1
61	DQS3	62	DM3	161	VSS	162	VSS
63	VSS	64	VSS	163	DQ48	164	DQ52
65	DQ26	66	DQ30	165	DQ49	166	DQ53
67	DQ27	68	DQ31	167	VDD	168	VDD
69	VDD	70	VDD	169	DQS6	170	DM6
71	CB0	72	CB4	171	DQ50	172	DQ54
73	CB1	74	CB5	173	VSS	174	VSS
75	VSS	76	VSS	175	DQ51	176	DQ55
77	DQS8	78	DM8	177	DQ56	178	DQ60
79	CB2	80	CB6	179	VDD	180	VDD
81	VDD	82	VDD	181	DQ57	182	DQ61
83	CB3	84	CB7	183	DQS7	184	DM7
85	DU	86	DU/(RESET)	185	VSS	186	VSS
87	VSS	88	VSS	187	DQ58	188	DQ62
89	CK2	90	VSS	189	DQ59	190	DQ63
91	/CK2	92	VDD	191	VDD	192	VDD
93	VDD	94	VDD	193	SDA	194	SA0
95	CKE1	96	CKE0	195	SCL	196	SA1
97	DU	98	DU (BA2)	197	VDDSPD	198	SA2
99	A12	100	A11	199	VDDID	200	DU

FUNCTIONAL BLOCK DIAGRAMM 512 MB DDR SDRAM SO-DIMM, 2 RANKS WITH 16 COMPONENTS





DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0℃ ≤ T_A ≤ + 70℃ ; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	2.3	2.7	V
I/O Supply Voltage	$V_{DD}Q$	2.3	2.7	V
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.51x $V_{DD}Q$	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} – 0.04	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3	V_{REF} – 0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤1.35V (All other pins not under test = 0V)	I_I	-16	16	µA
OUTPUT LEAKAGE CURRENT (DQ_S are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)	I_{OZ}	-40	40	µA
OUTPUT LEVELS: High Current (V_{OUT} = $V_{DD}Q$-0.373V,minimum V_{REF}, minimum V_{TT}) Low Current (V_{OUT} =0.373V, maximum V_{REF}, maximum V_{TT})	I_{OH} I_{OL}	-16.8 16.8	- -	mA mA

AC INPUT OPERATING CONDITIONS

(0℃ ≤ T_A ≤ + 70℃ ; V_{DD} = +2.5V ± 0.2V, V_{DDQ} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.310	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.310	V
I/O Reference Voltage	$V_{REF(AC)}$	0.49 x $V_{DD}Q$	0.51x $V_{DD}Q$	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C_{10}	4.0	5.0	pF
Input Capacitance: Command and Address	C_{11}	18.0	27.0	pF
Input Capacitance: /S 0,1	C_{11}	18.0	27.0	pF
Input Capacitance: CK, /CK	C_{12}	10.0	14.0	pF
Input Capacitance: CKE	C_{13}	18.0	27.0	pF

I_{DD} Specifications AND CONDITIONS

(0℃ ≤ T_A ≤ + 70℃ ; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

Parameter & Test Condition		Symb.	max. 3200-3033	max. 2700-2533	max. 2100-2533	Unit
OPERATING CURRENT : One device bank; Active-Precharge; t_{RC}= t_{RC} (Min); t_{CK} = t_{CK} (Min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DDO}	832	752	672	mA
OPERATING CURRENT : One device bank; Active-Read-Precharge; Burst = 2; t_{RC}= t_{RC} (Min); t_{CK} = t_{CK} (Min);I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	992	952	912	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (Min); CKE = (LOW)		I_{DD2P}	64	64	64	mA
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; t_{CK} = t_{CK} (Min); CKE= HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}	800	800	720	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t_{CK} = t_{CK} (Min);CKE = LOW		I_{DD3P}	560	480	400	mA
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; t_{RC}= t_{RAS} (Max); t_{CK} = t_{CK} (Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	960	880	800	mA
OPERATING CURRENT: Burst = 2; Reads; Continous burst; One bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (Min); I_{OUT} = 0mA		I_{DD4R}	1472	1312	1192	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (Min); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1472	1312	1192	mA
AUTO REFRESH CURRENT	t_{RC} = t_{RC} (Min)	I_{DD5}	2560	2560	2480	mA
	t_{RC} = 7.8125µs	I_{DD6}	96	96	96	mA
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}	64	64	64	mA
OPERATING CURRENT: Four device bank interleaving READs (BL =4) with auto precharge, t_{RC} = t_{RC} (Min); t_{CK} = t_{CK} (Min); Address and control inputs change only during Active READ, or WRITE commands		I_{DD8}	2352	2192	2112	mA

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0℃ ≤ T_A ≤ + 70℃ ; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

AC CHARACTERISTICS			3200-3033		2700-2533		2100-2533		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	Unit
Access window of DQ_S CK/CK#		t_{AC}	-0.70	+0.70	-0.70	+0.70	-0.75	+0.75	ns
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
Clock cycle time	CL = 2.0	t_{CK} (2.0)	7.5	13.0	7.5	13.0	10.0	13.0	ns
	CL = 2.5	t_{CK} (2.5)	6.0	13.0	6.0	13.0	7.5	13.0	ns
	CL = 3.0	t_{CK} (3.0)	5.0	7.5					ns
DQ and DM input hold time relative to DQS		t_{DH}	0.40		0.45		0.5		ns
DQ and DM input setup time relative to DQS		t_{DS}	0.40		0.45		0.5		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		1.75		ns
Access window of DQS from CK/CK#		t_{DQSCK}	-0.6	+0,6	-0.6	+0,6	-0.75	+0.75	ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		t_{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.40		0.45		0.5	ns
Write command to first DQS latching transition		t_{DQSS}	0.72	1.28	0.75	1.25	0.75	1.25	t_{CK}
DQS falling edge to CK rising-setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}
DQS falling edge from CK rising-hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}
Half clock period		t_{HP}	t_{CH}, t_{CL}		t_{CH}, t_{CL}		t_{CH}, t_{CL}		ns
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.7		+0.7		+0.75	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.7		-0.7		-0.75		ns
Address and control input hold time (fast slew rate)		t_{IHF}	0.6		0.75		0.90		ns
Address and control input setup time (fast slew rate)		t_{ISF}	0.6		0.75		0.90		ns
Address and control input hold time (slow slew rate)		t_{IHS}	0.6		0.8		1		ns
Address and control input setup time (slow slew rate)		t_{ISS}	0.6		0.8		1		ns
Address and control input pulse width (for each input)		t_{IPW}	2.2		2.2		2.2		ns
LOAD MODE REGISTER command cycle time		t_{MRD}	10		12		15		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns
Data hold skew factor		t_{QHS}		0.5		0.55		0.75	ns

AC CHARACTERISTICS		3200-3033		2700-2533		2100-2533		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**Unit**
ACTIVE to PRECHARGE command	t_{RAS}	40	70.000	42	70.000	40	120.000	ns
ACTIVE to READ with Auto precharge command	t_{RAP}	15		15		20		ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55		60		65		ns
AUTO REFRESH command period	t_{RFC}	70		72		75		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		15		20		ns
PRECHARGE command period	t_{RP}	15		18		20		ns
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	10		12		15		ns
DQS write preamble	t_{WPRE}	0.25		0.25		0.25		t_{CK}
DQS write preamble setup time	t_{WPRES}	0		0		0		ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time	t_{WR}	15		15		15		ns
Internal WRITE to READ command delay	t_{WTR}	2		1		1		t_{CK}
Data valid output window	na	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
REFRESH to REFRESH command interval	t_{REFC}		70.3		70.3		70.3	µs
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8	µs
Terminating voltage delay to V_{DD}	t_{VTD}	0		0		0		ns
Exit SELF REFRESH to non-READ command	t_{XSNR}	70		75		75		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		t_{CK}

Note 1: Values for AC timing, IDD, and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

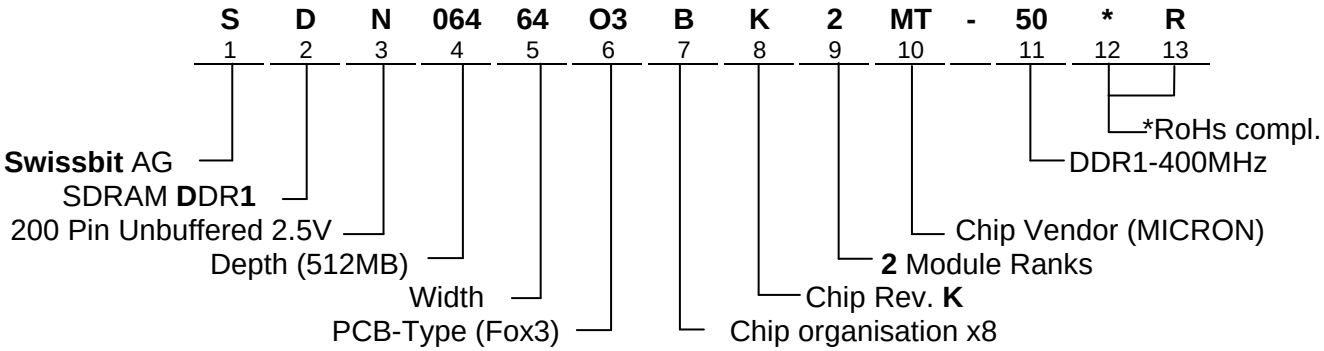
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	3200-3033	2700-2533	2100-2533
0	NUMBER OF SPD BYTES USED	0x80		
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08		
2	FUNDAMENTAL MEMORY TYPE	0x07		
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0d		
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0a		
5	NUMBER OF PHYSICAL BANKS ON DIMM	0x02		
6	MODULE DATA WIDTH	0x40		
7	MODULE DATA WIDTH (cotinued)	0x00		
8	MODULE VOLTAGE INTERFACE LEVELS ($V_{DD}Q$)	0x04		
9	SDRAM CYCLE TIME, (t_{CK}) CAS LATENCY =2.5 (2700, 2100) CL=3.0* (3200)	0x50*	0x60	0x75
10	SDRAM ACCESS FROM CLOCK,(t_{AC}) CAS LATENCY =2.5 (2700, 2100) CL=3* (3200)	0x70*	0x70	0x75
11	MODULE CONFIGURATION TYPE	0x00		
12	REFRESH RATE/ TYPE	0x82		
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08		
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00		
15	MINIMUM CLOCK DELAY, BACK- TO- BACK RANDOM COLUMN ACCESS	0x01		
16	BURST LENGTHS SUPPORTED	0x0e		
17	NUMBER OF BANKS ON SDRAM DEVICE	0x04		
18	CAS LATENCIES SUPPORTED	0x1c	0x0c	0x0c
19	CS LATENCY	0x01		
20	WE LATENCY	0x02		
21	SDRAM MODULE ATTRIBUTES	0x20		
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0xc0		
23	SDRAM CYCLE TIME, (t_{CK}) CAS LATENCY=2 (2700, 2100) CL=2,5* (3200)	0x60*	0x75	0xa0
24	SDRAM ACCESS FROM CK, (t_{AC}) CAS LATENCY=2 (2700, 2100) CL=2,5* (3200)	0x70*	0x70	0x75
25	SDRAM CYCLE TIME, (t_{CK}) CAS LATENCY=1.5 (2700, 2100) CL=2* (3200)	0x75*	0x00	0x00
26	SDRAM ACCESS FROM CK, (t_{AC}) CAS LATENCY=1.5 (2700, 2100) CL=2* (3200)	0x75*	0x00	0x00
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3c	0x48	0x50
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x28	0x30	0x3c
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3c	0x48	0x50
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x28	0x2a	0x2d
31	MODULE BANK DENSITY	0x40		

SERIAL PRESENCE-DTECT MATRIX (continued)

BYTE	DESCRIPTION	3200-3033	2700-2533	2100-2533
32	ADDRESS AND COMMAND SETUP TIME, (t_{IS})	0x60	0x80	0xa0
33	ADDRESS AND COOMAND HOLD TIME, (t_{IH})	0x60	0x80	0xa0
34	DATA/DATA MASK INPUT SETUP TIME, (t_{DS})	0x40	0x45	0x50
35	DATA/DATA MASK INPUT HOLD TIME, (t_{DH})	0x40	0x45	0x50
36-40	RESERVED	0x00		
41	MIN ACTIVE AUTO REFRESH TIME (t_{RC})	0x37	0x3c	0x46
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (t_{RFC})	0x46	0x48	0x46
43	SDRAM DEVICE MAX CYCLE TIME (t_{CKMAX})	0x30		
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME (t_{DQSQ})	0x28	0x2d	0x3c
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR (t_{QHS})	0x50	0x60	0xa0
46-61	RESERVED	0x00		
62	SPD REVISION	0x00		
63	CHECKSUM FOR BYTES 0-62	0x6f	0x22	0x38
64	MANUFACTURER`S JEDEC ID CODE	7F		
65	MANUFACTURER`S JEDEC ID CODE	7F		
66	MANUFACTURER`S JEDEC ID CODE	7F		
67	MANUFACTURER`S JEDEC ID CODE (continued)	DA		
72	MANUFACTURING LOCATION	0x02		
73-90	MODULE PART NUMBER (ASCII)	“SDN06464O3BK2MT-xx”		
91	PCB IDENTIFICATION CODE	0x52		
92	IDENTIFICATION CODE (continued)	0x00		
93	YEAR OF MANUFACTURE IN BCD	x		
94	WEEK OF MANUFACTURE IN BCD	x		
95-98	MODULE SERIAL NUMBER	x		
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)			

Part Number Code



* optional / additional information

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