

2048MB DDR3 – SDRAM DIMM

240 Pin UDIMM

SGU02G64B1BG2SA-xxR

2GByte in FBGA Technology

RoHS compliant

Options:

- | | |
|---------------------------------|-------------------------------|
| ▪ Data Rate / Latency | Marking |
| DDR3 1066 MT/s CL7 | -BB |
| DDR3 1333 MT/s CL9 | -CC |
| | |
| ▪ Module Density | |
| 2048MB with 16 dies and 2 ranks | |
| | |
| ▪ Standard Grade | (T _A) 0°C to 70°C |
| | (T _c) 0°C to 85°C |

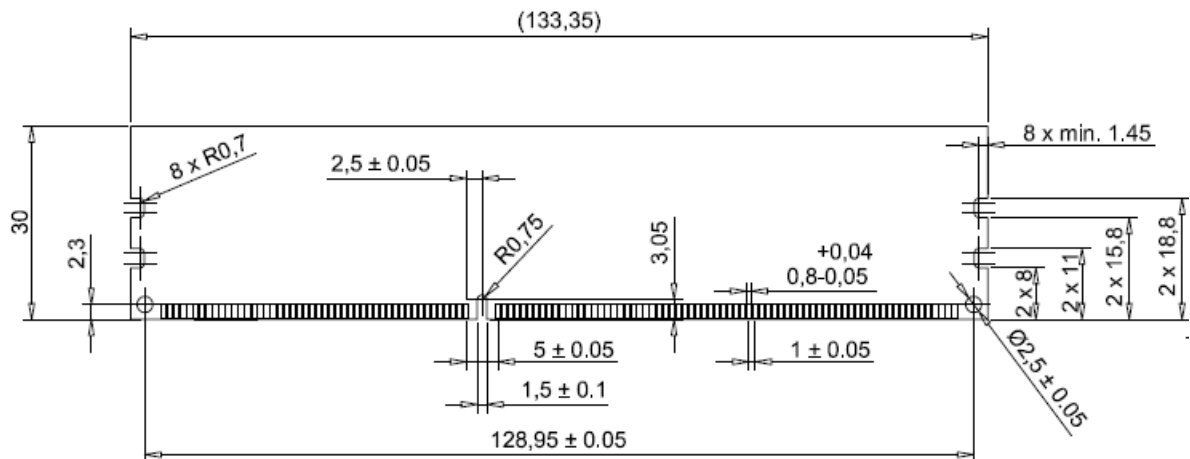
Environmental Requirements:

- Operating temperature (ambient)
Standard Grade 0°C to 70°C
- Operating Humidity
10% to 90% relative humidity, noncondensing
- Operating Pressure
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
-55°C to 100°C
- Storage Humidity
5% to 95% relative humidity, noncondensing
- Storage Pressure
1682 PSI (up to 5000 ft.) at 50°C

Features:

- 240-pin 64-bit DDR3 Dual-In-Line Double Data Rate Synchronous DRAM module for industrial applications
- Module organization: dual rank 256M x 64
- V_{DD} = 1.5V ±0.075V, V_{DDQ} 1.5V ±0.075V
- 1.5V I/O (SSTL_15 compatible)
- serial presence-detect (SPD) EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC3-10600 spec. and JEDEC- Standard MO-269. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- DDR3 - SDRAM component Samsung K4B1G0846G**
- 128Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit pre-fetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

Figure: mechanical dimensions¹



¹if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 240-pin 8-byte DDR3 SDRAM Dual-In-line Memory Module (UDIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.

The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I²C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (Swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
256M x 64bit	16 x 128M x 8bit (1024Mbit)	14	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions in mm
133.35 (long) x 30 (high) x 4.00 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SGU02G64B1BG2SA-BBR	2048 MB	8.5 GB/s	1.87ns/1066MT/s	7-7-7
SGU02G64B1BG2SA-CCR	2048 MB	10.6 GB/s	1.5ns/1333MT/s	9-9-9

Pin Name

A0-9, A11 – A13	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
DQS0 – DQS7#	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0#, S1#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
ODT0, ODT1	On-Die Termination

CK0 – CK1	Clock inputs, positive line
CK0# - CK1#	Clock inputs, negative line
V _{DD}	Supply Voltage (1.5V± 0.075V)
V _{REFDQ}	Reference voltage: DQ, DM (VDD/2)
V _{REFCA}	Reference voltage: Control, command, and address (VDD/2)
V _{SS}	Ground
V _{TT}	Termination voltage: Used for control, command, and address (VDD/2).
V _{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA2	Presence Detect Address Inputs
Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
NC	No Connection

Pin Configuration

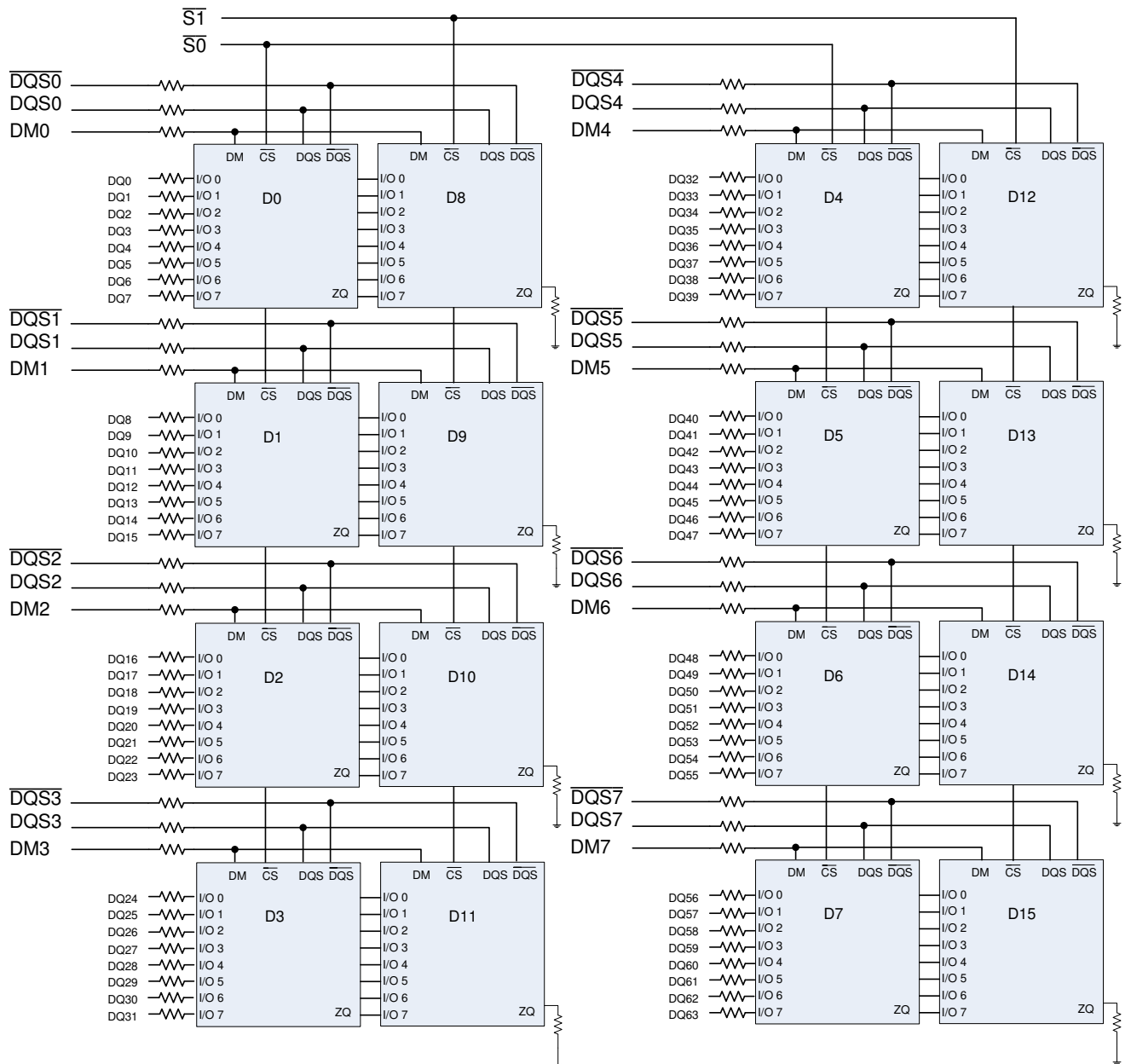
Frontside									
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	V _{REFDQ}	27	DQ18	49	NC(V _{TT})	75	V _{DD}	101	V _{SS}
2	V _{SS}	28	DQ19	50	CKE0	76	S1#	102	DQS6#
3	DQ0	29	V _{SS}	51	V _{DD}	77	ODT1	103	DQS6
4	DQ1	30	DQ24	52	BA2	78	V _{DD}	104	V _{SS}
5	V _{SS}	31	DQ25	53	NC(Err_Out#)	79	NC(S2#)	105	DQ50
6	DQS0#	32	V _{SS}	54	V _{DD}	80	V _{SS}	106	DQ51
7	DQS0	33	DQS3#	55	A11	81	DQ32	107	V _{SS}
8	V _{SS}	34	DQS3	56	A7	82	DQ33	108	DQ56
9	DQ2	35	V _{SS}	57	V _{DD}	83	V _{SS}	109	DQ57
10	DQ3	36	DQ26	58	A5	84	DQS4#	110	V _{SS}
11	V _{SS}	37	DQ27	59	A4	85	DQS4	111	DQS7#
12	DQ8	38	V _{SS}	60	V _{DD}	86	V _{SS}	112	DQS7
13	DQ9	39	NC(CB0)	61	A2	87	DQ34	113	V _{SS}
14	V _{SS}	40	NC(CB1)	62	V _{DD}	88	DQ35	114	DQ58
15	DQS1#	41	V _{SS}	63	CK1	89	V _{SS}	115	DQ59
16	DQS1	42	NC(DQS8#)	64	CK1#	90	DQ40	116	V _{SS}
17	V _{SS}	43	NC(DQS8)	65	V _{DD}	91	DQ41	117	SA0
18	DQ10	44	V _{SS}	66	V _{DD}	92	V _{SS}	118	SCL
19	DQ11	45	NC(CB2)	67	V _{REFCA}	93	DQS5#	119	SA2
20	V _{SS}	46	NC(CB3)	68	NC(Par_In)	94	DQS5	120	V _{TT}
21	DQ16	47	V _{SS}	69	V _{DD}	95	V _{SS}		
22	DQ17	48	NC(V _{TT})	70	A10/ AP	96	DQ42		
23	V _{SS}			71	BA0	97	DQ43		
24	DQS2#			72	V _{DD}	98	V _{SS}		
25	DQS2			73	WE#	99	DQ48		
26	V _{SS}			74	CAS#	100	DQ49		

Signals in brackets (...) may be connected at the DIMM socket, but are not used on the DIMM

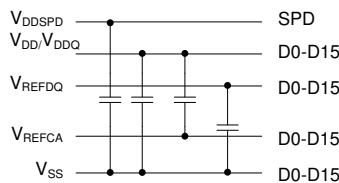
Backside									
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
121	V _{SS}	147	DQ23	169	CKE1	195	ODT0	221	DM6(DQS15)
122	DQ4	148	V _{SS}	170	V _{DD}	196	A13	222	NC(DQS15#)
123	DQ5	149	DQ28	171	NC(A15)	197	V _{DD}	223	V _{SS}
124	V _{SS}	150	DQ29	172	NC(A14)	198	NC(S3#)	224	DQ54
125	DM0(DQS9)	151	V _{SS}	173	V _{DD}	199	V _{SS}	225	DQ55
126	NC(DQS9#)	152	DM3(DQS12)	174	A12, BC#	200	DQ36	226	V _{SS}
127	V _{SS}	153	NC(DQS12#)	175	A9	201	DQ37	227	DQ60
128	DQ6	154	V _{SS}	176	V _{DD}	202	V _{SS}	228	DQ61
129	DQ7	155	DQ30	177	A8	203	DM4(DQS13)	229	V _{SS}
130	V _{SS}	156	DQ31	178	A6	204	NC(DQS13#)	230	DM7(DQS16)
131	DQ12	157	V _{SS}	179	V _{DD}	205	V _{SS}	231	NC(DQS16#)
132	DQ13	158	NC(CB4)	180	A3	206	DQ38	232	V _{SS}
133	V _{SS}	159	NC(CB5)	181	A1	207	DQ39	233	DQ62
134	DM1(DQS10)	160	V _{SS}	182	V _{DD}	208	V _{SS}	234	DQ63
135	NC(DQS10#)	161	DM8(DQS17)	183	V _{DD}	209	DQ44	235	V _{SS}
136	V _{SS}	162	NC(DQS17#)	184	CK0	210	DQ45	236	V _{DDSPD}
137	DQ14	163	V _{SS}	185	CK0#	211	V _{SS}	237	SA1
138	DQ15	164	NC(CB6)	186	V _{DD}	212	DM5(DQS14)	238	SDA
139	V _{SS}	165	NC(CB7)	187	NC(EVENT#)	213	NC(DQS14#)	239	V _{SS}
140	DQ20	166	V _{SS}	188	A0	214	V _{SS}	240	V _{TT}
141	DQ21	167	NC(TEST)	189	V _{DD}	215	DQ46		
142	V _{SS}	168	RESET#	190	BA1	216	DQ47		
143	DM2(DQS11)			191	V _{DD}	217	V _{SS}		
144	NC(DQS11#)			192	RAS#	218	DQ52		
145	V _{SS}			193	S0#	219	DQ53		
146	DQ22			194	V _{DD}	220	V _{SS}		

Signals in brackets (...) may be connected at the DIMM socket, but are not used on the DIMM

**FUNCTIONAL BLOCK DIAGRAM 2048MB DDR3 SDRAM DIMM,
2 RANKS AND 16 COMPONENTS**



BA0-BA2 → BA0-BA2: SDRAM D0-D15
 A0-A13 → A0-A13: SDRAM D0-D15
 RAS → RAS: SDRAM D0-D15
 CAS → CAS: SDRAM D0-D15
 WE → WE: SDRAM D0-D15
 ODT0 → ODT: SDRAM D0-D7
 ODT1 → ODT: SDRAM D8-D15
 CEK0 → CEK: SDRAM D0-D7
 CEK1 → CEK: SDRAM D8-D15
 CK0,CK1 → CK: SDRAM D0-D15
 CK0,CK1 → CK: SDRAM D0-D15
 RESET → RESET: SDRAM D0-D15



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationship must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDEC document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-0.4	1.975	V
I/O Supply Voltage	V_{DDQ}	-0.4	1.975	V
V_{DDL} Supply Voltage	V_{DDL}	-0.4	1.975	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	I_I			μA
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	I_{OZ}	-5	5	μA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-8	8	μA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V
V_{DDL} Supply Voltage	V_{DDL}	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	V_{TT}	$0.49 \times V_{DDQ} - 20mV$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ} + 20mV$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.1$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.1$	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.175$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.175$	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85 °C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

Parameter & Test Condition	Symbol	max.		Unit
		10600-999	8500-777	
OPERATING CURRENT *) : One device bank Active-Precharge; $t_{RC} = t_{RC}(I_{DD})$; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I_{DD0}	360	360	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; $I_{OUT} = 0mA$; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RC} = t_{RC}(I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN}(I_{DD})$, $t_{RCD} = t_{RCD}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}	I_{DD1}	416	400	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast Exit	I_{DD2P}	192	mA
	Slow Exit		160	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	I_{DD2Q}	240	240	mA
PRECHARGE STANDBY CURRENT: All device banks idle; $t_{CK} = t_{CK}(I_{DD})$; CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD2N}	240	240	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; $t_{CK} = t_{CK}(I_{DD})$; CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF} (always fast exit)	I_{DD3P}	240	240	mA
ACTIVE STANDBY CURRENT: All device banks open; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX}(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD3N}	320	320	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; $I_{OUT} = 0mA$; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}(I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX}(I_{DD})$, $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4R}	640	560	mA

Parameter & Test Condition	Symbol	max.		Unit
		10600-999	8500-777	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4W}	640	560	mA
BURST REFRESH CURRENT: t _{CK} = t _{CK} (I _{DD}); refresh command at every t _{RFC} (I _{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD5}	1440	1360	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V _{REF} ; DQ's are floating at V _{REF}	I _{DD6}	160	160	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = t _{RCD} (I _{DD}) - 1 x t _{CK} (I _{DD}); t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RRD} = t _{RRD} (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I _{DD7}	1120	920	mA

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I _{DD} MEASUREMENT CONDITIONS			
SYMBOL	10600-999	8500-777	Unit
CL (I _{DD})	9	7	t _{CK}
t _{RCD} (I _{DD})	13.5	13.125	ns
t _{RC} (I _{DD})	49.5	50.625	ns
t _{RRD} (I _{DD})	6	7.5	ns
t _{CK} (I _{DD})	1.5	1.87	ns
t _{RAS} MIN (I _{DD})	36	37.5	ns
t _{RAS} MAX (I _{DD})	70'200	70'200	ns
t _{RP} (I _{DD})	13.5	13.125	ns
t _{RFC} (I _{DD})	110	110	ns

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.5\text{V} \pm 0.075\text{V}, V_{\text{DD}} = +1.5\text{V} \pm 0.075\text{V})$

AC CHARACTERISTICS			10600-999		8500-777		Unit
PARAMETER		SYMBOL	MIN	MAX	MAX	MAX	
Clock cycle time	CL = 10	$t_{\text{CK}}(10)$	1.5	<1.875	-	-	ns
	CL = 9	$t_{\text{CK}}(9)$	1.5	<1.875	-	-	ns
	CL = 8	$t_{\text{CK}}(8)$	1.875	<2.5	-	-	ns
	CL = 7	$t_{\text{CK}}(7)$	1.875	<2.5	1.875	<2.5	ns
	CL = 6	$t_{\text{CK}}(6)$	2.5	3.3	2.5	3.3	ns
	CL = 5	$t_{\text{CK}}(5)$					ns
CK high-level width		t_{CH}	0.47	0.53	0.47	0.53	t_{CK}
CK low-level width		t_{CL}	0.47	0.53	0.47	0.53	t_{CK}
Data-out high-impedance window from CK/CK#		t_{HZ}		0.25		0.3	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.5	0.25	-0.6	0.3	ns
DQ and DM input setup time relative to DQS		$t_{\text{DS(Base)}}$	30		25		ps
DQ and DM input hold time relative to DQS		$t_{\text{DH(Base)}}$	65		100		ps
DQ and DM input setup time relative to DQS $V_{\text{REF}}=1\text{V/ns}$		t_{DS1V}	180		200		ps
DQ and DM input hold time relative to DQS $V_{\text{REF}}=1\text{V/ns}$		t_{DH1V}	165		200		ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.4		0.49		ns
DQS, DQS# to DQ skew, per access		t_{DQSQ}		125		150	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	0.38		0.38		t_{CK} (AVG)
DQS input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}
DQS input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}
DQS, DQS# rising to/from CK, CK#		t_{DQSK}	-255	+255	-300	300	ps
DQS, DQS# rising to/from CK, CK# when DLL disabled		$t_{\text{DQSK}}^{\text{DLL DIS}}$	1	10	1	10	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
DQS read preamble		t_{RPRE}	0.9	Note1	0.9	Note1	t_{CK}
DQS read postamble		t_{RPST}	0.3	Note2	0.3	Note2	t_{CK}
DQS write preamble		t_{WPRE}	0.9		0.9		t_{CK}
DQS write postamble		t_{WPST}	0.3		0.3		t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	620		780		ps
CTRL, CMD, Addr setup to CK, CK#		$t_{\text{IS(Base)}}$	65		125		ps
CTRL, CMD, Addr setup to CK, CK# $V_{\text{REF}} @ 1\text{V/ns}$		$t_{\text{IS(1V)}}$	240		300		ps

1 The maximum preamble is bound by t_{LZDQS} (MAX)

2 The maximum postamble is bound by t_{HZDQS} (MAX)

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
 $0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.5\text{V} \pm 0.075\text{V}, V_{\text{DD}} = +1.5\text{V} \pm 0.075\text{V}$

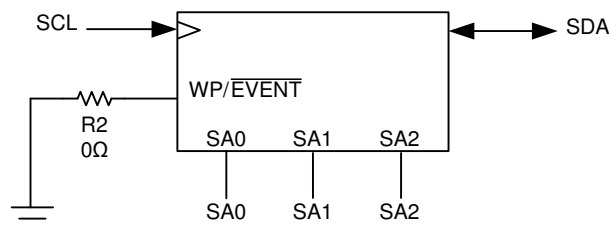
AC CHARACTERISTICS		10600-999		8500-777		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
CTRL, CMD, Addr hold to CK, CK#	$t_{\text{IH(Base)}}$	140		200		ps
CTRL, CMD, Addr hold to CK, CK# $V_{\text{REF}} @ 1\text{V/ns}$	$t_{\text{IH(1V)}}$	240		300		ps
CAS# to CAS# command delay	t_{CCD}	4		4		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	49.5		50.625		ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	6		7.5		ns
ACTIVE to READ or WRITE delay	t_{RCD}	13.5		13.125		ns
Four bank Activate period	t_{FAW}	30		37.5		ns
1K Page size 2K Page size		45		50		
ACTIVE to PRECHARGE command	t_{RAS}	36	70'200	37.5	70'200	ns
Internal READ to precharge command delay	t_{RTP}	7.5		7.5		ns
Write recovery time	t_{WR}	15		15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$		$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		ns
PRECHARGE command period	t_{RP}	13.5		13.125		ns
LOAD MODE command cycle time	t_{MRD}	4		4		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	110	70'200	110	70'200	ns
Average periodic refresh interval $0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	t_{REFI}		7.8		7.8	μs
$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	$t_{\text{REFI (IT)}}$		3.9		3.9	
RTT turn-on from ODTL on reference	t_{AON}	-250	250	-300	300	ps
RTT turn-on from ODTL off reference	t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)	t_{AONPD}	1	9	1	9	ns
Asynchronous RTT turn-off delay (power Down with DLL off)	t_{AOFPD}	1	9	1	9	ns
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
Exit self refresh to commands not requiring a locked DLL	t_{XS}	120		120		ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	t_{WLS}	195		245		ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing	t_{WLH}	195		245		ps
First DQS, DQS# rising edge	t_{WLMRD}	40		40		t_{CK}
DQS, DQS# delay	t_{WLDQSEN}	25		25		t_{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		10600-999		8500-777		Unit
PARAMETER	SYMBOL	MIN	MAX	MAX	MAX	
Exit reset from CKE HIGH to a valid command	t _{XPR}	120		120		ns
Begin power supply ramp to power supplies stable	t _{VDDPR}		200		200	ms
RESET# LOW to power supplies stable	t _{RPS}		200		200	ms
RESET# LOW to I/O and RTT High-Z	t _{IOz}		20		20	ns
Exit precharge power-down to any non-READ command	t _{XP}	6		7.5		ns
CKE minimum high/low time	t _{CKE}	5.625		5.625		t _{CK}

Serial Presence-Detect EEPROM

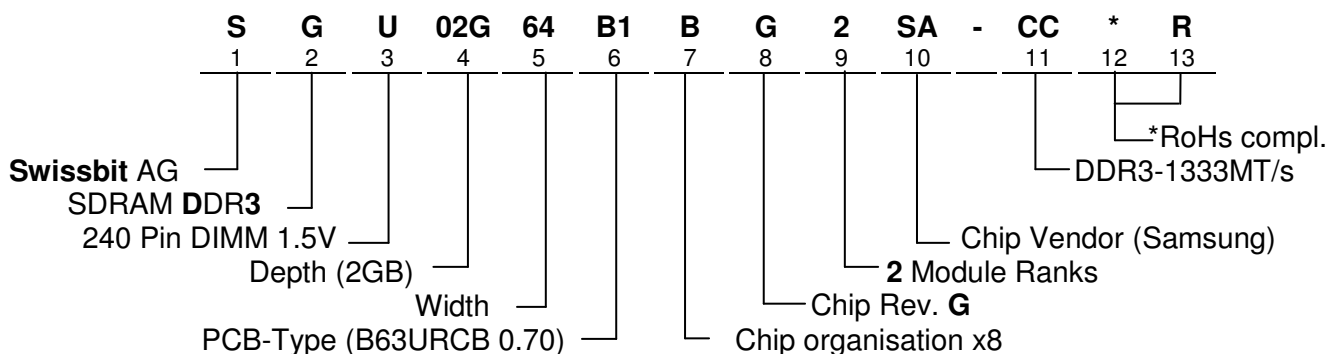


SERIAL PRESENCE-DETECT MATRIX

Byte	Byte Description	10600-999	8500-777
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISION	0x10	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x02	
4	SDRAM DEVICE DENSITY & BANKS	0x02	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x11	
6	BYTE 6 RESERVED	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x09	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x03	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x52	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ($t_{CK\ MIN}$)	0x0C	0x0F
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0x3C	0x1C
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ($t_{AA\ MIN}$)	0x69	
17	MIN WRITE RECOVERY TIME ($t_{WR\ MIN}$)	0x78	
18	MIN RAS# TO CAS# DELAY ($t_{RCD\ MIN}$)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ($t_{RRD\ MIN}$)	0x30	0x3C
20	MIN ROW PRECHARGE DELAY ($t_{RP\ MIN}$)	0x69	
21	UPPER NIBBLE FOR t_{RAS} & t_{RC}	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ($t_{RAS\ MIN}$)	0x20	0x2C
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY ($t_{RC\ MIN}$)	0x89	0x95
24	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) LSB	0x70	
25	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) MSB	0x03	
26	MIN INTERNAL WRITE TO READ CMD DELAY ($t_{WTR\ MIN}$)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ($t_{RTP\ MIN}$)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) MSB	0x00	0x01
29	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) LSB	0xF0	0x2C
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x83	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x01	

Byte	Byte Description	10600-999	8500-777
32-59	BYTES 32-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x0F	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x01	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x01	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0Xda	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0x626C	0x20C5
128-145	MODULE PART NUMBER	"SGU02G64B1BG2SA-xx"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	X	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0xCE	
150-175	MFR RESERVED BYTES 150-175	0xFF	
176-255	CUSTOMER RESERVED BYTES 176-255	0xFF	

Part Number Code



* optional / additional information

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