4096MB DDR3 – SDRAM RDIMM

240 Pin registered DIMM

SGP04G72D1BD2MT-CCRT

4096MB PC3-10600 in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  DDR3 1333 MT/s CL9 — -CC
  DDR3 1066 MT/s CL7 — -BB
- Module Density
  4096MB with 18 dies and 2 ranks
- Standard Grade (T_A) 0°C to 70°C
  (T_C) 0°C to 85°C

Environmental Requirements:

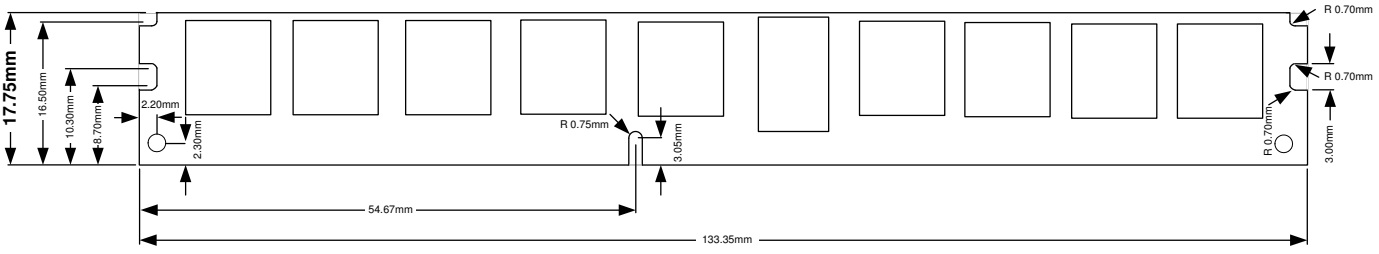
- Operating temperature (ambient)
  Standard Grade 0°C to 70°C
- Operating Humidity
  10% to 90% relative humidity, non condensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, non condensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Features:

- 240-pin 72-bit DDR3 registered Dual-In-Line Double Data Rate synchronous DRAM module for server applications
- Module organization: dual rank 512M x 72
- V_{DD} = 1.5V ±0.075V, V_{DDQ} 1.5V ±0.075V
- 1.5V I/O (SSTL_15 compatible)
- Ultra Low Profile (ULP)
- JEDEC compatible DDR3 PLL/Register component with parity bit support for address and control bus
- Supports ECC error detection and correction
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC3-10600 spec. and JEDEC- Standard MO-269. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR3 - SDRAM component Micron MT41J256M8HX-15E:D**
- 256Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit prefetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

Figure: mechanical dimensions[1]



[1]the reference according MO269

This Swissbit module is an industry standard 240-pin 8-byte DDR3 registered SDRAM Dual-In-line Memory Module (RDIMM) which is organized as x72 high speed CMOS memory array. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. De-coupling capacitors, stub resistors, calibration resistors and termination resistors are mounted on the PCB board. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.

The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (Swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
512M x 72bit	18 x 256M x 8bit (2Gbit)	15	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions in mm
133.35 (long) x 17.75 (high) x 4.00 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SGP04G72D1BD2MT-BBRT	4096 MB	8.5 GB/s	1.87ns / 1066MT/s	7-7-7
SGP04G72D1BD2MT-CCRT	4096 MB	10.6 GB/s	1.5ns / 1333MT/s	9-9-9

Pin Name

A0 – A9, A11, A13 – A15	Address Inputs (A15 not functional, but included in parity check)
A10/AP	Address Input / Auto precharge Bit
A12/BC	Address Input / Burst chop
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
CB0 – CB7	Data check bits Input / Output
DM0-DM8	Input Data Mask
DQS0 – DQS8	Data Strobe, positive line
DQS0# - DQS8#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable

CKE0 – CKE1	Clock Inputs, negative line
S0#, S1#	Chip Select
CK0 – CK1	Clock Inputs, positive line
CK0# - CK1#	Clock Inputs, negative Line
Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
V_{DD}	Supply Voltage (1.5V± 0.075V)
V_{REF}DQ	Reference voltage: DQ, DM (VDD/2)
V_{REF}CA	Reference voltage: Control, command, and address (VDD/2)
V_{SS}	Ground
V_{TT}	Termination voltage: Used for control, command, and address (VDD/2).
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Serial Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

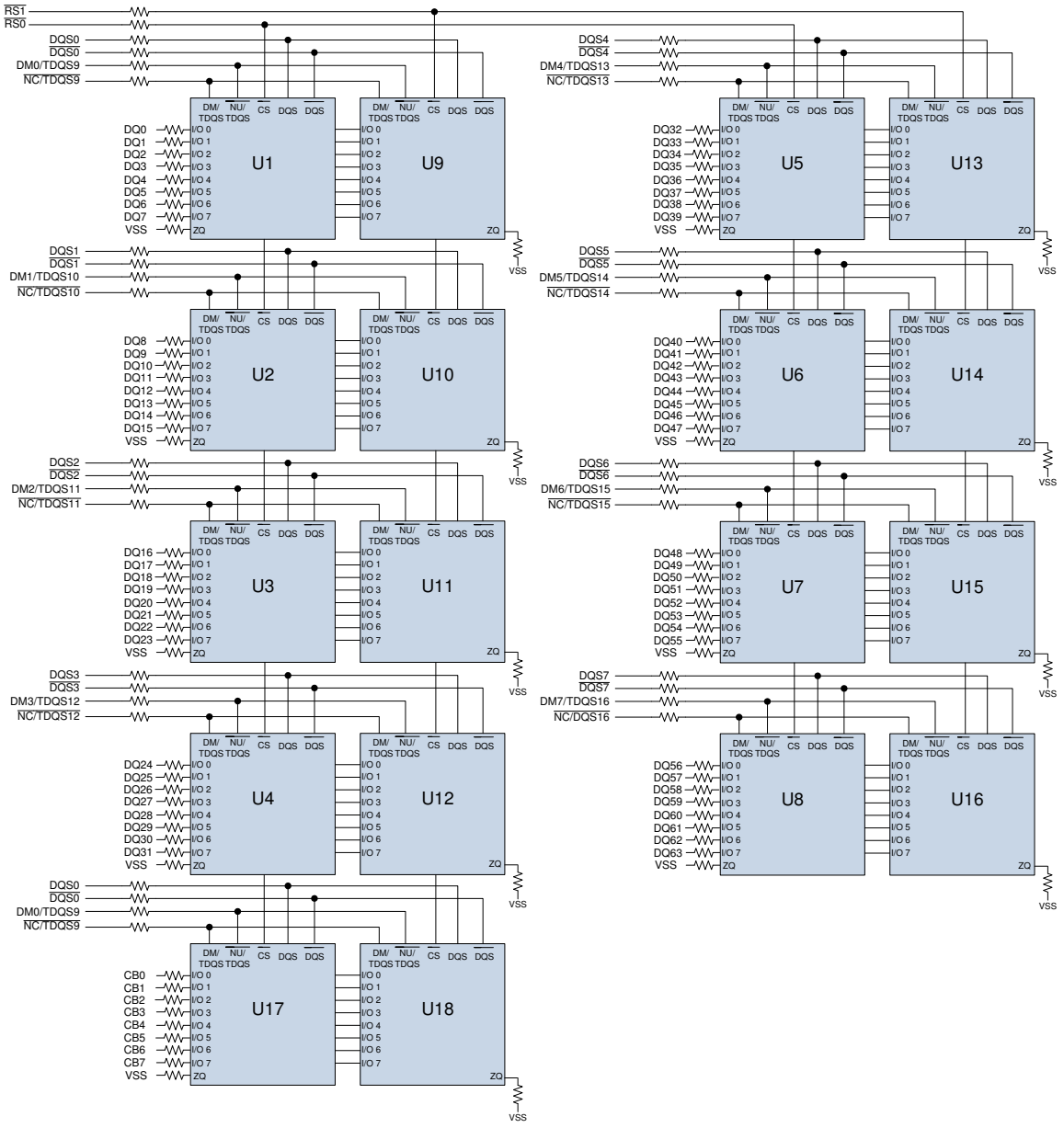
Frontside									
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
Pin 1	V_{REFDQ}	Pin 27	DQ18	Pin 49	V_{TT}	Pin 75	V_{DD}	Pin 101	V_{SS}
Pin 2	V_{SS}	Pin 28	DQ19	Pin 50	CKE0	Pin 76	S1# *	Pin 102	DQS6#
Pin 3	DQ0	Pin 29	V_{SS}	Pin 51	V_{DD}	Pin 77	NC, ODT1 *	Pin 103	DQS6
Pin 4	DQ1	Pin 30	DQ24	Pin 52	BA2	Pin 78	V_{DD}	Pin 104	V_{SS}
Pin 5	V_{SS}	Pin 31	DQ25	Pin 53	Err_Out#	Pin 79	NC, S2# *	Pin 105	DQ50
Pin 6	DQS0#	Pin 32	V_{SS}	Pin 54	V_{DD}	Pin 80	V_{SS}	Pin 106	DQ51
Pin 7	DQS0	Pin 33	DQS3#	Pin 55	A11	Pin 81	DQ32	Pin 107	V_{SS}
Pin 8	V_{SS}	Pin 34	DQS3	Pin 56	A7	Pin 82	DQ33	Pin 108	DQ56
Pin 9	DQ2	Pin 35	V_{SS}	Pin 57	V_{DD}	Pin 83	V_{SS}	Pin 109	DQ57
Pin 10	DQ3	Pin 36	DQ26	Pin 58	A5	Pin 84	DQS4#	Pin 110	V_{SS}
Pin 11	V_{SS}	Pin 37	DQ27	Pin 59	A4	Pin 85	DQS4	Pin 111	DQS7#
Pin 12	DQ8	Pin 38	V_{SS}	Pin 60	V_{DD}	Pin 86	V_{SS}	Pin 112	DQS7
Pin 13	DQ9	Pin 39	CB0	Pin 61	A2	Pin 87	DQ34	Pin 113	V_{SS}
Pin 14	V_{SS}	Pin 40	CB1	Pin 62	V_{DD}	Pin 88	DQ35	Pin 114	DQ58
Pin 15	DQS1#	Pin 41	V_{SS}	Pin 63	RFU	Pin 89	V_{SS}	Pin 115	DQ59
Pin 16	DQS1	Pin 42	DQS8#	Pin 64	RFU	Pin 90	DQ40	Pin 116	V_{SS}
Pin 17	V_{SS}	Pin 43	DQS8	Pin 65	V_{DD}	Pin 91	DQ41	Pin 117	SA0
Pin 18	DQ10	Pin 44	V_{SS}	Pin 66	V_{DD}	Pin 92	V_{SS}	Pin 118	SCL
Pin 19	DQ11	Pin 45	CB2	Pin 67	V_{REFCA}	Pin 93	DQS5#	Pin 119	SA2
Pin 20	V_{SS}	Pin 46	CB3	Pin 68	Par_In	Pin 94	DQS5	Pin 120	V_{TT}
Pin 21	DQ16	Pin 47	V_{SS}	Pin 69	V_{DD}	Pin 95	V_{SS}		
Pin 22	DQ17	Pin 48	V_{TT}	Pin 70	A10/ AP	Pin 96	DQ42		
Pin 23	V_{SS}			Pin 71	BA0	Pin 97	DQ43		
Pin 24	DQS2#			Pin 72	V_{DD}	Pin 98	V_{SS}		
Pin 25	DQS2			Pin 73	WE#	Pin 99	DQ48		
Pin 26	V_{SS}			Pin 74	CAS#	Pin 100	DQ49		

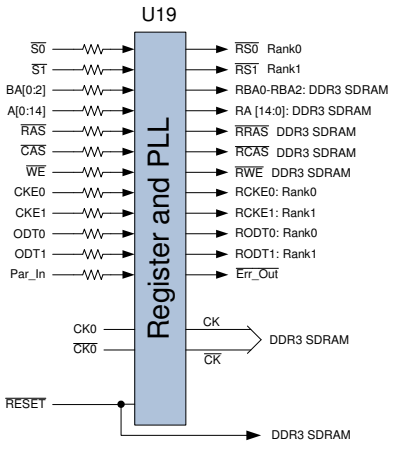
Backside									
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Pin 121	V_{SS}	Pin 147	DQ23	Pin 169	NC,CKE1 *	Pin 195	ODT0	Pin 221	(T)DQS15 *
Pin 122	DQ4	Pin 148	V_{SS}	Pin 170	V_{DD}	Pin 196	A13, NC *	Pin 222	(T)DQS15# *
Pin 123	DQ5	Pin 149	DQ28	Pin 171	NC, A15 *	Pin 197	V_{DD}	Pin 223	V_{SS}
Pin 124	V_{SS}	Pin 150	DQ29	Pin 172	A14, NC *	Pin 198	NC, S3# *	Pin 224	DQ54
Pin 125	(T)DQS9# *	Pin 151	V_{SS}	Pin 173	V_{DD}	Pin 199	V_{SS}	Pin 225	DQ55
Pin 126	(T)DQS9# *	Pin 152	(T)DQS12 *	Pin 174	A12, BC	Pin 200	DQ36	Pin 226	V_{SS}
Pin 127	V_{SS}	Pin 153	(T)DQS12# *	Pin 175	A9	Pin 201	DQ37	Pin 227	DQ60
Pin 128	DQ6	Pin 154	V_{SS}	Pin 176	V_{DD}	Pin 202	V_{SS}	Pin 228	DQ61
Pin 129	DQ7	Pin 155	DQ30	Pin 177	A8	Pin 203	(T)DQS13 *	Pin 229	V_{SS}
Pin 130	V_{SS}	Pin 156	DQ31	Pin 178	A6	Pin 204	(T)DQS13# *	Pin 230	(T)DQS16 *
Pin 131	DQ12	Pin 157	V_{SS}	Pin 179	V_{DD}	Pin 205	V_{SS}	Pin 231	(T)DQS16# *
Pin 132	DQ13	Pin 158	CB4	Pin 180	A3	Pin 206	DQ38	Pin 232	V_{SS}
Pin 133	V_{SS}	Pin 159	CB5	Pin 181	A1	Pin 207	DQ39	Pin 233	DQ62
Pin 134	(T)DQS10 *	Pin 160	V_{SS}	Pin 182	V_{DD}	Pin 208	V_{SS}	Pin 234	DQ63
Pin 135	(T)DQS10# *	Pin 161	(T)DQS17 *	Pin 183	V_{DD}	Pin 209	DQ44	Pin 235	V_{SS}
Pin 136	V_{SS}	Pin 162	(T)DQS17# *	Pin 184	CK0	Pin 210	DQ45	Pin 236	VDD_{SPD}
Pin 137	DQ14	Pin 163	V_{SS}	Pin 185	CK0#	Pin 211	V_{SS}	Pin 237	SA1
Pin 138	DQ15	Pin 164	CB6	Pin 186	V_{DD}	Pin 212	(T)DQS14 *	Pin 238	SDA
Pin 139	V_{SS}	Pin 165	CB7	Pin 187	NC	Pin 213	(T)DQS14# *	Pin 239	V_{SS}/Event# *
Pin 140	DQ20	Pin 166	V_{SS}	Pin 188	A0	Pin 214	V_{SS}	Pin 240	V_{TT}
Pin 141	DQ21	Pin 167	NC(TEST) *	Pin 189	V_{DD}	Pin 215	DQ46		
Pin 142	V_{SS}	Pin 168	RESET#	Pin 190	BA1	Pin 216	DQ47		
Pin 143	(T)DQS11 *			Pin 191	V_{DD}	Pin 217	V_{SS}		
Pin 144	(T)DQS11# *			Pin 192	RAS#	Pin 218	DQ52		
Pin 145	V_{SS}			Pin 193	S0#	Pin 219	DQ53		
Pin 146	DQ22			Pin 194	V_{DD}	Pin 220	V_{SS}		

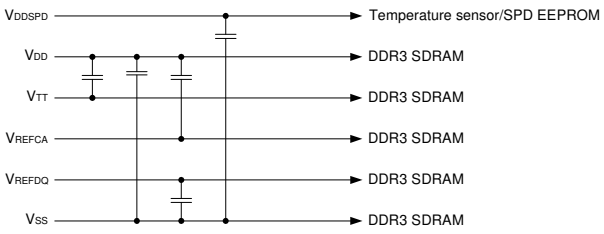
*) Following pin functions are depending on module configuration:

- (T)DQS is DQS for x4 based modules and TDQS for x8 based modules
- S1# is connected, but not used functionally for single rank DIMMs
- ODT1, CKE1 are not used for single rank modules
- S2# and S3# are only used for quad rank modules
- Event# is only used with temperature sensor equipped modules
- A13, A14, A15 are included in parity calculation. Function depends on DRAM address configuration
- A13 used for 1Gb, A13 & A14 for 2Gb, A13-A15 for 4Gb SDRAM

FUNCTIONAL BLOCK DIAGRAMM 4096MB DDR3 SDRAM RDIMM, 2 RANKS AND 18 COMPONENTS







MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-0.4	1.975	V
I/O Supply Voltage	V_{DDQ}	-0.4	1.975	V
V_{DD}L Supply Voltage	V_{DDL}	-0.4	1.975	V
Voltage on any pin relative to V_{SS}	V_{in}, V_{out}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	I_I			µA
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-5	5	µA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-8	8	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V
V_{DD}L Supply Voltage	V_{DDL}	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	0.49 x V_{DDQ}-20mV	0.50 x V_{DDQ}	0.51x V_{DDQ}+20mV	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1		V_{DDQ} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.1	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.175	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.175	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

Parameter & Test Condition		Symbol	max.		Unit
			10600-999	8500-777	
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	873	783	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	1008	963	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast Exit	I_{DD2P}	540	450	mA
	Slow Exit		216	216	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	630	540	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	666	576	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF} (always fast exit)		I_{DD3P}	630	540	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	720	630	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	1548	1368	mA

Parameter & Test Condition	Symbol	max.		Unit
		10600-999	8500-777	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	1593	1413	mA
BURST REFRESH CURRENT: $t_{CK} = t_{CK}$ (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	3600	3420	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	216	216	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RRD} = t_{RRD}$ (I_{DD}), $t_{RCD} = t_{RCD}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	3573	3123	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS			
SYMBOL	**10600-999**	**8500-777**	**Unit**
CL (I_{DD})	9	7	t_{CK}
t_{RCD} (I_{DD})	13.5	13.125	ns
t_{RC} (I_{DD})	49.5	50.625	ns
t_{RRD} (I_{DD})	6	7.5	ns
t_{CK} (I_{DD})	1.5	1,87	ns
t_{RAS} MIN (I_{DD})	36	37.5	ns
t_{RAS} MAX (I_{DD})	70,200	70,200	ns
t_{RP} (I_{DD})	13.5	13.125	ns
t_{RFC} (I_{DD})	160	160	ns

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS			10600-999		8500-777		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Clock cycle time	CL = 10	t_{CK} (10)	1.5	<1.875	-	-	ns
	CL = 9	t_{CK} (9)	1.5	<1.875	-	-	ns
	CL = 8	t_{CK} (8)	1.875	<2.5	-	-	ns
	CL = 7	t_{CK} (7)	1.875	<2.5	1.875	<2.5	ns
	CL = 6	t_{CK} (6)	2.5	3.3	2.5	3.3	ns
CK high-level width		t_{CH} (avg)	0.47	0.53	0.47	0.53	t_{CK}
CK low-level width		t_{CL} (avg)	0.47	0.53	0.47	0.53	t_{CK}
Data-out high-impedance window from CK/CK#		t_{HZ}		250		300	ps
Data-out low-impedance window from CK/CK#		t_{LZ}	-500	250	-600	300	ps
DQ and DM input setup time relative to DQS		$t_{DS(Base)}$	30		25		ps
DQ and DM input hold time relative to DQS		$t_{DH(Base)}$	65		100		ps
DQ and DM input setup time relative to DQS V_{REF}=1V/ns		t_{DS1V}	180		200		ps
DQ and DM input hold time relative to DQS V_{REF}=1V/ns		t_{DH1V}	165		200		ps
DQ and DM input pulse width (for each input)		t_{DIPW}	400		490		ps
DQS, DQS# to DQ skew, per access		t_{DQSQ}		125		150	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	0.38		0.38		t_{CK} (AVG)
DQS input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}
DQS input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}
DQS, DQS# rising to/from CK, CK#		t_{DQSCK}	-255	255	-300	300	ps
DQS, DQS# rising to/from CK, CK# when DLL disabled		$t_{DQSCK\ DLL\ DIS}$	1	10	1	10	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
DQS read preamble		t_{RPRE}	0.9	Note1	0.9	Note1	t_{CK}
DQS read postamble		t_{RPST}	0.3	Note2	0.3	Note2	t_{CK}
DQS write preamble		t_{WPRE}	0.9		0.9		t_{CK}
DQS write postamble		t_{WPST}	0.3		0.3		t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	620		780		ps
CTRL, CMD, Addr setup to CK, CK#		$t_{IS(Base)}$	65		125		ps
CTRL, CMD, Addr setup to CK, CK#	V_{REF} @ 1V/ns	$t_{IS(1V)}$	240		300		ps

1 The maximum preamble is bound by tLZDQS (MAX)

2 The maximum postamble is bound by tHZDQS (MAX)

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS			10600-999		8500-777		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
CTRL, CMD, Addr hold to CK,CK#		$t_{IH(Base)}$	140		200		ps
CTRL, CMD, Addr hold to CK,CK# V_{REF} @ 1V/ns		$t_{IH(1V)}$	240		300		ps
CAS# to CAS# command delay		t_{CCD}	4		4		t_{CK}
ACT to ACT (same bank) command period		t_{RC}	49.5		50.625		ns
ACT bank *a* to ACT bank *b* command		t_{RRD}	max 4nCK,10ns		max 4nCK,7.5ns		ns
ACT to READ or WRITE delay		t_{RCD}	13.5		13.125		ns
Four bank Activate period	1K Page size	t_{FAW}	30		37.5		ns
	2K Page size		45		50		
ACT to PRE command		t_{RAS}	36	70,200	37.5	70,200	ns
Internal READ to PRE command delay		t_{RTP}	max 4nCK,7.5ns		max 4nCK,7.5ns		ns
Write recovery time		t_{WR}	15		15		ns
Auto precharge write recovery + precharge time		t_{DAL}	$t_{WR} + t_{RP}/t_{CK}$		$t_{WR} + t_{RP}/t_{CK}$		ns
Internal WRITE to READ command delay		t_{WTR}	max 4nCK,7.5ns		max 4nCK,7.5ns		ns
PRE command period		t_{RP}	15		13.125		ns
LOAD MODE command cycle time		t_{MRD}	4		4		t_{CK}
REF to ACT or REF to REF command interval		t_{RFC}	160	70,200	160	70,200	ns
Average periodic refresh interval (0°C<= T_{CASE} <= 85 °C)		t_{REFI}		7.8		7.8	µs
(85°C<= T_{CASE} <= 95 °C)		t_{REFI}		3.9		3.9	µs
RTT turn-on from ODTL on reference		t_{AON}	-250	250	-300	300	ps
RTT turn-on from ODTL off reference		t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)		t_{AONPD}	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)		t_{AOFPD}	2	8,5	2	8,5	ns
RTT dynamic change skew		t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
Exit self refresh to commands not requiring a locked DLL		t_{XS}	max 5nCK,tRFC + 10ns		max 5nCK,tRFC + 10ns		ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		t_{WLS}	195		245		ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing		t_{WLH}	195		245		ps
First DQS, DQS# rising edge		t_{WLMRD}	40		40		t_{CK}
DQS, DQS# delay		$t_{WLDQSEN}$	25		25		t_{CK}
Exit reset from CKE HIGH to a valid command		t_{XPR}	max 5nCK, tRFC + 10ns		max 5nCK, tRFC + 10ns		
Begin power supply ramp to power supplies stable		t_{VDDPR}		200		200	ms

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

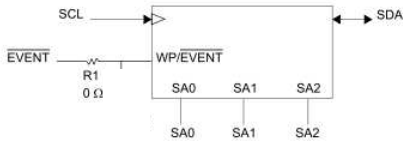
AC CHARACTERISTICS		10600-999		8500-777		
PARAMETER	SYMBOL	MIN	MAX	Min	MAX	Unit
RESET# LOW to power supplies stable	t_{RPS}		200		200	ms
RESET# LOW to I/O and RTT High-Z	t_{IOz}		20		20	ns
Exit precharge power-down to any non-READ command	t_{XP}	max 3nCK,6ns		max 3nCK,7.5ns		
CKE minimum high/low time	t_{CKE}	max 3nCK, 5.625ns		max 3nCK, 5.625ns		

Register Specifications

Parameter	Symbol	Pins	Min	Max	Units
DV supply voltage	V_{DD}	-	1.425	1.575	V
DC reference voltage	V_{REF}	-	0.49 × V_{DD} - 20mV	0.51 × V_{DD} + 20mV	V
DC termination Voltage	V_{TT}	-	0.49 × V_{DD} - 20mV	0.51 × V_{DD} + 20mV	V
DC high-level input voltage	$V_{IH(DC)}$	Address, control, command	V_{REF} + 100	V_{DD} + 400	mV
DC low-level input voltage	$V_{IL(DC)}$	Address, control, command	-400	V_{REF} – 100	mV
AC high-level input voltage	$V_{IH(AC)}$	Address, control, command	VREF + 175	VDD + 400	mV
AC low-level input voltage	$V_{IL(AC)}$	Address, control, command	-400	VREF - 175	mV
High-level output current	I_{OH}	Err_Out#	-	TBD	mA
Low-level output current	I_{OL}	Err_Out#	TBD	TBD	mA
High-level input voltage	$V_{IH(CMOS)}$	RESET#, MIRROR	0.65 × V_{DD}	V_{DD}	V
Low-level input voltage	$V_{IL(CMOS)}$	RESET#, MIRROR	0	.35 × V_{DD}	V
Differential input cross point voltage range	$V_{IX(AC)}$	CK, CK#, FBIN, FBIN#	0.5 × V_{DD} - 175mV	0.5 × V_{DD} + 175mV	V
Differential input voltage	$V_{ID(AC)}$	CK, CK#	350	TBD	mV

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR3 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.

Temperature Sensor with Serial Presence-Detect EEPROM



Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter / Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DDSPD}	+3	+3.6	V
Supply current: Vdd = 3.3V	I_{DD}		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	Vih	+1.45	V_{DDSPD} +1	V
Input low voltage: Logic 0; SCL, SDA	Vil	-	550	mV
Output low voltage: Iout = 2.1mA	Vol	-	400	mV
Input current	Iin	-5.0	5.0	µA
Temperature sensing range		TBD	TBD	℃
Temperature sensor accuracy		TBD	TBD	℃

A.C. Characteristics of Temperature Sensor

VCC = 3.3 V ± 10%, TA = −40°C to +125°C

Symbol	Parameter / Condition	Min	Max	Unit
f_{SCL}	SCL clock frequency	10	400	kHz
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
t_F	SDA fall time		300	ns
t_R	SDA rise time		300	ns
$t_{HD:DAT}$	Data hold time (accepted for Input Data)	0		ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
$t_{H:STA}$	Start condition hold time	600		ns
t_{HIGH}	High Period of SCL	600		ns
t_{LOW}	Low Period of SCL	1300		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	Start condition setup time	600		ns
$t_{SU:STO}$	Stop condition setup time	600		ns
$t_{TIMEOUT}$	SMBus SCL Clock Low Timeout	25	35	ms
t_i	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU}	Power-up Delay to Valid Temperature Recording		100	ms

Temperature Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T_A ≤ +95°C, active range	±1.0	℃
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	℃
	-40°C ≤ T_A ≤ +125°C, sensing range	±3.0	℃
ADC Resolution		12	Bits
Temperature Resolution		0.0625	℃
Conversion Time		100	Ms
Thermal Resistance[1] θ_{JA}	Junction-to-Ambient (Still Air)	92	℃/W

[1] Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where TJ is the junction temperature and TA is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

Slave Address Bits of Temperature Sensor

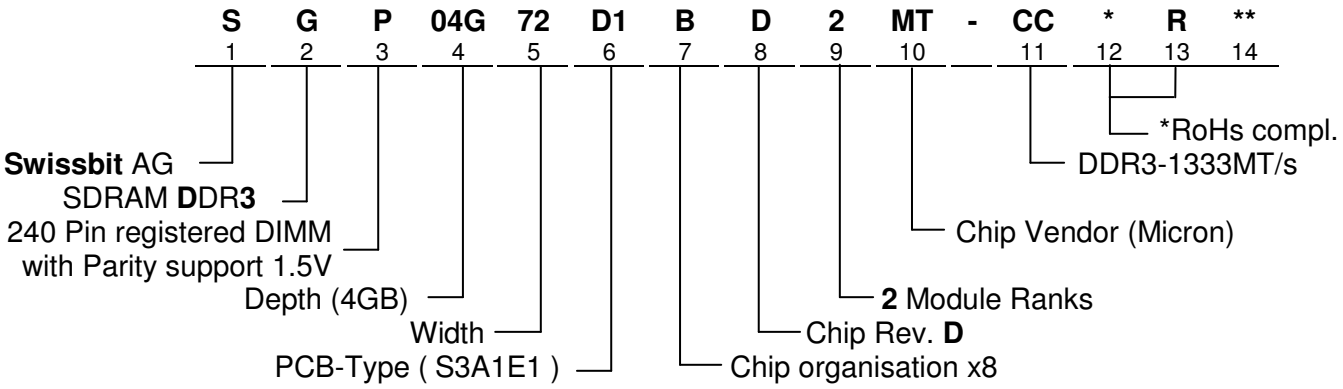
Device	Device Type Identifier				Select Address Signals			R/W#
	b7[1]	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/W#
Temp. Sensor	0	0	1	1	A_2	A_1	A_0	R/W#

[1] The most significant bit, b7, is sent first.

Byte	Byte Description	10600-999	8500-777
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISON	0x10	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x01	
4	SDRAM DEVICE DENSITY & BANKS	0x03	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x19	
6	BYTE 6 RESERVED	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x09	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x52	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME (tCK $_{MIN}$)	0x0C	0x0F
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0x7E	0x1E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME (tAA $_{MIN}$)	0x69	
17	MIN WRITE RECOVERY TIME (tWR $_{MIN}$)	0x78	
18	MIN RAS# TO CAS# DELAY (tRCD $_{MIN}$)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY (tRRD $_{MIN}$)	0x30	0x3C
20	MIN ROW PRECHARGE DELAY (tRP $_{MIN}$)	0x69	
21	UPPER NIBBLE FOR tRAS & tRC	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY (tRAS $_{MIN}$)	0x20	0x2C
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY (tRC $_{MIN}$)	0x89	0x95
24	MIN REFRESH RECOVERY DELAY (tRFC $_{MIN}$) LSB	0x00	
25	MIN REFRESH RECOVERY DELAY (tRFC $_{MIN}$) MSB	0x05	
26	MIN INTERNAL WRITE TO READ CMD DELAY (tWTR $_{MIN}$)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY (tRTP $_{MIN}$)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY (tFAW $_{MIN}$) MSB	0x00	0x01
29	MIN FOUR ACTIVE WINDOW DELAY (tFAW $_{MIN}$) LSB	0xF0	0x2C
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x82	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x05	

Byte	Byte Description	10600-999	8500-777
32	DDR3-MODULE THERMAL SENSOR	0x80	
33-59	BYTES 33-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x03	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x0A	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x05	
64	RDIMM THERMAL HEAT SPREADER SOLUTION	0x00	
65	REGISTER MFR ID (LSB)	0x04	
66	REGISTER MFR ID (MSB)	0xB3	
67	REGISTER REVISION NUMBER	0x03	
68	REGISTER TYPE	0x00	
69	RC1 (MS NIBBLE) / RC0 (LS NIBBLE) - RESERVED	0x00	
70	RC3 (MS NIBBLE) / RC2 (LS NIBBLE) – DRIVE STRENGTH, COMMAND/ADDRESS	0x50	
71-116	BYTES 71-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 Swizerland | 0x02 Germany | 0x03 USA	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0xEEDD	0x4D75
128-145	MODULE PART NUMBER	"SGP04G72D1BD2MT-xx"	
146	MODULE DIE REV	0x52	
147	MODULE PCB REV	0x54	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0x2C	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xff	

Part Number Code



* optional / additional information
** T = thermal sensor

Locations

Swissbit AG
Industriestrasse 4 – 8
CH – 9552 Bronschhofen
Switzerland
Phone: +41 (0)71 913 03 03
Fax: +41 (0)71 913 03 15

Swissbit Germany GmbH
Wolfener Strasse 36
D – 12681 Berlin
Germany
Phone: +49 (0)30 93 69 54 – 0
Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.
14 Willett Avenue, Suite 301A
Port Chester, NY 10573
USA
Phone: +1 914 935 1400
Fax: +1 914 935 9865

Swissbit NA, Inc.
3913 Todd Lane, Suite – 307
Austin, TX 78744
USA
Phone: +1 512 302 9001
Fax: +1 512 302 4808

Swissbit Japan, Inc.
3F Core Koenji,
2-1-24 Koenji-Kita, Suginami-Ku,
Tokyo 166-0002
Japan
Phone: +81 3 5356 3511
Fax: +81 3 5356 3512