4096MB DDR3 – SDRAM ECC SO-DIMM

204 Pin ECC SO-DIMM

SGN04G72G1BD2MT-CCRT

4096MB PC3-10600 in FBGA Technique

RoHS compliant

Options:

- Frequency / Latency — Marking
  - DDR3 1333 MHz CL9 — -CC
  - DDR3 1066 MHz CL7 — -BB
- Module densities
  4096MB with 18 dies and 1 rank
- Standard Grade (T_A) 0°C to 70°C; (Tc) 0°C to 85°C
  Grade W (T_A) -40°C to 85°C; (Tc) -40°C to 95°C

Environmental Requirements:

- Operating temperature (ambient)
  - Standard Grade 0°C to 70°C
  - Grade W -40°C to 85°C
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Features:

- 204-pin 72-bit Small Outline, Dual-In-Line Double Data Rate synchronous DRAM Module
- DDR3 - SDRAM component base Micron MT41J256M8
- V_{DD} = 1.5V ±0.075V, V_{DDQ} 1.5V ±0.075V
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- 1.5V I/O (SSTL_15 compatible)
- Serial Presence Detect with EEPROM
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Supports ECC error detection and correction
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 8 or 4
- Adjustable data-output drive strength
- On-die termination (ODT)
- Gold-contact pad
- This module family is fully pin and functional compatible to the JEDEC PC3-10600 spec. and JEDEC- Standard MO 268C. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

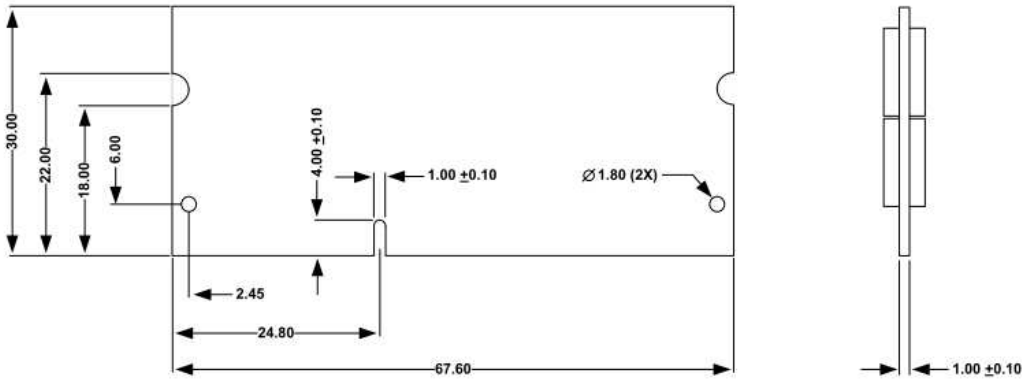


Figure: mechanical dimensions[1]

[1] if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 204-pin 8-byte DDR3 SDRAM ECC Small Outline Dual-In-line Memory Module (SO-UDIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured oct-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.
The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-UDIMM manufacturer (Swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Select	Col. Addr.	Refresh	Module Bank Select
512M x 72bit	18 x 256M x 8bit (2Gbit)	15	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions in mm
67.60 (long) x 30(high) x 3.80 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SGN04G72G1BD2MT-BB[W]RT	4096MB	8.5 GB/s	1.87ns/1066MT/s	8500-777
SGN04G72G1BD2MT-CC[W]RT	4096MB	10.6 GB/s	1.5ns/1333MT/s	10600-999

Pin Name

A0-9, A11 – A13	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0, BA1	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
CK0 – CK2	Clock Inputs, positive line
CK0# – CK2#	Clock Inputs, negative line
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)

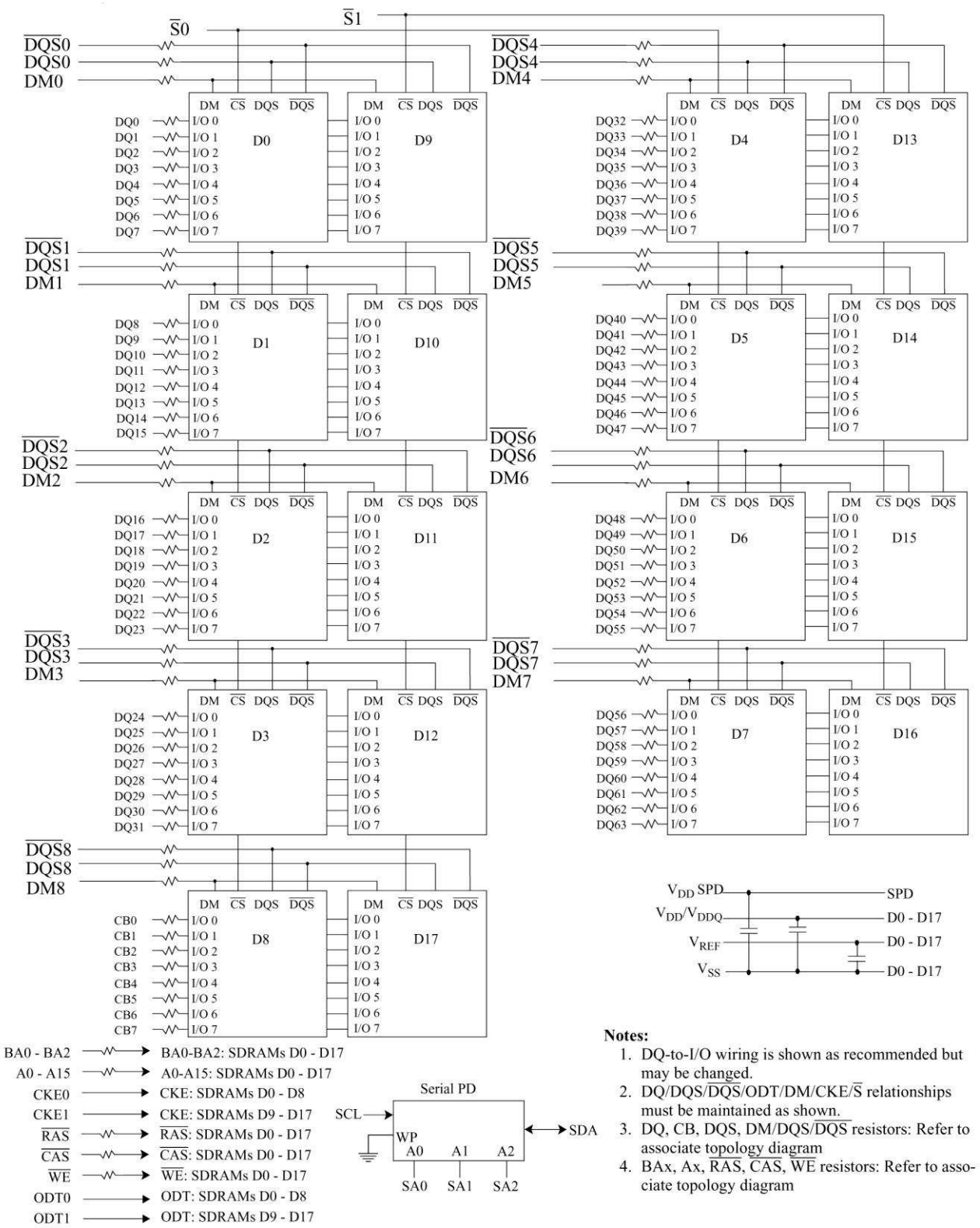
S0#, S1#	Chip Select
Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
V_{DD}	Supply Voltage (1.5V± 0.075V)
V_{REF}DQ	Reference voltage: DQ, DM (VDD/2)
V_{REF}CA	Reference voltage: Control, command, and address (VDD/2)
V_{SS}	Ground
V_{TT}	Termination voltage: Used for control, command, and address (VDD/2).
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

Frontside							
PIN	**Symbol**	**PIN**	**Symbol**	**PIN**	**Symbol**	**PIN**	**Symbol**
1	VREFDQ	53	VSS	103	A3	155	VSS
3	VSS	55	DQ24	105	A1	157	DM5
5	DQ0	57	DQ25	107	A0	159	DQ42
7	DQ1	59	DM3	109	VDD	161	DQ43
9	VSS	61	VSS	111	CK0	163	VSS
11	DM0	63	DQ26	113	CK0#	165	DQ48
13	DQ2	65	DQ27	115	VDD	167	DQ49
15	DQ3	67	VSS	117	A10/AP	169	VSS
17	VSS	69	CB0	119	BA0	171	DQS6#
19	DQ8	71	CB1	121	WE#	173	DQS6
21	DQ9	Key		123	VDD	175	VSS
23	VSS	73	VSS	125	CAS#	177	DQ50
25	DQS1#	75	DQS8#	127	S0#	179	DQ51
27	DQS1	77	DQS8#	129	S1#	181	VSS
29	VSS	79	VSS	131	VDD	183	DQ56
31	DQ10	81	CB2	133	DQ32	185	DQ57
33	DQ11	83	CB3	135	DQ33	187	VSS
35	VSS	85	VDD	137	VSS	189	DM7
37	DQ16	87	CKE0	139	DQS4#	191	DQ58
39	DQ17	89	CKE1	141	DQS4	193	DQ59
41	VSS	91	BA2	143	VSS	195	VSS
43	DQS2#	93	VDD	145	DQ34	197	SA0
45	DQS2	95	A12/BC#	147	DQ35	199	VDDSPD
47	VSS	97	A8	149	VSS	201	SA1
49	DQ18	99	A5	151	DQ40	203	VTT
51	DQ19	101	VDD	153	DQ41		

Backside							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
2	VSS	54	DQ28	104	A4	156	DQS5
4	DQ4	56	DQ29	106	A2	158	VSS
6	DQ5	58	VSS	108	BA1	160	DQ46
8	VSS	60	DQS3#	110	VDD	162	DQ47
10	DQS0#	62	DQS3	112	Par_IN/NC/CK1	164	VSS
12	DQS0	64	VSS	114	Err_Out#/ NC/CK1	166	DQ52
14	VSS	66	DQ30	116	VDD	168	DQ53
16	DQ6	68	DQ31	118	S3#	170	VSS
18	DQ7	70	VSS	120	S2#	172	DM6
20	VSS	72	CB4	122	RAS#	174	DQ54
22	DQ12	Key		124	VDD	176	DQ55
24	DQ13	74	CB5	126	ODT0	178	VSS
26	VSS	76	DM8	128	ODT1	180	DQ60
28	DM1	78	VSS	130	A13	182	DQ61
30	Reset#	80	CB6	132	VDD	184	VSS
32	VSS	82	CB7	134	DQ36	186	DQS7#
34	DQ14	84	VREFCA	136	DQ37	188	DQS7
36	DQ15	86	VDD	138	VSS	190	VSS
38	VSS	88	A15	140	DM4	192	DQ62
40	DQ20	90	A14	142	DQ38	194	DQ63
42	DQ21	92	A9	144	DQ39	196	VSS
44	DM2	94	VDD	146	VSS	198	EVENT#
46	VSS	96	A11	148	DQ44	200	SDA
48	DQ22	98	A7	150	DQ45	202	SCL
50	DQ23	100	A6	152	VSS	204	VTT
52	VSS	102	VDD	154	DQS5#		

FUNCTIONAL BLOCK DIAGRAMM 4096MB DDR3 SDRAM SODIMM, 2 RANK AND 18 COMPONENTS



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{\text{DQS}}$/ODT/DM/CKE/$\overline{\text{S}}$ relationships must be maintained as shown.
3. DQ, CB, DQS, DM/DQS/$\overline{\text{DQS}}$ resistors: Refer to associate topology diagram
4. BAx, Ax, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ resistors: Refer to associate topology diagram

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{DD}	-0.4	1.975	V
I/O Supply Voltage		$V_{DD}Q$	-0.4	1.975	V
$V_{DD}L$ Supply Voltage		$V_{DD}L$	-0.4	1.975	V
Voltage on any pin relative to V_{SS}		V_{in}, V_{out}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)		I_I			µA
	Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
	CK, CK#		-16	16	
	DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$)		I_{OZ}	-5	5	µA
	DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level		I_{VREF}	-8	8	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	$V_{DD}Q$	1.425	1.5	1.575	V
$V_{DD}L$ Supply Voltage	$V_{DD}L$	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.50 x $V_{DD}Q$	0.51x $V_{DD}Q$	V
I/O Termination Voltage (system)	V_{TT}	0.49 x $V_{DD}Q$-20mV	0.50 x $V_{DD}Q$	0.51x $V_{DD}Q$+20mV	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1		$V_{DD}Q$ + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.1	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.175	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.175	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; $V_{DD}Q$ = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

Parameter & Test Condition		Symbol	max. 10600-999	max. 8500-777	Unit
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DDO}	1278	1188	mA
OPERATING CURRENT :*) One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	1503	1323	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast Exit	I_{DD2P}	216	216	mA
	Slow Exit		720	630	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	1350	1170	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	1440	1260	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF} (always fast exit)		I_{DD3P}	1170	990	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	1710	1440	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	2403	2133	mA

Parameter & Test Condition	Symbol	max.		Unit
		10600-999	8500-777	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; $t_{CK} = t_{CK}$ (I_{DD}), $t_{RAS} = t_{RAS}$ MAX (I_{DD}), $t_{RP} = t_{RP}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	3078	2763	mA
BURST REFRESH CURRENT: $t_{CK} = t_{CK}$ (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	5490	5220	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	180	180	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); $t_{CK} = t_{CK}$ (I_{DD}), $t_{RC} = t_{RC}$ (I_{DD}), $t_{RRD} = t_{RRD}$ (I_{DD}), $t_{RCD} = t_{RCD}$ (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	4248	3978	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS			
SYMBOL	**10600-999**	**8500-777**	**Unit**
CL (I_{DD})	9	7	t_{CK}
t_{RCD} (I_{DD})	13.5	13.125	ns
t_{RC} (I_{DD})	49.5	50.625	ns
t_{RRD} (I_{DD})	6	7.5	ns
t_{CK} (I_{DD})	1.5	1,87	ns
t_{RAS} MIN (I_{DD})	36	37.5	ns
t_{RAS} MAX (I_{DD})	70,200	70,200	ns
t_{RP} (I_{DD})	13.5	13.125	ns
t_{RFC} (I_{DD})	110	110	ns

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; $V_{DD}Q$ = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS			10600-999		8500-777		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Clock cycle time					-	-	ns
	CL = 9	t_{CK} (9)	1.5	<1.875	-	-	ns
	CL = 8	t_{CK} (8)	1.875	<2.5	-	-	ns
	CL = 7	t_{CK} (7)	1.875	<2.5	1.875	<2.5	ns
	CL = 6	t_{CK} (6)	2.5	3.3	2.5	3.3	ns
CK high-level width		t_{CH}	0.47	0.53	0.47	0.53	t_{CK}
CK low-level width		t_{CL}	0.47	0.53	0.47	0.53	t_{CK}
Data-out high-impedance window from CK/CK#		t_{HZ}		0.25		0.3	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.5	0.25	-0.6	0.3	ns
DQ and DM input setup time relative to DQS		$t_{DS(Base)}$	30		25		ps
DQ and DM input hold time relative to DQS		$t_{DH(Base)}$	65		100		ps
DQ and DM input setup time relative to DQS V_{REF}=1V/ns		t_{DS1V}	180		200		ps
DQ and DM input hold time relative to DQS V_{REF}=1V/ns		t_{DH1V}	165		200		ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.4		0.49		ns
DQS, DQS# to DQ skew, per access		t_{DQSQ}		125		150	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	0.38		0.38		t_{CK} (AVG)
DQS input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}
DQS input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}
DQS, DQS# rising to/from CK, CK#		t_{DQSCK}	-255	+255	-300	300	ps
DQS, DQS# rising to/from CK, CK# when DLL disabled		$t_{DQSCK\ DLL\ DIS}$	1	10	1	10	ns
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}
DQS read preamble		t_{RPRE}	0.9	Note1	0.9	Note1	t_{CK}
DQS read postamble		t_{RPST}	0.3	Note2	0.3	Note2	t_{CK}
DQS write preamble		t_{WPRE}	0.9		0.9		t_{CK}
DQS write postamble		t_{WPST}	0.3		0.3		t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	400		490		ps
CTRL, CMD, Addr setup to CK, CK#		$t_{IS(Base)}$	65		125		ps
CTRL, CMD, Addr setup to CK, CK#	V_{REF} @ 1V/ns	$t_{IS(1V)}$	240		300		ps

1 The maximum preamble is bound by tLZDQS (MAX)
2 The maximum postamble is bound by tHZDQS (MAX)

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; $V_{DD}Q$ = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

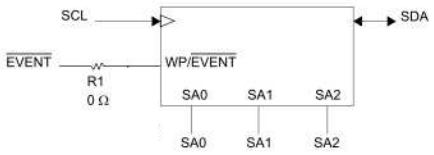
AC CHARACTERISTICS			10600-999		8500-777		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
CTRL, CMD, Addr hold to CK, CK#		$t_{IH(Base)}$	140		200		ps
CTRL, CMD, Addr hold to CK, CK# V_{REF} @ 1V/ns		$t_{IH(1V)}$	240		300		ps
CAS# to CAS# command delay		t_{CCD}	4		4		t_{CK}
ACTIVE to ACTIVE (same bank) command period		t_{RC}	49.5		50.625		ns
ACTIVE bank *a* to ACTIVE bank *b* command		t_{RRD}	6		7.5		ns
ACTIVE to READ or WRITE delay		t_{RCD}	13.5		13.125		ns
Four bank Activate period	1K Page size	t_{FAW}	30		37.5		ns
	2K Page size		45		50		
ACTIVE to PRECHARGE command		t_{RAS}	36	70,200	37.5	70,200	ns
Internal READ to precharge command delay		t_{RTP}	7.5		7.5		ns
Write recovery time		t_{WR}	15		15		ns
Auto precharge write recovery + precharge time		t_{DAL}	$t_{WR} + t_{RP}/t_{CK}$		$t_{WR} + t_{RP}/t_{CK}$		ns
Internal WRITE to READ command delay		t_{WTR}	7.5		7.5		ns
PRECHARGE command period		t_{RP}	15		13.125		ns
LOAD MODE command cycle time		t_{MRD}	6		7.5		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval		t_{RFC}	110	70,200	110	70,200	ns
Average periodic refresh interval		t_{REFI}		7.8		7.8	µs
RTT turn-on from ODTL on reference		t_{AON}	-250	250	-300	300	ps
RTT turn-on from ODTL off reference		t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)		t_{AONPD}	1	9	1	9	ns
Asynchronous RTT turn-off delay (power Down with DLL off)		t_{AOFPD}	1	9	1	9	ns
RTT dynamic change skew		t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
Exit self refresh to commands not requiring a locked DLL		t_{XS}	120		120		ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		t_{WLS}	195		245		ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing		t_{WLH}	195		245		ps
First DQS, DQS# rising edge		t_{WLMRD}	40		40		t_{CK}
DQS, DQS# delay		$t_{WLDQSEN}$	25		25		t_{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; $V_{DD}Q$ = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		10600-999		8500-777		
PARAMETER	SYMBOL	MIN	MAX	Min	MAX	Unit
Exit reset from CKE HIGH to a valid command	t_{XPR}	120		120		ns
Begin power supply ramp to power supplies stable	tV_{DDPR}		200		200	ms
RESET# LOW to power supplies stable	t_{RPS}		200		200	ms
RESET# LOW to I/O and RTT High-Z	t_{IOz}		20		20	ns
Exit precharge power-down to any non-READ command	t_{XP}	4.5		5.61		ns
CKE minimum high/low time	t_{CKE}	5.625		5.61		t_{CK}

Temperature Sensor with Serial Presence-Detect EEPROM



Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter / Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DDSPD}	+3	+3.6	V
Supply current: Vdd = 3.3V	I_{DD}		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	Vih	+1.45	V_{DDSPD} +1	V
Input low voltage: Logic 0; SCL, SDA	Vil	-	550	mV
Output low voltage: Iout = 2.1mA	Vol	-	400	mV
Input current	Iin	-5.0	5.0	µA
Temperature sensing range		TBD	TBD	℃
Temperature sensor accuracy		TBD	TBD	℃

A.C. Characteristics of Temperature Sensor

VCC = 3.3 V ± 10%, TA = −40°C to +125°C

Symbol	Parameter / Condition	Min	Max	Unit
f_{SCL}	SCL clock frequency	10	400	kHz
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
t_F	SDA fall time		300	ns
t_R	SDA rise time		300	ns
$t_{HD:DAT}$	Data hold time (accepted for Input Data)	0		ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
$t_{H:STA}$	Start condition hold time	600		ns
t_{HIGH}	High Period of SCL	600		ns
t_{LOW}	Low Period of SCL	1300		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	Start condition setup time	600		ns
$t_{SU:STO}$	Stop condition setup time	600		ns
$t_{TIMEOUT}$	SMBus SCL Clock Low Timeout	25	35	ms
T_i	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU}	Power-up Delay to Valid Temperature Recording		100	ms

Temperature Characteristics of Temperature Sensor

VCC = 3.3 V ± 10%, TA = −40°C to +125°C

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ TA ≤ +95°C, active range	±1.0	℃
	+40°C ≤ TA ≤ +125°C, monitor range	±2.0	℃
	-40°C ≤ TA ≤ +125°C, sensing range	±3.0	℃
ADC Resolution		12	Bits
Temperature Resolution		0.0625	℃
Conversion Time		100	Ms
Thermal Resistance[1] θ_{JA}	Junction-to-Ambient (Still Air)	92	℃/W

[1] Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where TJ is the junction temperature and TA is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

Slave Address Bits of Temperature Sensor

Device	Device Type Identifier				Select Address Signals			R/W#
	b7[1]	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/W#
Temp. Sensor	0	0	1	1	A_2	A_1	A_0	R/W#

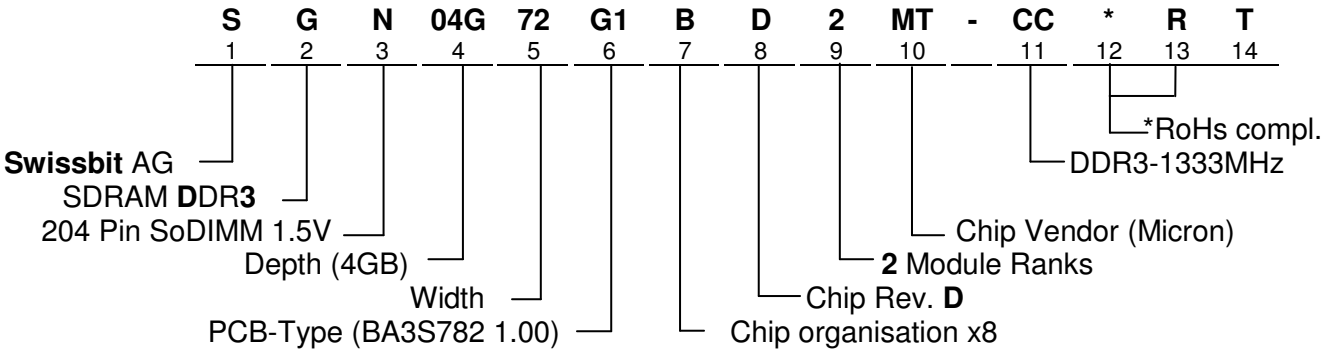
[1] The most significant bit, b7, is sent first.

SERIAL PRESENCE-DETECT MATRIX

Byte	Byte Description	10600-999	8500-777
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISON	0x10	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x08	
4	SDRAM DEVICE DENSITY & BANKS	0x03	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x19	
6	BYTE 6 RESERVED	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x09	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x52	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME (TCKMIN)	0x0C	0x0F
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0x7E	0x1E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME (TAAMIN)	0x69	
17	MIN WRITE RECOVERY TIME (TWRMIN)	0x78	
18	MIN RAS# TO CAS# DELAY (TRCDMIN)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY (TRRDMIN)	0x30	0x3C
20	MIN ROW PRECHARGE DELAY (TRPMIN)	0x69	
21	UPPER NIBBLE FOR TRAS & TRC	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY (TRASMIN)	0x20	0x2C
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY (TRCMIN)	0x89	0x95
24	MIN REFRESH RECOVERY DELAY (TRFCMIN) LSB	0x00	
25	MIN REFRESH RECOVERY DELAY (TRFCMIN) MSB	0x05	
26	MIN INTERNAL WRITE TO READ CMD DELAY (TWTRMIN)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY (TRTPMIN)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) MSB	0x00	0x01
29	MIN FOUR ACTIVE WINDOW DELAY (TFAWMIN) LSB	0xF0	0x2C
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x82	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x01	

Byte	Byte Description	10600-999	8500-777
32	DDR3-MODULE THERMAL SENSOR	0x80	
33-59	BYTES 33-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x0F	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x05	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x00	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Swizerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0xF854	0xAB51
128-145	MODULE PART NUMBER	"SGN04G72G1BD2MT-xx"	
146	MODULE DIE REV	0x52	
147	MODULE PCB REV	0x54	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0x2C	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xff	

Part Number Code



* optional / additional information

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