

# 1024MB DDR3 – SDRAM SO-DIMM

## 204 Pin SO-DIMM

SGN01G64D2BG1MT-xxRT

1GByte in FBGA Technology

RoHS compliant

### Options:

- |                               |                                    |         |
|-------------------------------|------------------------------------|---------|
| ▪ Data Rate / Latency         |                                    | Marking |
| DDR3 1066 MT/s CL7            |                                    | -BB     |
| DDR3 1333 MT/s CL9            |                                    | -CC     |
| ▪ Module Density              |                                    |         |
| 1024MB with 8 dies and 1 rank |                                    |         |
| ▪ Standard Grade              | (T <sub>A</sub> ) 0°C to 70°C      |         |
|                               | (T <sub>C</sub> ) 0°C to 85°C      |         |
| Grade E                       | (T <sub>A</sub> ) 0°C to 85°C      |         |
|                               | (T <sub>C</sub> ) 0°C to 95°C *)   |         |
| Grade W                       | (T <sub>A</sub> ) -40°C to 85°C    |         |
|                               | (T <sub>C</sub> ) -40°C to 95°C *) |         |

\*) The refresh rate has to be doubled when 85°C < T<sub>C</sub> < 95°C

### Environmental Requirements:

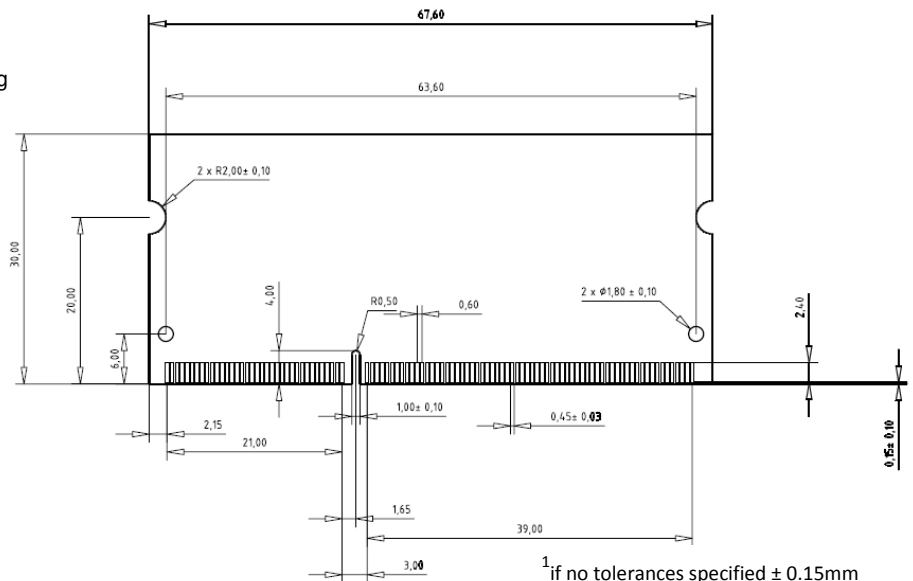
- Operating temperature (ambient)
 

Standard Grade	0°C to 70°C
Grade E	0°C to 85°C
Grade W	-40°C to 85°C
- Operating Humidity  
10% to 90% relative humidity, noncondensing
- Operating Pressure  
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature  
-55°C to 100°C
- Storage Humidity  
5% to 95% relative humidity, noncondensing
- Storage Pressure  
1682 PSI (up to 5000 ft.) at 50°C

### Features:

- 204-pin 64-bit DDR3 Small Outline Dual-In-Line Double Data Rate Synchronous DRAM module
- Module organization: single rank 128M x 64
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC3-10600 spec. and JEDEC- Standard MO-268. (see [www.jedec.org](http://www.jedec.org))
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
- **DDR3 - SDRAM component Micron MT41J128M8JP-15E :G**
- 128Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- V<sub>DD</sub> = 1.5V ±0.075V, V<sub>DDQ</sub> 1.5V ±0.075V
- 1.5V I/O ( SSTL\_15 compatible)
- 8-bit pre-fetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

Figure: mechanical dimensions<sup>1</sup>



This Swissbit module is an industry standard 204-pin 8-byte DDR3 SDRAM Small Outline Dual-In-line Memory Module (SO-DIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL\_15 compatible.

The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I<sup>2</sup>C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-DIMM manufacturer (Swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

### Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
128M x 64bit	8 x 128M x 8bit (1024Mbit)	14	BA0, BA1, BA2	10	8k	S0#

### Module Dimensions

in mm

67.60 (long) x 30(high) x 3.80 [max] (thickness)

### Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SGN01G64D2BG1MT-BB[E/W]RT	1024 MB	8.5 GB/s	1.87ns/1066MT/s	7-7-7
SGN01G64D2BG1MT-CC[E/W]RT	1024 MB	10.6 GB/s	1.5ns/1333MT/s	9-9-9

### Pin Name

A0-9, A11 – A13	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
S0#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE	Clock Enable
ODT0	On-Die Termination
CK0	Clock Inputs, positive line
CK0#	Clock Inputs, negative line

V <sub>DD</sub>	Supply Voltage (1.5V± 0.075V)
V <sub>REFDQ</sub>	Reference voltage: DQ, DM (V <sub>DD</sub> /2)
V <sub>REFCA</sub>	Reference voltage: Control, command, and address (V <sub>DD</sub> /2)
V <sub>SS</sub>	Ground
V <sub>TT</sub>	Termination voltage: Used for control, command, and address (V <sub>DD</sub> /2).
V <sub>DDSPD</sub>	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
NC	No Connection

**Pin Configuration**

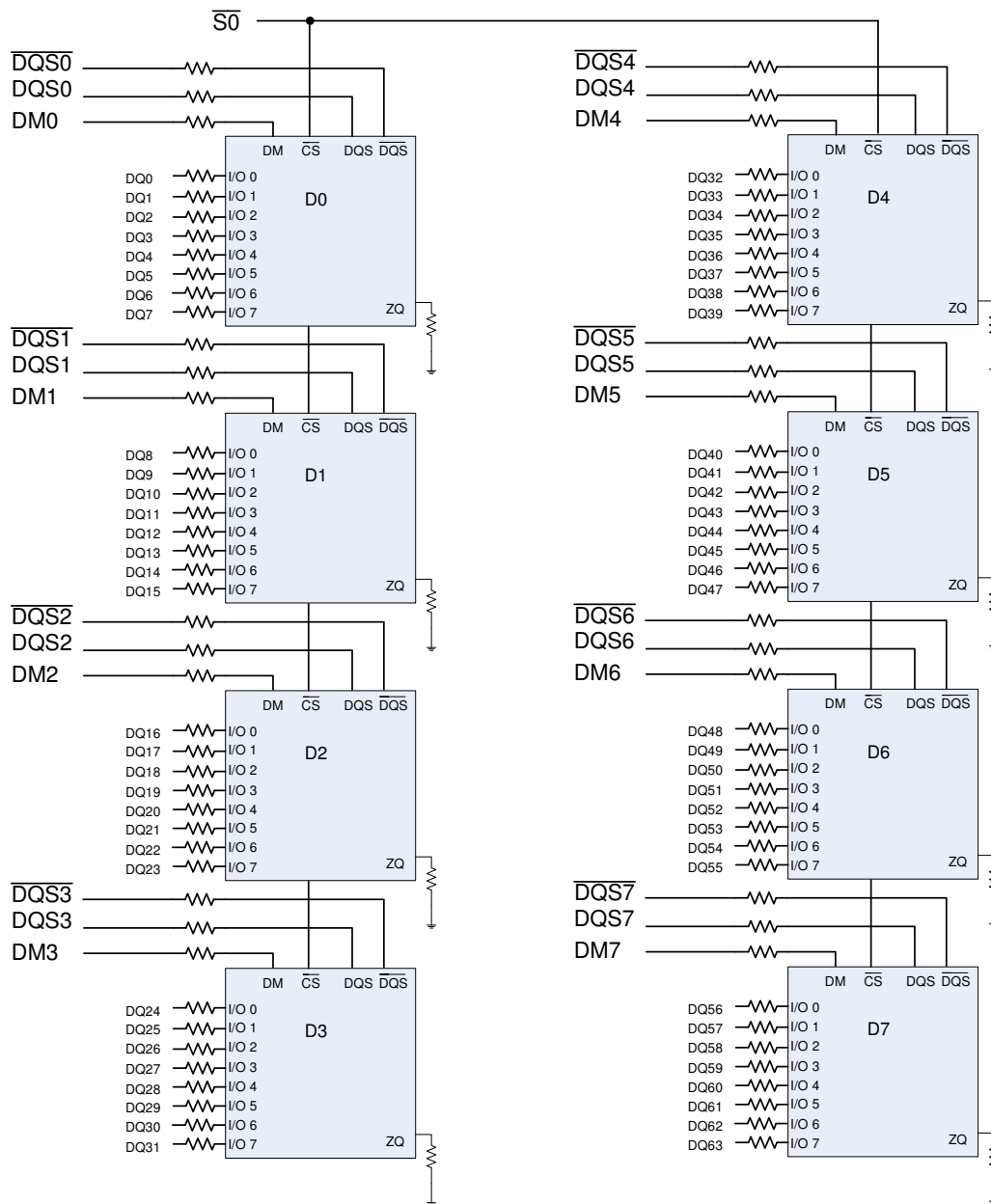
Frontside							
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V <sub>REFDQ</sub>	53	DQ19	103	CK0#	155	V <sub>SS</sub>
3	V <sub>SS</sub>	55	V <sub>SS</sub>	105	V <sub>DD</sub>	157	DQ42
5	DQ0	57	DQ24	107	A10/AP	159	DQ43
7	DQ1	59	DQ25	109	BA0	161	V <sub>SS</sub>
9	V <sub>SS</sub>	61	V <sub>SS</sub>	111	V <sub>DD</sub>	163	DQ48
11	DM0	63	DM3	113	WE#	165	DQ49
13	V <sub>SS</sub>	65	V <sub>SS</sub>	115	CAS#	167	V <sub>SS</sub>
15	DQ2	67	DQ26	117	V <sub>DD</sub>	169	DQS6#
17	DQ3	69	DQ27	119	A13	171	DQS6
19	V <sub>SS</sub>	71	V <sub>SS</sub>	121	NC (S1#)	173	V <sub>SS</sub>
21	DQ8	<b>KEY</b>		123	V <sub>DD</sub>	175	DQ50
23	DQ9	73	CKE0	125	NC (TEST)	177	DQ51
25	V <sub>SS</sub>	75	V <sub>DD</sub>	127	V <sub>SS</sub>	179	V <sub>SS</sub>
27	DQS1#	77	NC	129	DQ32	181	DQ56
29	DQS1	79	BA2	131	DQ33	183	DQ57
31	V <sub>SS</sub>	81	V <sub>DD</sub>	133	V <sub>SS</sub>	185	V <sub>SS</sub>
33	DQ10	83	A12/BC#	135	DQS4#	187	DM7
35	DQ11	85	A9	137	DQS4	189	V <sub>SS</sub>
37	V <sub>SS</sub>	87	V <sub>DD</sub>	139	V <sub>SS</sub>	191	DQ58
39	DQ16	89	A8	141	DQ34	193	DQ59
41	DQ17	91	A5	143	DQ35	195	V <sub>SS</sub>
43	V <sub>SS</sub>	93	V <sub>DD</sub>	145	V <sub>SS</sub>	197	SA0
45	DQS2#	95	A3	147	DQ40	199	V <sub>DDSPD</sub>
47	DQS2	97	A1	149	DQ41	201	SA1
49	V <sub>SS</sub>	99	V <sub>DD</sub>	151	V <sub>SS</sub>	203	V <sub>TT</sub>
51	DQ18	101	CK0	153	DM5		

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

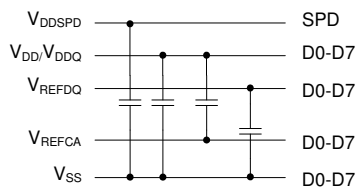
Backside							
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
2	V <sub>SS</sub>	54	V <sub>SS</sub>	104	NC (CK1#)	156	V <sub>SS</sub>
4	DQ4	56	DQ28	106	V <sub>DD</sub>	158	DQ46
6	DQ5	58	DQ29	108	BA1	160	DQ47
8	V <sub>SS</sub>	60	V <sub>SS</sub>	110	RAS#	162	V <sub>SS</sub>
10	DQS0#	62	DQS3#	112	V <sub>DD</sub>	164	DQ52
12	DQS0	64	DQS3	114	S0#	166	DQ53
14	V <sub>SS</sub>	66	V <sub>SS</sub>	116	ODT0	168	V <sub>SS</sub>
16	DQ6	68	DQ30	118	V <sub>DD</sub>	170	DM6
18	DQ7	70	DQ31	120	NC (ODT1)	172	V <sub>SS</sub>
20	V <sub>SS</sub>	72	V <sub>SS</sub>	122	NC	174	DQ54
22	DQ12	<b>KEY</b>		124	V <sub>DD</sub>	176	DQ55
24	DQ13	74	NC (CKE1)	126	V <sub>REFCA</sub>	178	V <sub>SS</sub>
26	V <sub>SS</sub>	76	V <sub>DD</sub>	128	V <sub>SS</sub>	180	DQ60
28	DM1	78	NC (A15)	130	DQ36	182	DQ61
30	NC (RESET#)	80	NC (A14)	132	DQ37	184	V <sub>SS</sub>
32	V <sub>SS</sub>	82	V <sub>DD</sub>	134	V <sub>SS</sub>	186	DQS7#
34	DQ14	84	A11	136	DM4	188	DQS7
36	DQ15	86	A7	138	V <sub>SS</sub>	190	V <sub>SS</sub>
38	V <sub>SS</sub>	88	V <sub>DD</sub>	140	DQ38	192	DQ62
40	DQ20	90	A6	142	DQ39	194	DQ63
42	DQ21	92	A4	144	V <sub>SS</sub>	196	V <sub>SS</sub>
44	V <sub>SS</sub>	94	V <sub>DD</sub>	146	DQ44	198	EVENT#
46	DM2	96	A2	148	DQ45	200	SDA
48	V <sub>SS</sub>	98	A0	150	V <sub>SS</sub>	202	SCL
50	DQ22	100	V <sub>DD</sub>	152	DQS5#	204	V <sub>TT</sub>
52	DQ23	102	NC (CK1)	154	DQS5		

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

**FUNCTIONAL BLOCK DIAGRAM 1024MB DDR3 SDRAM SODIMM,  
1 RANK AND 8 COMPONENTS**



- BA0-BA2 → BA0-BA2: SDRAM D0-D7
- A0-A13 → A0-A13: SDRAM D0-D7
- RAS → RAS: SDRAM D0-D7
- CAS → CAS: SDRAM D0-D7
- WE → WE: SDRAM D0-D7
- ODT0 → ODT: SDRAM D0-D7
- CKE0 → CKE: SDRAM D0-D7
- CK0 → CK: SDRAM D0-D7
- CK0 → CK: SDRAM D0-D7
- RESET → RESET: SDRAM D0-D7



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationship must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDED document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

**MAXIMUM ELECTRICAL DC CHARACTERISTICS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{DD}$	-0.4	1.975	V
I/O Supply Voltage	$V_{DDQ}$	-0.4	1.975	V
$V_{DDL}$ Supply Voltage	$V_{DDL}$	-0.4	1.975	V
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.4	1.975	V
<b>INPUT LEAKAGE CURRENT</b> Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	$I_I$			$\mu A$
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
<b>OUTPUT LEAKAGE CURRENT</b> (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu A$
DQ, DQS, DQS#				
$V_{REF}$ LEAKAGE CURRENT ; $V_{REF}$ is on a valid level	$I_{VREF}$	-8	8	$\mu A$

**DC OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	$V_{DD}$	1.425	1.5	1.575	V
I/O Supply Voltage	$V_{DDQ}$	1.425	1.5	1.575	V
$V_{DDL}$ Supply Voltage	$V_{DDL}$	1.425	1.5	1.575	V
I/O Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	$V_{TT}$	$0.49 \times V_{DDQ} - 20mV$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ} + 20mV$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.1$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.1$	V

**AC INPUT OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.175$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.175$	V

**CAPACITANCE**

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

**I<sub>DD</sub> Specifications and Conditions**

 (0°C ≤ T<sub>CASE</sub> ≤ + 85°C; V<sub>DDQ</sub> = +1.5V ± 0.075V, V<sub>DD</sub> = +1.5V ± 0.075V)

Parameter & Test Condition	Symbol	max.		Unit	
		10600-999	8500-777		
<b>OPERATING CURRENT *) :</b> One device bank Active-Precharge; t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	880	800	mA	
<b>OPERATING CURRENT *) :</b> One device bank; Active-Read-Precharge; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MIN (I <sub>DD</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I <sub>DD4W</sub>	I <sub>DD1</sub>	1040	960	mA	
<b>PRECHARGE POWER-DOWN CURRENT:</b> All device banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	Fast Exit	I <sub>DD2P</sub>	320	280	mA
	Slow Exit		96	96	
<b>PRECHARGE QUIET STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD2Q</sub>	480	424	mA	
<b>PRECHARGE STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD2N</sub>	520	440	mA	
<b>ACTIVE POWER-DOWN CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub> (always fast exit)	I <sub>DD3P</sub>	320	280	mA	
<b>ACTIVE STANDBY CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD3N</sub>	496	456	mA	
<b>OPERATING READ CURRENT:</b> All device banks open, Continuous burst reads; One module rank active; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD4R</sub>	1600	1280	mA	

Parameter & Test Condition	Symbol	max.		Unit
		10600-999	8500-777	
<b>OPERATING WRITE CURRENT:</b> All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD4W</sub>	1760	1520	mA
<b>BURST REFRESH CURRENT:</b> t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); refresh command at every t <sub>RFC</sub> (I <sub>DD</sub> ) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD5</sub>	1920	1760	mA
<b>SELF REFRESH CURRENT:</b> CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V <sub>REF</sub> ; DQ's are floating at V <sub>REF</sub>	I <sub>DD6</sub>	48	48	mA
<b>OPERATING CURRENT*) :</b> Four device bank interleaving READs, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = t <sub>RCD</sub> (I <sub>DD</sub> ) - 1 x t <sub>CK</sub> (I <sub>DD</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ), t <sub>RRD</sub> = t <sub>RRD</sub> (I <sub>DD</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I <sub>DD7</sub>	3920	3120	mA

\*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**TIMING VALUES USED FOR I<sub>DD</sub> MEASUREMENT**

I <sub>DD</sub> MEASUREMENT CONDITIONS			
SYMBOL	10600-999	8500-777	Unit
CL (I <sub>DD</sub> )	9	7	t <sub>CK</sub>
t <sub>RCD</sub> (I <sub>DD</sub> )	13.5	13.125	ns
t <sub>RC</sub> (I <sub>DD</sub> )	49.5	50.625	ns
t <sub>RRD</sub> (I <sub>DD</sub> )	6	7.5	ns
t <sub>CK</sub> (I <sub>DD</sub> )	1.5	1.87	ns
t <sub>RAS</sub> MIN (I <sub>DD</sub> )	36	37.5	ns
t <sub>RAS</sub> MAX (I <sub>DD</sub> )	70'200	70'200	ns
t <sub>RP</sub> (I <sub>DD</sub> )	13.5	13.125	ns
t <sub>RFC</sub> (I <sub>DD</sub> )	110	110	ns

**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

 (0°C ≤ T<sub>CASE</sub> ≤ +85°C; V<sub>DDQ</sub> = +1.5V ± 0.075V, V<sub>DD</sub> = +1.5V ± 0.075V)

AC CHARACTERISTICS			10600-999		8500-777		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
Clock cycle time	CL = 10	t <sub>CK</sub> (10)	1.5	<1.875	-	-	ns
	CL = 9	t <sub>CK</sub> (9)	1.5	<1.875	-	-	ns
	CL = 8	t <sub>CK</sub> (8)	1.875	<2.5	-	-	ns
	CL = 7	t <sub>CK</sub> (7)	1.875	<2.5	1.875	<2.5	ns
	CL = 6	t <sub>CK</sub> (6)	2.5	3.3	2.5	3.3	ns
CK high-level width		t <sub>CH</sub> (avg)	0.47	0.53	0.47	0.53	t <sub>CK</sub>
CK low-level width		t <sub>CL</sub> (avg)	0.47	0.53	0.47	0.53	t <sub>CK</sub>
Data-out high-impedance window from CK/CK#		t <sub>HZ</sub>		250		300	ps
Data-out low-impedance window from CK/CK#		t <sub>LZ</sub>	-500	250	-600	300	ps
DQ and DM input setup time relative to DQS		t <sub>DS(Base)</sub>	30		25		ps
DQ and DM input hold time relative to DQS		t <sub>DH(Base)</sub>	65		100		ps
DQ and DM input setup time relative to DQS V <sub>REF</sub> =1V/ns		t <sub>DS1V</sub>	180		200		ps
DQ and DM input hold time relative to DQS V <sub>REF</sub> =1V/ns		t <sub>DH1V</sub>	165		200		ps
DQ and DM input pulse width ( for each input )		t <sub>DIPW</sub>	400		490		ps
DQS, DQS# to DQ skew, per access		t <sub>DQSQ</sub>		125		150	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t <sub>QH</sub>	0.38		0.38		t <sub>CK</sub> (AVG)
DQS input high pulse width		t <sub>DQSH</sub>	0.45	0.55	0.45	0.55	t <sub>CK</sub>
DQS input low pulse width		t <sub>DQSL</sub>	0.45	0.55	0.45	0.55	t <sub>CK</sub>
DQS, DQS# rising to/from CK, CK#		t <sub>DQSCK</sub>	-255	255	-300	300	ps
DQS, DQS# rising to/from CK, CK# when DLL disabled		t <sub>DQSCK</sub> DLL DIS	1	10	1	10	ns
DQS falling edge to CK rising - setup time		t <sub>DSS</sub>	0.2		0.2		t <sub>CK</sub>
DQS falling edge from CK rising - hold time		t <sub>DSH</sub>	0.2		0.2		t <sub>CK</sub>
DQS read preamble		t <sub>RPRE</sub>	0.9	Note1	0.9	Note1	t <sub>CK</sub>
DQS read postamble		t <sub>RPST</sub>	0.3	Note2	0.3	Note2	t <sub>CK</sub>
DQS write preamble		t <sub>WPRE</sub>	0.9		0.9		t <sub>CK</sub>
DQS write postamble		t <sub>WPST</sub>	0.3		0.3		t <sub>CK</sub>
Positive DQS latching edge to associated clock edge		t <sub>DQSS</sub>	- 0.25	+ 0.25	- 0.25	+ 0.25	t <sub>CK</sub>
Address and control input pulse width ( for each input )		t <sub>IPW</sub>	620		780		ps
CTRL, CMD, Addr setup to CK, CK#		t <sub>IS(Base)</sub>	65		125		ps
CTRL, CMD, Addr setup to CK, CK# V <sub>REF</sub> @ 1V/ns		t <sub>IS(1V)</sub>	240		300		ps

- 1 The maximum preamble is bound by t<sub>LZDQS</sub> (MAX)
- 2 The maximum postamble is bound by t<sub>HZDQS</sub> (MAX)

**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.5\text{V} \pm 0.075\text{V}, V_{\text{DD}} = +1.5\text{V} \pm 0.075\text{V})$ 

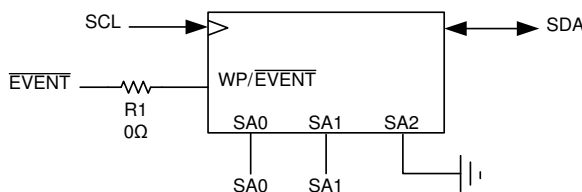
AC CHARACTERISTICS		10600-999		8500-777		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
CTRL, CMD, Addr hold to CK, CK#	$t_{\text{IH(Base)}}$	140		200		ps
CTRL, CMD, Addr hold to CK, CK# $V_{\text{REF}} @ 1\text{V/ns}$	$t_{\text{IH(1V)}}$	240		300		ps
CAS# to CAS# command delay	$t_{\text{CCD}}$	4		4		$t_{\text{CK}}$
ACTIVE to ACTIVE (same bank) command period	$t_{\text{RC}}$	49.5		50.625		ns
ACTIVE bank a to ACTIVE bank b command	$t_{\text{RRD}}$	max 4nCK,10ns		max 4nCK,7.5ns		ns
ACTIVE to READ or WRITE delay	$t_{\text{RCD}}$	13.5		13.125		ns
Four bank Activate period	$t_{\text{FAW}}$	1K Page size 30		37.5		ns
2K Page size		45		50		
ACTIVE to PRECHARGE command	$t_{\text{RAS}}$	36	70'200	37.5	70'200	ns
Internal READ to precharge command delay	$t_{\text{RTP}}$	max 4nCK,7.5ns		max 4nCK,7.5ns		ns
Write recovery time	$t_{\text{WR}}$	15		15		ns
Auto precharge write recovery + precharge time	$t_{\text{DAL}}$	$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$		$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$		ns
Internal WRITE to READ command delay	$t_{\text{WTR}}$	max 4nCK,7.5ns		max 4nCK,7.5ns		ns
PRECHARGE command period	$t_{\text{RP}}$	15		13.125		ns
LOAD MODE command cycle time	$t_{\text{MRD}}$	4		4		$t_{\text{CK}}$
REFRESH to ACTIVE or REFRESH to REFRESH command interval	$t_{\text{RFC}}$	110	70'200	110	70'200	ns
Average periodic refresh interval $0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	$t_{\text{REFI}}$		7.8		7.8	$\mu\text{s}$
$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	$t_{\text{REFI (IT)}}$		3.9		3.9	
RTT turn-on from ODTL on reference	$t_{\text{AON}}$	-250	250	-300	300	ps
RTT turn-on from ODTL off reference	$t_{\text{AOF}}$	0.3	0.7	0.3	0.7	$t_{\text{CK}}$
Asynchronous RTT turn-on delay (power Down with DLL off)	$t_{\text{AONPD}}$	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)	$t_{\text{AOFPD}}$	2	8,5	2	8,5	ns
RTT dynamic change skew	$t_{\text{ADC}}$	0.3	0.7	0.3	0.7	$t_{\text{CK}}$
Exit self refresh to commands not requiring a locked DLL	$t_{\text{XS}}$	max 5nCK,tR FC + 10ns		max 5nCK,tR FC + 10ns		ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing	$t_{\text{WLS}}$	195		245		ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing	$t_{\text{WLH}}$	195		245		ps
First DQS, DQS# rising edge	$t_{\text{WLMRD}}$	40		40		$t_{\text{CK}}$
DQS, DQS# delay	$t_{\text{WLDQSEN}}$	25		25		$t_{\text{CK}}$

**DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**

(0°C ≤ T<sub>CASE</sub> ≤ + 85°C; V<sub>DDQ</sub> = +1.5V ± 0.075V, V<sub>DD</sub> = +1.5V ± 0.075V)

AC CHARACTERISTICS		10600-999		8500-777		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit
Exit reset from CKE HIGH to a valid command	t <sub>XPR</sub>	max 5nCK, t <sub>REFC</sub> + 10ns		max 5nCK, t <sub>REFC</sub> + 10ns		t <sub>CK</sub>
Begin power supply ramp to power supplies stable	t <sub>VDDPR</sub>		200		200	ms
RESET# LOW to power supplies stable	t <sub>RPS</sub>		200		200	ms
RESET# LOW to I/O and RTT High-Z	t <sub>IOz</sub>		20		20	ns
Exit precharge power-down to any non-READ command	t <sub>XP</sub>	max 3nCK,6ns		max 3nCK,7.5ns		t <sub>CK</sub>
CKE minimum high/low time	t <sub>CKE</sub>	max 3nCK, 5.625ns		max 3nCK, 5.625ns		t <sub>CK</sub>

**Temperature Sensor with Serial Presence-Detect EEPROM**



**Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions**

Parameter / Condition	Symbol	MIN	MAX	Unit
Supply voltage	V <sub>DDSPD</sub>	+3	+3.6	V
Supply current: V <sub>DD</sub> = 3.3V	I <sub>DD</sub>		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V <sub>IH</sub>	+1.45	V <sub>DDSPD</sub> + 1	V
Input low voltage: Logic 0; SCL, SDA	V <sub>IL</sub>	-	550	mV
Output low voltage: I <sub>OUT</sub> = 2.1mA	V <sub>OL</sub>	-	400	mV
Input current	I <sub>IN</sub>	-5.0	5.0	µA
Temperature sensing range		TBD	TBD	°C
Temperature sensor accuracy		TBD	TBD	°C

### A.C. Characteristics of Temperature Sensor

$V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$

Symbol	Parameter / Condition	MIN	MAX	Unit
$f_{SCL}$	SCL clock frequency	10	400	kHz
$t_{BUF}$	Bus Free Time Between STOP and START	1300		ns
$t_F$	SDA fall time		300	ns
$t_R$	SDA rise time		300	ns
$t_{HD:DAT}$	Data hold time (accepted for Input Data)	0		ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
$t_{H:STA}$	Start condition hold time	600		ns
$t_{HIGH}$	High Period of SCL	600		ns
$t_{LOW}$	Low Period of SCL	1300		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	Start condition setup time	600		ns
$t_{SU:STO}$	Stop condition setup time	600		ns
$t_{TIMEOUT}$	SMBus SCL Clock Low Timeout	25	35	ms
$t_I$	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
$t_{WR}$	Write Cycle Time		5	ms
$t_{PU}$	Power-up Delay to Valid Temperature Recording		100	ms

### Temperature Characteristics of Temperature Sensor

$V_{CC} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$

Parameter	Test Conditions/Comments	MAX	Unit
Temperature Reading Error Class B, JC42.4 compliant	$+75^\circ\text{C} \leq T_A \leq +95^\circ\text{C}$ , active range	$\pm 1.0$	$^\circ\text{C}$
	$+40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , monitor range	$\pm 2.0$	$^\circ\text{C}$
	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , sensing range	$\pm 3.0$	$^\circ\text{C}$
ADC Resolution		12	Bits
Temperature Resolution		0.0625	$^\circ\text{C}$
Conversion Time		100	Ms
Thermal Resistance <sup>1</sup> $\theta_{JA}$	Junction-to-Ambient (Still Air)	92	$^\circ\text{C}/\text{W}$

<sup>1</sup> Power Dissipation is defined as  $P_J = (T_J - T_A)/\theta_{JA}$ , where  $T_J$  is the junction temperature and  $T_A$  is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

### Slave Address Bits of Temperature Sensor

Device	Device Type Identifier				Select Address Signals			R/W#
	b7 <sup>1</sup>	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W#
Temp. Sensor	0	0	1	1	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/W#

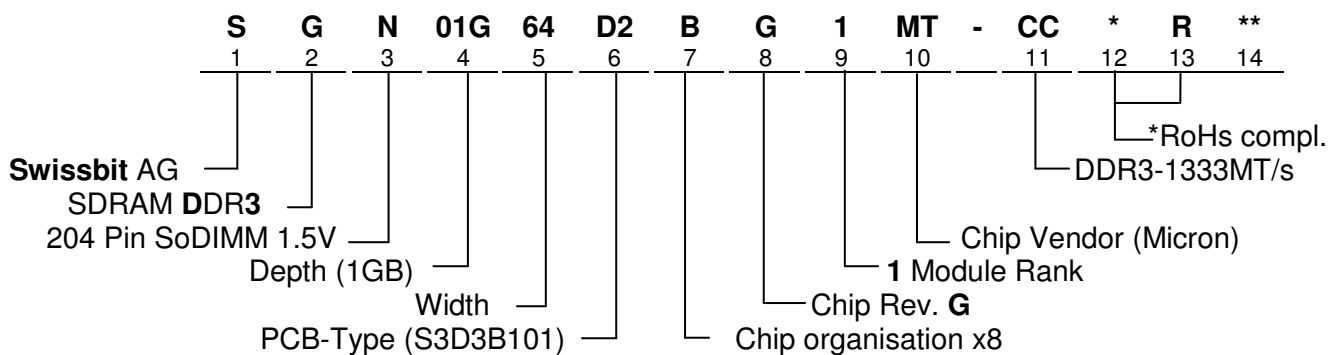
<sup>1</sup> The most significant bit, b7, is sent first.

**SERIAL PRESENCE-DETECT MATRIX**

Byte	Byte Description	10600-999	8500-777
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISION	0x10	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x03	
4	SDRAM DEVICE DENSITY & BANKS	0x02	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x11	
6	BYTE 6 RESERVED	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x01	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x03	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x52	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ( $t_{CK\ MIN}$ )	0x0C	0x0F
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0x7E	0x1E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ( $t_{AA\ MIN}$ )	0x69	
17	MIN WRITE RECOVERY TIME ( $t_{WR\ MIN}$ )	0x78	
18	MIN RAS# TO CAS# DELAY ( $t_{RCD\ MIN}$ )	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ( $t_{RRD\ MIN}$ )	0x30	0x3C
20	MIN ROW PRECHARGE DELAY ( $T_{RP\ MIN}$ )	0x69	
21	UPPER NIBBLE FOR $t_{RAS}$ & $t_{RC}$	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ( $t_{RAS\ MIN}$ )	0x20	0x2C
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY ( $t_{RC\ MIN}$ )	0x89	0x95
24	MIN REFRESH RECOVERY DELAY ( $t_{RFC\ MIN}$ ) LSB	0x70	
25	MIN REFRESH RECOVERY DELAY ( $t_{RFC\ MIN}$ ) MSB	0x03	
26	MIN INTERNAL WRITE TO READ CMD DELAY ( $t_{WTR\ MIN}$ )	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ( $t_{RTP\ MIN}$ )	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ( $t_{FAW\ MIN}$ ) MSB	0x00	0x01
29	MIN FOUR ACTIVE WINDOW DELAY ( $t_{FAW\ MIN}$ ) LSB	0xF0	0x2C
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x82	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x05	

Byte	Byte Description	10600-999	8500-777
32	DDR3-MODULE THERMAL SENSOR	0x80	
33-59	BYTES 32-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x0F	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x01	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x00	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0x34C0	0x9768
128-145	MODULE PART NUMBER	"SGN01G64D2BG1MT-xx"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	0x54	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0xCE	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xff	

**Part Number Code**



\* optional / additional information  
 \*\* T= thermal sensor

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