

# 512MB DDR2 – SDRAM DIMM

240 Pin UDIMM

SEU06464H1CH1MT-25R

512MB PC2-6400 in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency Marking  
 DDR2 800 MT/s CL6 -25  
 DDR2 667 MT/s CL5 -30
  
  - Module Density  
 512MB with 4 dies and 1 rank
  
  - Standard Grade  $(T_A)$  0°C to 70°C  
 $(T_C)$  0°C to 85°C  
 Grade W  $(T_A)$  -40°C to 85°C  
 $(T_C)$  -40°C to 95°C\*
- \* The refresh rate has to be doubled when  $85^\circ\text{C} > T_C > 95^\circ\text{C}$

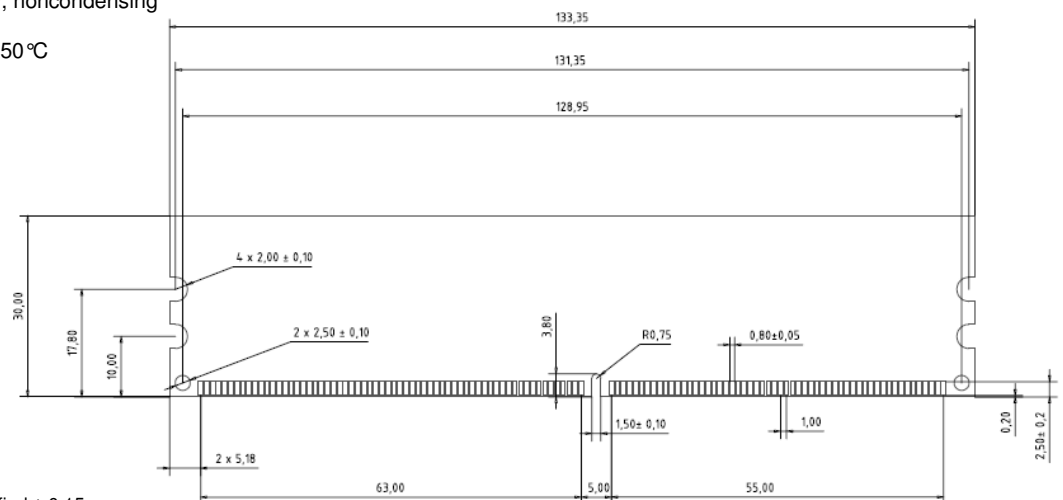
Environmental Requirements:

- Operating temperature (ambient)  
 Standard Grade 0°C to 70°C  
 Grade W -40°C to 85°C\*
- Operating Humidity  
 10% to 90% relative humidity, noncondensing
- Operating Pressure  
 105 to 69 kPa (up to 10000 ft.)
- Storage Temperature  
 -55°C to 100°C
- Storage Humidity  
 5% to 95% relative humidity, noncondensing
- Storage Pressure  
 1682 PSI (up to 5000 ft.) at 50°C

Features:

- 240-pin 64-bit DDR2 Dual-In-Line Double Data Rate Synchronous DRAM Module
- Module organization: single rank 64M x 64
- $V_{DD} = 1.8V \pm 0.1V$ ,  $V_{DDQ} 1.8V \pm 0.1V$
- 1.8V I/O ( SSTL\_18 compatible)
- Serial Presence Detect (SPD) EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC PC2-6400 spec. and JEDEC- Standard MO-237. (see [www.jedec.org](http://www.jedec.org))
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]
  
- **DDR2 - SDRAM component Micron MT47H64M16HR-25 DIE-Rev.H**
- 64Mx16 DDR2 SDRAM in FBGA-84 package
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Eight internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1  $t_{CK}$
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)

Figure: mechanical dimensions<sup>1</sup>



This Swissbit module is an industry standard 240-pin 8-byte DDR2 SDRAM Dual-In-line Memory Module (UDIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL\_18 compatible.

The DDR2 SDRAM module uses the optional serial presence detect (SPD) function implemented via serial EEPROM using the standard I<sup>2</sup>C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

### Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
64M x 64bit	4 x 64M x 16bit (1024Mbit)	13	BA0, BA1, BA2	10	8k	S0#

### Module Dimensions

in mm

133.35 (long) x 30(high) x 4.00 [max] (thickness)

### Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SEU06464H1CH1MT-25[W]R	512 MB	6.4 GB/s	2.5ns/800MT/s	6-6-6
SEU06464H1CH1MT-30[W]R	512 MB	5.3 GB/s	3.0ns/667MT/s	5-5-5

### Pin Name

A0-9, A11 – A13	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0, BA1	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0	Clock Enable
CK0	Clock Inputs, positive line
CK0#	Clock Inputs, negative line
S0#	Chip Select

V <sub>DD</sub>	SDRAM core power supply (1.8V± 0.1V)
V <sub>DDQ</sub>	SDRAM I/O driver power supply (1.8V± 0.1V)
V <sub>REF</sub>	SDRAM I/O reference supply
V <sub>SS</sub>	Ground
V <sub>DDSPD</sub>	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0	On-Die Termination
NC	No Connection

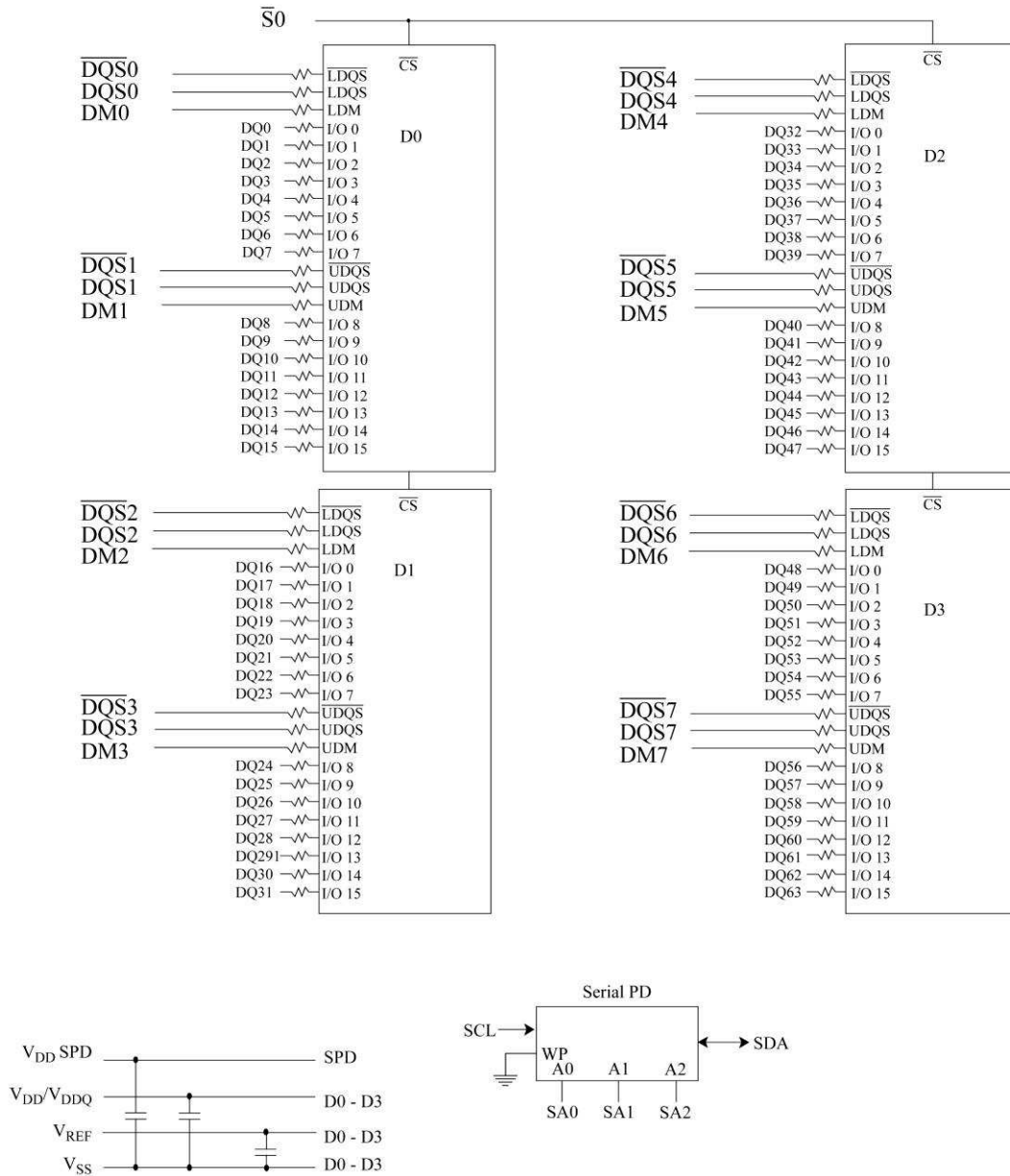
**Pin Configuration**

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	121	V <sub>SS</sub>	61	A4	181	V <sub>DDQ</sub>
2	V <sub>SS</sub>	122	DQ4	62	V <sub>DDQ</sub>	182	A3
3	DQ0	123	DQ5	63	A2	183	A1
4	DQ1	124	V <sub>SS</sub>	64	V <sub>DD</sub>	184	V <sub>DD</sub>
5	V <sub>SS</sub>	125	DM0	65	V <sub>SS</sub>	185	CK0
6	DQS0#	126	NC	66	V <sub>SS</sub>	186	CK0#
7	DQS0	127	V <sub>SS</sub>	67	V <sub>DD</sub>	187	V <sub>DD</sub>
8	V <sub>SS</sub>	128	DQ6	68	NC	188	A0
9	DQ2	129	DQ7	69	V <sub>DD</sub>	189	V <sub>DD</sub>
10	DQ3	130	V <sub>SS</sub>	70	A10/AP	190	BA1
11	V <sub>SS</sub>	131	DQ12	71	BA0	191	V <sub>DDQ</sub>
12	DQ8	132	DQ13	72	V <sub>DD</sub>	192	RAS#
13	DQ9	133	V <sub>SS</sub>	73	WE#	193	S0#
14	V <sub>SS</sub>	134	DM1	74	CAS#	194	V <sub>DDQ</sub>
15	DQS1#	135	NC	75	V <sub>DDQ</sub>	195	ODT0
16	DQS1	136	V <sub>SS</sub>	76	NC(CS1#)	196	A13
17	V <sub>SS</sub>	137	NC(CK1)	77	NC(ODT1)	197	V <sub>DD</sub>
18	NC(RESET#)	138	NC(CK1#)	78	V <sub>DDQ</sub>	198	V <sub>SS</sub>
19	NC	139	V <sub>SS</sub>	79	V <sub>SS</sub>	199	DQ36
20	V <sub>SS</sub>	140	DQ14	80	DQ32	200	DQ37
21	DQ10	141	DQ15	81	DQ33	201	V <sub>SS</sub>
22	DQ11	142	V <sub>SS</sub>	82	V <sub>SS</sub>	202	DM4
23	V <sub>SS</sub>	143	DQ20	83	DQS4#	203	NC
24	DQ16	144	DQ21	84	DQS4	204	V <sub>SS</sub>
25	DQ17	145	V <sub>SS</sub>	85	V <sub>SS</sub>	205	DQ38
26	V <sub>SS</sub>	146	DM2	86	DQ34	206	DQ39
27	DQS2#	147	NC	87	DQ35	207	V <sub>SS</sub>
28	DQS2	148	V <sub>SS</sub>	88	V <sub>SS</sub>	208	DQ44
29	V <sub>SS</sub>	149	DQ22	89	DQ40	209	DQ45
30	DQ18	150	DQ23	90	DQ41	210	V <sub>SS</sub>
31	DQ19	151	V <sub>SS</sub>	91	V <sub>SS</sub>	211	DM5
32	V <sub>SS</sub>	152	DQ28	92	DQS5#	212	NC

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
33	DQ24	153	DQ29	93	DQS5	213	V <sub>SS</sub>
34	DQ25	154	V <sub>SS</sub>	94	V <sub>SS</sub>	214	DQ46
35	V <sub>SS</sub>	155	DM3	95	DQ42	215	DQ47
36	DQS3#	156	NC	96	DQ43	216	V <sub>SS</sub>
37	DQS3	157	V <sub>SS</sub>	97	V <sub>SS</sub>	217	DQ52
38	V <sub>SS</sub>	158	DQ30	98	DQ48	218	DQ53
39	DQ26	159	DQ31	99	DQ49	219	V <sub>SS</sub>
40	DQ27	160	V <sub>SS</sub>	100	V <sub>SS</sub>	220	NC(CK2)
41	V <sub>SS</sub>	161	NC(CB4)	101	SA2	221	NC(CK2#)
42	NC(CB0)	162	NC(CB5)	102	NC(TEST)	222	V <sub>SS</sub>
43	NC(CB1)	163	V <sub>SS</sub>	103	V <sub>SS</sub>	223	DM6
44	V <sub>SS</sub>	164	NC(DM8)	104	DQS6#	224	NC
45	NC(DQS8#)	165	NC	105	DQS6	225	V <sub>SS</sub>
46	NC(DQS8)	166	V <sub>SS</sub>	106	V <sub>SS</sub>	226	DQ54
47	V <sub>SS</sub>	167	NC(CB6)	107	DQ50	227	DQ55
48	NC(CB2)	168	NC(CB7)	108	DQ51	228	V <sub>SS</sub>
49	NC(CB3)	169	V <sub>SS</sub>	109	V <sub>SS</sub>	229	DQ60
50	V <sub>SS</sub>	170	V <sub>DDQ</sub>	110	DQ56	230	DQ61
51	V <sub>DDQ</sub>	171	NC(CKE1)	111	DQ57	231	V <sub>SS</sub>
52	CKE0	172	V <sub>DD</sub>	112	V <sub>SS</sub>	232	DM7
53	V <sub>DD</sub>	173	NC(A15)	113	DQS7#	233	NC
54	BA2	174	NC(A14)	114	DQS7	234	V <sub>SS</sub>
55	NC	175	V <sub>DDQ</sub>	115	V <sub>SS</sub>	235	DQ62
56	V <sub>DDQ</sub>	176	A12	116	DQ58	236	DQ63
57	A11	177	A9	117	DQ59	237	V <sub>SS</sub>
58	A7	178	V <sub>DD</sub>	118	V <sub>SS</sub>	238	V <sub>DDSPD</sub>
59	V <sub>DD</sub>	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

Signals in brackets (...) may be connected at the DIMM socket, but are not used on the DIMM

**FUNCTIONAL BLOCK DIAGRAM 512MB DDR2 SDRAM DIMM,  
1 RANK AND 4 COMPONENTS**



- BA0 - BA2 → BA0-BA2: SDRAMs D0 - D3
- A0 - A15 → A0-A15: SDRAMs D0 - D3
- $\overline{\text{RAS}}$  →  $\overline{\text{RAS}}$ : SDRAMs D0 - D3
- $\overline{\text{CAS}}$  →  $\overline{\text{CAS}}$ : SDRAMs D0 - D3
- CKE0 → CKE: SDRAMs D0 - D3
- $\overline{\text{WE}}$  →  $\overline{\text{WE}}$ : SDRAMs D0 - D3
- ODT0 → ODT: SDRAMs D0 - D3

**Notes:**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/ $\overline{\text{DQS}}$ /ODT/DM/ $\overline{\text{CKE}}$ / $\overline{\text{S}}$  relationships must be maintained as shown.
3. DQ, DM, DQS/ $\overline{\text{DQS}}$  resistors: 22 Ohms  $\pm$  5%.
4. BAx, Ax,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  resistors: 10 Ohms  $\pm$  5%.
5. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document

**MAXIMUM ELECTRICAL DC CHARACTERISTICS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{DD}$	-1.0	2.3	V
I/O Supply Voltage	$V_{DDQ}$	-0.5	2.3	V
$V_{DDL}$ Supply Voltage	$V_{DDL}$	-0.5	2.3	V
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	2.3	V
<b>INPUT LEAKAGE CURRENT</b> Any input $0V \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	$I_I$			$\mu A$
Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
CK, CK#		-20	20	
DM		-5	5	
<b>OUTPUT LEAKAGE CURRENT</b> (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu A$
DQ, DQS, DQS#				
$V_{REF}$ LEAKAGE CURRENT ; $V_{REF}$ is on a valid level	$I_{VREF}$	-16	16	$\mu A$

**DC OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V
I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V
$V_{DDL}$ Supply Voltage	$V_{DDL}$	1.7	1.8	1.9	V
I/O Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.125$	V

**AC INPUT OPERATING CONDITIONS**

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.25$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.25$	V

**CAPACITANCE**

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

**I<sub>DD</sub> Specifications and Conditions**

 (0°C ≤ T<sub>CASE</sub> ≤ + 85°C; V<sub>DDQ</sub> = +1.8V ± 0.1V, V<sub>DD</sub> = +1.8V ± 0.1V)

Parameter & Test Condition	Symbol	max		Unit	
		6400-666	5300-555		
<b>OPERATING CURRENT *) :</b> One device bank Active-Precharge; t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	600	540	mA	
<b>OPERATING CURRENT *) :</b> One device bank; Active-Read-Precharge; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); t <sub>RC</sub> = t <sub>RC</sub> (I <sub>DD</sub> ); t <sub>RAS</sub> = t <sub>RAS</sub> MIN (I <sub>DD</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I <sub>DD4W</sub>	I <sub>DD1</sub>	700	520	mA	
<b>PRECHARGE POWER-DOWN CURRENT:</b> All device banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD2P</sub>	28	28	mA	
<b>PRECHARGE QUIET STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD2Q</sub>	300	260	mA	
<b>PRECHARGE STANDBY CURRENT:</b> All device banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD2N</sub>	320	280	mA	
<b>ACTIVE POWER-DOWN CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V <sub>REF</sub>	I <sub>DD3P</sub>	Fast PDN Exit MR[12] = 0	160	120	mA
		Slow PDN Exit MR[12] = 1	40	40	
<b>ACTIVE STANDBY CURRENT:</b> All device banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD3N</sub>	340	300	mA	
<b>OPERATING READ CURRENT:</b> All device banks open, Continuous burst reads; One module rank active; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>DD</sub> ), t <sub>RAS</sub> = t <sub>RAS</sub> MAX (I <sub>DD</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>DD</sub> ); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD4R</sub>	1280	880	mA	

Parameter & Test Condition	Symbol	max		Unit
		6400-666	5300-555	
<b>OPERATING WRITE CURRENT:</b> All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I <sub>DD</sub> ), AL = 0; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$ , $t_{RP} = t_{RP} (I_{DD})$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD4W</sub>	1260	800	mA
<b>BURST REFRESH CURRENT:</b> $t_{CK} = t_{CK} (I_{DD})$ ; refresh command at every $t_{RFC} (I_{DD})$ interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I <sub>DD5</sub>	1120	1080	mA
<b>SELF REFRESH CURRENT:</b> CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V <sub>REF</sub> ; DQ's are floating at V <sub>REF</sub>	I <sub>DD6</sub>	28	28	mA
<b>OPERATING CURRENT*) :</b> Four device bank interleaving READs, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL (I <sub>DD</sub> ), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$ ; $t_{CK} = t_{CK} (I_{DD})$ , $t_{RC} = t_{RC} (I_{DD})$ , $t_{RRD} = t_{RRD} (I_{DD})$ , $t_{RCD} = t_{RCD} (I_{DD})$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I <sub>DD7</sub>	1760	1400	mA

\*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

#### TIMING VALUES USED FOR I<sub>DD</sub> MEASUREMENT

I <sub>DD</sub> MEASUREMENT CONDITIONS			
SYMBOL	6400-666	5300-555	Unit
CL (I <sub>DD</sub> )	6	5	t <sub>CK</sub>
t <sub>RCD</sub> (I <sub>DD</sub> )	15	15	ns
t <sub>RC</sub> (I <sub>DD</sub> )	60	60	ns
t <sub>RRD</sub> (I <sub>DD</sub> )	7.5	7.5	ns
t <sub>CK</sub> (I <sub>DD</sub> )	2.5	3.0	ns
t <sub>RAS</sub> MIN (I <sub>DD</sub> )	45	40	ns
t <sub>RAS</sub> MAX (I <sub>DD</sub> )	70'000	70'000	ns
t <sub>RP</sub> (I <sub>DD</sub> )	15	15	ns
t <sub>RFC</sub> (I <sub>DD</sub> )	127.5	127.5	ns

**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$ 

AC CHARACTERISTICS			6400-666		5300-555		Unit
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	
Clock cycle time	CL = 6	$t_{\text{CK}}(6)$	2.5	8.0	-	+	ns
	CL = 5	$t_{\text{CK}}(5)$	3.0-	8.0-	3.0	8.0	ns
	CL = 4	$t_{\text{CK}}(4)$	3.75	8.0	3.75	8.0	ns
	CL = 3	$t_{\text{CK}}(3)$	-	-	5.0	8.0	ns
CK high-level width		$t_{\text{CH}}$	0.48	0.52	0.45	0.55	$t_{\text{CK}}$
CK low-level width		$t_{\text{CL}}$	0.48	0.52	0.45	0.55	$t_{\text{CK}}$
Half clock period		$t_{\text{HP}}$	min ( $t_{\text{CH}}, t_{\text{CL}}$ )		min ( $t_{\text{CH}}, t_{\text{CL}}$ )		ps
Access window (output) of DQ <sub>s</sub> from CK/CK#		$t_{\text{AC}}$	-0.40	+0.40	-0.45	+0.45	ns
Data-out high-impedance window from CK/CK#		$t_{\text{HZ}}$		$t_{\text{AC max}}$		+0.45 (= $t_{\text{AC max}}$ )	ns
Data-out low-impedance window from CK/CK#		$t_{\text{LZ}}$	$t_{\text{AC min}}$	$t_{\text{AC max}}$	-0.45 (= $t_{\text{AC min}}$ )	+0.45 (= $t_{\text{AC max}}$ )	ns
DQ and DM input setup time relative to DQS		$t_{\text{DS}}$	0.05		0.10		ns
DQ and DM input hold time relative to DQS		$t_{\text{DH}}$	0.125		0.30		ns
DQ and DM input pulse width ( for each input )		$t_{\text{DIPW}}$	0.35		0.35		$t_{\text{CK}}$
Data hold skew factor		$t_{\text{QHS}}$		0.3		0.34	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		$t_{\text{QH}}$	$t_{\text{HP}} - t_{\text{QHS}}$		$t_{\text{HP}} - t_{\text{QHS}}$		ns
Data valid output window		$t_{\text{DVW}}$	$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		ns
DQS input high pulse width		$t_{\text{DQSH}}$	0.35		0.35		$t_{\text{CK}}$
DQS input low pulse width		$t_{\text{DQSL}}$	0.35		0.35		$t_{\text{CK}}$
DQS falling edge to CK rising - setup time		$t_{\text{DSS}}$	0.2		0.2		$t_{\text{CK}}$
DQS falling edge from CK rising - hold time		$t_{\text{DSH}}$	0.2		0.2		$t_{\text{CK}}$
DQS -DQ skew, DQS to last DQ valid, per group, per access		$t_{\text{DQSQ}}$		0.2		0.24	ns
DQS read preamble		$t_{\text{RPRE}}$	0.9	1.1	0.9	1.1	$t_{\text{CK}}$
DQS read postamble		$t_{\text{RPST}}$	0.4	0.6	0.4	0.6	$t_{\text{CK}}$
DQS write preamble		$t_{\text{WPRE}}$	0.35		0.35		$t_{\text{CK}}$
DQS write preamble setup time		$t_{\text{WPRES}}$	0		0		ns
DQS write postamble		$t_{\text{WPST}}$	0.4	0.6	0.4	0.6	$t_{\text{CK}}$
Positive DQS latching edge to associated clock edge		$t_{\text{DQSS}}$	- 0.25	+ 0.25	- 0.25	+ 0.25	$t_{\text{CK}}$
Write command to first DQS latching transition			WL- $t_{\text{DQSS}}$	WL+ $t_{\text{DQSS}}$	WL- $t_{\text{DQSS}}$	WL+ $t_{\text{DQSS}}$	$t_{\text{CK}}$
Address and control input pulse width ( for each input )		$t_{\text{IPW}}$	0.6		0.6		$t_{\text{CK}}$
Address and control input setup time		$t_{\text{ISa}}$	0.175		0.4		ns

**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**

 (0°C ≤ T<sub>CASE</sub> ≤ +85°C; V<sub>DDQ</sub> = +1.8V ± 0.1V, V<sub>DD</sub> = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-666		5300-555		Unit
PARAMETER	SYMBOL	Min	Max	MIN	MAX	
Address and control input hold time	t <sub>IH</sub>	0.25		0.4		ns
CAS# to CAS# command delay	t <sub>CCD</sub>	2		2		t <sub>CK</sub>
ACTIVE to ACTIVE (same bank) command period	t <sub>RC</sub>	60		55		ns
ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	7.5		7.5		ns
ACTIVE to READ or WRITE delay	t <sub>RCD</sub>	15		15		ns
Four bank Activate period	t <sub>FAW</sub>	37.5		37.5		ns
ACTIVE to PRECHARGE command	t <sub>RAS</sub>	45	70'000	40	70'000	ns
Internal READ to precharge command delay	t <sub>RTP</sub>	7.5		7.5		ns
Write recovery time	t <sub>WR</sub>	15		15		ns
Auto precharge write recovery + precharge time	t <sub>DAL</sub>	t <sub>WR</sub> + t <sub>RP</sub>		t <sub>WR</sub> + t <sub>RP</sub>		ns
Internal WRITE to READ command delay	t <sub>WTR</sub>	7.5		7.5		ns
PRECHARGE command period	t <sub>RP</sub>	15		15		ns
PRECHARGE ALL command period	t <sub>RPA</sub>	t <sub>RP</sub> + t <sub>CK</sub>		t <sub>RP</sub> + t <sub>CK</sub>		ns
LOAD MODE command cycle time	t <sub>MRD</sub>	2		2		t <sub>CK</sub>
CKE low to CK, CK# uncertainty	t <sub>DELAY</sub>	t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>IS</sub> + t <sub>CK</sub> + t <sub>IH</sub>		t <sub>CK</sub>
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t <sub>RFC</sub>	127.5	70'000	127.5	70'000	ns
Average periodic refresh interval 0 °C ≤ T <sub>CASE</sub> ≤ 85 °C	t <sub>REFI</sub>		7.8		7.8	μs
85 °C < T <sub>CASE</sub> ≤ 95 °C	t <sub>REFI (IT)</sub>		3.9		3.9	
Exit SELF REFRESH to non-READ command	t <sub>XSNR</sub>	t <sub>RFC(min)</sub> + 10		t <sub>RFC(min)</sub> + 10		ns
Exit SELF REFRESH to READ command	t <sub>XSRD</sub>	200		200		t <sub>CK</sub>
Exit SELF REFRESH timing reference	t <sub>ISXR</sub>	t <sub>IS</sub>		t <sub>IS</sub>		ps
ODT turn-on delay	t <sub>AOND</sub>	2	2	2	2	t <sub>CK</sub>
ODT turn-on	t <sub>AON</sub>	t <sub>AC(min)</sub>	t <sub>AC(max)</sub> + 1,000	t <sub>AC(min)</sub>	t <sub>AC(max)</sub> + 1,000	ps
ODT turn-off delay	t <sub>AOFD</sub>	2.5	2.5	2.5	2.5	t <sub>CK</sub>
ODT turn-off	t <sub>AOF</sub>	t <sub>AC(min)</sub>	t <sub>AC(max)</sub> + 600	t <sub>AC(min)</sub>	t <sub>AC(max)</sub> + 600	ps
ODT turn-on (power-down mode)	t <sub>AONPD</sub>	t <sub>AC(min)</sub> + 2,000	2 x t <sub>CK</sub> + t <sub>AC(max)</sub> + 1,000	t <sub>AC(min)</sub> + 2,000	2 x t <sub>CK</sub> + t <sub>AC(max)</sub> + 1,000	ps
ODT turn-off (power-down mode)	t <sub>AOFPD</sub>	t <sub>AC(min)</sub> + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC(max)</sub> + 1,000	t <sub>AC(min)</sub> + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC(max)</sub> + 1,000	ps
ODT to power-down entry latency	t <sub>ANPD</sub>	3		3		t <sub>CK</sub>

**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)**(0°C ≤ T<sub>CASE</sub> ≤ +85°C; V<sub>DDQ</sub> = +1.8V ± 0.1V, V<sub>DD</sub> = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-666		5300-555		Unit
PARAMETER	SYMBOL	Min	Max	MIN	MAX	
ODT power-down exit latency	t <sub>AXPD</sub>	8		8		t <sub>CK</sub>
ODT enable from MRS command	T <sub>MOD</sub>	12		12		ns
Exit active power-down to READ command, MR [bit 12 = 0]	t <sub>XARD</sub>	2		2		t <sub>CK</sub>
Exit active power-down to READ command, MR [bit 12 = 1]	t <sub>XARDS</sub>	8 – AL		7 – AL		t <sub>CK</sub>
Exit precharge power-down to any non-READ command	t <sub>XP</sub>	2		2		t <sub>CK</sub>
CKE minimum high/low time	t <sub>CKE</sub>	3		3		t <sub>CK</sub>

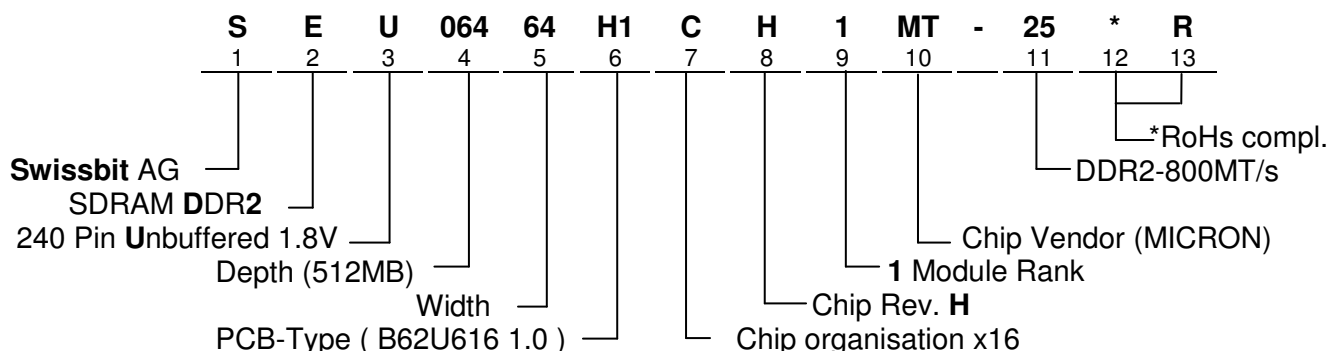
**SERIAL PRESENCE-DETECT MATRIX**

BYTE	DESCRIPTION	6400-666	5300-555
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x08	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0D	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A	
5	DIMM HIGHT AND MODULE RANKS	0x60	
6	MODULE DATA WIDTH	0x40	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V <sub>DDQ</sub> )	0x05	
9	SDRAM CYCLE TIME, (t <sub>CK</sub> ) [max CL] CAS LATENCY = 6 (6400); CL = 5 (5300)	0x25	0x30
10	SDRAM ACCESS FROM CLOCK, (t <sub>AC</sub> ) [max CL] CAS LATENCY = 6 (6400); CL = 5 (5300)	0x40	0x45
11	MODULE CONFIGURATION TYPE	0x00	
12	REFRESH RATE / TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x10	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00	
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00	
16	BURST LENGTHS SUPPORTED	0x0C	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08	
18	CAS LATENCIES SUPPORTED	0x70	0x38
19	MODULE THICKNESS	0x01	
20	DDR2 DIMM TYPE	0x02	
21	SDRAM MODULE ATTRIBUTES	0x00	
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x03	
23	SDRAM CYCLE TIME, (t <sub>CK</sub> ) [max CL – 1] CAS LATENCY = 5 (6400); CL = 4 (5300)	0x30	0x3D
24	SDRAM ACCESS FROM CK, (t <sub>AC</sub> ) [max CL – 1] CAS LATENCY = 5 (6400); CL = 4 (5300)	0x40	0x45
25	SDRAM CYCLE TIME, (t <sub>CK</sub> ) [max CL – 2] CAS LATENCY = 4 (6400); CL = 3 (5300)	0x3D	0x50
26	SDRAM ACCESS FROM CK, (t <sub>AC</sub> ) [max CL – 2] CAS LATENCY = 4 (6400); CL = 3 (5300)	0x40	0x45
27	MINIMUM ROW PRECHARGE TIME, (t <sub>RP</sub> )	0x3C	
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t <sub>RRD</sub> )	0x28	
29	MINIMUM RAS# TO CAS# DELAY, (t <sub>RCD</sub> )	0x3C	
30	MINIMUM RAS# PULSE WIDTH, (t <sub>RAS</sub> )	0x2D	
31	MODULE BANK DENSITY	0x80	

**SERIAL PRESENCE-DETECT MATRIX (continued)**

BYTE	DESCRIPTION	6400-666	5300-555
32	ADDRESS AND COMMAND SETUP TIME, (t <sub>ISb</sub> )	0x17	0x20
33	ADDRESS AND COMMAND HOLD TIME, (t <sub>IHb</sub> )	0x25	0x27
34	DATA / DATA MASK INPUT SETUP TIME, (t <sub>DSb</sub> )	0x05	0x10
35	DATA / DATA MASK INPUT HOLD TIME, (t <sub>DHb</sub> )	0x12	0x17
36	WRITE RECOVERY TIME, (t <sub>WR</sub> )	0x3C	
37	WRITE to READ Command Delay, (t <sub>WTR</sub> )	0x1E	
38	READ to PRECHARGE Command Delay, (t <sub>RTP</sub> )	0x1E	
39	Mem Analysis Probe	0x00	
40	Extension for Bytes 41 and 42	0x06	
41	MIN ACTIVE AUTO REFRESH TIME, (t <sub>RC</sub> )	0x3C	
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t <sub>RFC</sub> )	0x7F	
43	SDRAM DEVICE MAX CYCLE TIME, (t <sub>CKMAX</sub> )	0x80	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t <sub>DQSQ</sub> )	0x14	0x18
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t <sub>QHS</sub> )	0x1E	0x22
46	PLL Relock Time	0x00	
47-61	Optional Features, not supported	0x00	
62	SPD REVISION	0x13	
63	CHECKSUM FOR BYTES 0-62	0x58	0x7D
64-66	MANUFACTURER'S JEDEC ID CODE	0x7F	
67	MANUFACTURER'S JEDEC ID CODE (continued)	0xDA	
68-71	RESERVED	0x00	
72	MANUFACTURING LOCATION	0x01 (Switzerland)   0x02 (Germany)   0x03 (USA)	
73-90	MODULE PART NUMBER (ASCII)	"SEU06464H1CH1MT-xx"	
91	PCB IDENTIFICATION CODE	x	
92	IDENTIFICATION CODE (continued)	x	
93	YEAR OF MANUFACTURE IN BCD	x	
94	WEEK OF MANUFACTURE IN BCD	x	
95-98	MODULE SERIAL NUMBER	x	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	x	
128-255	Open for customer use	0xFF	

**Part Number Code**



\* optional / additional information

## Locations

**Swissbit AG**

Industriestrasse 4 – 8  
CH – 9552 Bronschhofen  
Switzerland  
Phone: +41 (0)71 913 03 03  
Fax: +41 (0)71 913 03 15

---

**Swissbit Germany GmbH**

Wolfener Strasse 36  
D – 12681 Berlin  
Germany  
Phone: +49 (0)30 93 69 54 – 0  
Fax: +49 (0)30 93 69 54 – 55

---

**Swissbit NA, Inc.**

14 Willett Avenue, Suite 301A  
Port Chester, NY 10573  
USA  
Phone: +1 914 935 1400  
Fax: +1 914 935 9865

---

**Swissbit NA, Inc.**

3913 Todd Lane, Suite – 307  
Austin, TX 78744  
USA  
Phone: +1 512 302 9001  
Fax: +1 512 302 4808

---

**Swissbit Japan, Inc.**

3F Core Koenji,  
2-1-24 Koenji-Kita, Suginami-Ku,  
Tokyo 166-0002  
Japan  
Phone: +81 3 5356 3511  
Fax: +81 3 5356 3512