

1GB DDR2 – SDRAM registered DIMM

240 Pin RDIMM

SEP01G72J2BE1SA-25R

1GB PC2-6400 in FBGA Technique

RoHS compliant

Options:

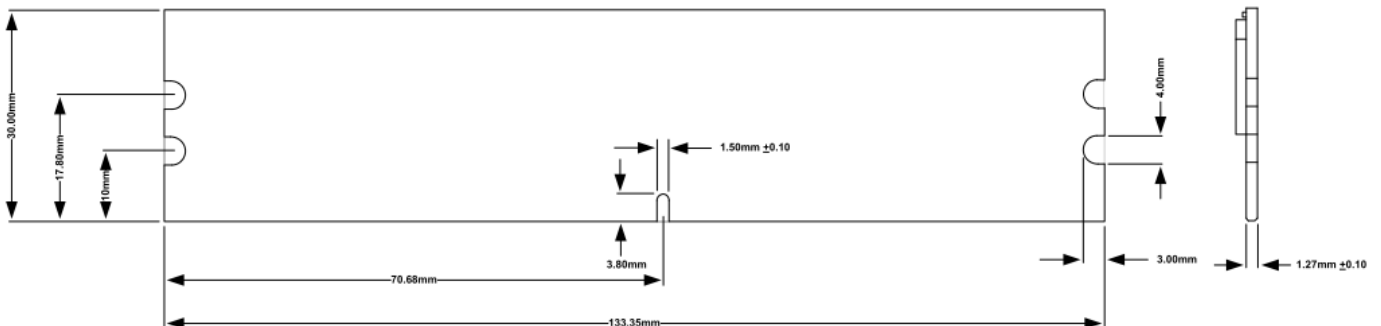
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|-------------------------------|-------------------|-------------|
| ▪ Frequency / Latency | | Marking |
| DDR2 800MHZ CL6 | | -25 |
| 800MHZ CL5 | | -2A |
| 667MHz CL5 | | -30 |
| 533MHz CL4 | | -37 |
| ▪ Module densities | | |
| 1024MB with 9 dies and 1 rank | | |
| ▪ Standard Grade | (T _C) | 0°C to 85°C |
| | (T _A) | 0°C to 70°C |

Environmental Requirements:

- Operating temperature (T_C)
Standard Grade 0°C to 85°C
- Operating Humidity
10% to 90% relative humidity, noncondensing
- Operating Pressure
105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
-55°C to 100°C
- Storage Humidity
5% to 95% relative humidity, noncondensing
- Storage Pressure
1682 PSI (up to 5000 ft.) at 50°C

Features:

- 240-pin 72-bit Dual-In-Line Double Data Rate synchronous DRAM Module for server applications
- DDR2 - SDRAM component base Samsung K4T1G084QE die rev. E
- V_{DD} = 1.8V ±0.2V, V_{DDQ} 1.8V ±0.2V
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- 1.8V I/O (SSTL_18 compatible)
- Serial Presence Detect with EEPROM
- Four bit prefetch architecture
- Parity support
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Phase-lock loop (PLL) clock driver to reduce loading
- Supports ECC error detection and correction
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)
- Gold-contact pad
- This module family is fully pin and functional compatible to JEDEC. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]



mechanical dimensions¹

¹ if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 240-pin 8-byte DDR2 SDRAM Dual-In-line Memory Module (DIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured quad-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.

The DDR2 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I²C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Select	Col. Addr.	Refresh	Module Bank Select
128M x 72bit	9 x 128M x 8bit (1Gbit)	14	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions

in mm

133.33 (long) x 30(high) x 4 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SEP01G72J2BE1SA-25R	1024 MB	6.4 GB/s	2.5ns/800MT/s	6400-666
SEP01G72J2BE1SA-2AR	1024 MB	6.4 GB/s	2.0ns/800MT/s	6400-555
SEP01G72J2BE1SA-30R	1024 MB	5.3 GB/s	3.0ns/667MT/s	5300-555
SEP01G72J2BE1SA-37R	1024 MB	4.2 GB/s	3.7ns/533MT/s	4200-444

Pin Name

A0 - A13	Address Inputs
BA0, BA1	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM8	Input Data Mask
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
CK0	Clock Input, positive line
CK0#	Clock Input, negative line
DQS0 – DQS17	Data Strobe, positive line
DQS0# - DQS17#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
CS0#, CS1#	Chip Select

Reset#	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQs are High-Z.
PAR_IN	Parity bit for the address and control bus.
ERR_OUT	Parity error found on the address and control bus.
CB0 – CB7	Check Bits
V _{DD} /V _{DDQ}	Supply Voltage (1.8V± 0.1V/41)
V _{REF}	Input / Output Reference
V _{SS}	Ground
V _{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

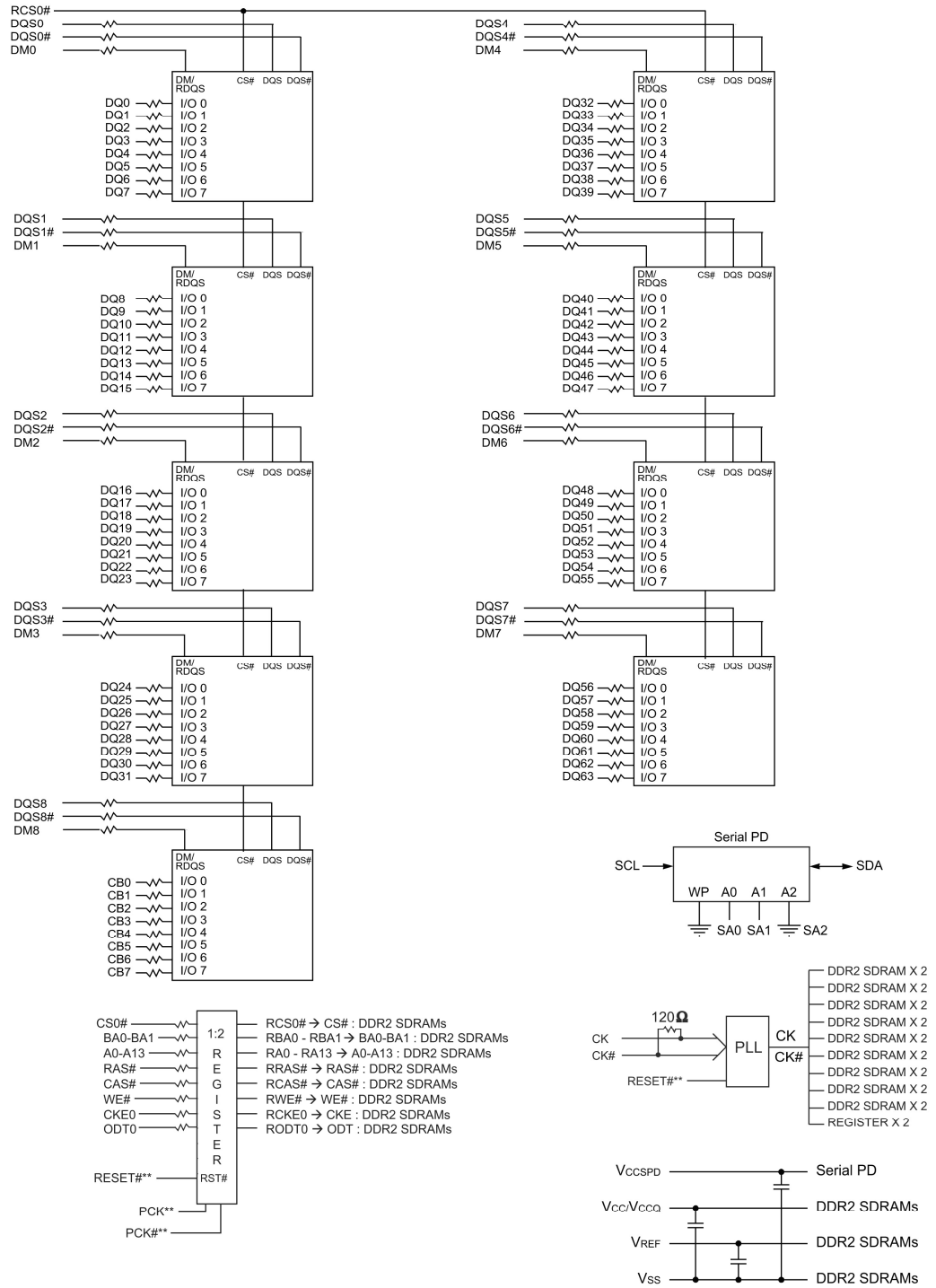
Pin Configuration

PIN #	Front Side	PIN #	Front Side	PIN #	Back Side	PIN #	Back Side
1	VREF	61	A4	121	Vss	181	VDDQ
2	Vss	62	VDDQ	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	VDD	124	Vss	184	VDD
5	Vss	65	Vss	125	DM0 DQS9	185	CK0
6	DQS0#	66	Vss	126	NC DQS9#	186	CK0#
7	DQS0	67	VDD	127	Vss	187	VDD
8	Vss	68	NC PAR_IN	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	VDDQ
12	DQ8	72	VDDQ	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	CS0#
14	VSS	74	CAS#	134	DM1 DQS10	194	VDDQ
15	DQS1#	75	VDDQ	135	NC DQS10#	195	ODT0
16	DQS1	76	CS1#	136	Vss	196	A13
17	Vss	77	ODT1	137	NC	197	VDD
18	RESET#	78	VDDQ	138	NC	198	Vss
19	NC	79	Vss	139	Vss	199	DQ36
20	Vss	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	Vss	142	Vss	202	DM4 DQS13
23	Vss	83	DQS4#	143	DQ20	203	NC DQS13#
24	DQ16	84	DQS4	144	DQ21	204	Vss
25	DQ17	85	Vss	145	Vss	205	DQ38
26	Vss	86	DQ34	146	DM2 DQS11	206	DQ39
27	DQS2#	87	DQ35	147	NC DQS11#	207	Vss
28	DQS2	88	Vss	148	Vss	208	DQ44
29	Vss	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	Vss

PIN #	Front Side	PIN #	Front Side	PIN #	Back Side	PIN #	Back Side
31	DQ19	91	Vss	151	Vss	211	DM5 DQS14
32	Vss	92	DQS5#	152	DQ28	212	NC DQS14#
33	DQ24	93	DQS5	153	DQ29	213	Vss
34	DQ25	94	Vss	154	Vss	214	DQ46
35	Vss	95	DQ42	155	DM3 DQS12	215	DQ47
36	DQS3#	96	DQ43	156	NC DQS12#	216	Vss
37	DQS3	97	Vss	157	Vss	217	DQ52
38	Vss	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	Vss
40	DQ27	100	Vss	160	Vss	220	NC
41	Vss	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	Vss
43	CB1	103	Vss	163	Vss	223	DM6 DQS15
44	Vss	104	DQS6#	164	DM8 DQS17	224	NC DQS15#
45	DQS8#	105	DQS6	165	NC DQS17#	225	Vss
46	DQS8	106	Vss	166	Vss	226	DQ54
47	Vss	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	Vss
49	CB3	109	Vss	169	Vss	229	DQ60
50	Vss	110	DQ56	170	VDD	230	DQ61
51	VDD	111	DQ57	171	CKE1	231	Vss
52	CKE0	112	Vss	172	VDD	232	DM7 DQS16
53	VDD	113	DQS7#	173	NC	233	NC DQS16#
54	BA2	114	DQS7	174	NC	234	Vss
55	NC ERR_OUT	115	Vss	175	VDD	235	DQ62
56	VDDQ	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	Vss
58	A7	118	Vss	178	VDD	238	VDDSPD
59	VDD	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

**FUNCTIONAL BLOCK DIAGRAM 1024MB DDR2 ECC Registered DIMM,
1 RANK AND 9 COMPONENTS**

FUNCTIONAL BLOCK DIAGRAM



** RESET#, PCK and PCK# connect to both Registers. Other signals connect to one of two Registers.
Note: All resistor values are 22 ohms ±5% unless otherwise specified.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-1.0	2.3	V
I/O Supply Voltage	V_{DDQ}	-0.5	2.3	V
V_{DDL} Supply Voltage	V_{DDL}	-0.5	2.3	V
Voltage on any pin relative to V_{SS}	V_{in}, V_{out}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	I_I			μA
Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
CK, CK#		-20	20	
DM		-5	5	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	I_{OZ}	-5	5	μA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-16	16	μA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V
V_{DDL} Supply Voltage	V_{DDL}	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	V_{TT}	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.125$	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.25$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.25$	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

 (0°C ≤ T_{CASE} ≤ + 85°C V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition	Symbol	max.				Unit
		6400-555	6400-666	5300-555	4200-444	
OPERATING CURRENT *) : One device bank Active-Precharge; t _{RC} = t _{RC} (I _{DD}); t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	468		450	450	mA
OPERATING CURRENT*) : One device bank; Active-Read-Precharge; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RAS} = t _{RAS} MIN (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I _{DD4W}	I _{DD1}	522		495	495	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2P}	90		90	90	mA
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2Q}	207		207	207	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD2N}	252		243	243	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD3P}	Fast PDN Exit MR[12] = 0	234	225	225	mA
		Slow PDN Exit MR[12] = 1	135	135	135	
ACTIVE STANDBY CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD3N}	333		315	315	mA

Parameter & Test Condition	Symbol	Max.				Unit
		6400-555	6400-666	5300-555	4200-444	
OPERATING READ CURRENT*) : All device banks open, Continuous burst reads; One module rank active; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4R}	810		720	720	mA
OPERATING WRITE CURRENT*) : All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4W}	648		585	585	mA
BURST REFRESH CURRENT: t _{CK} = t _{CK} (I _{DD}); refresh command at every t _{RFC} (I _{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD5}	1080		1035	1035	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V _{REF} ; DQ's are floating at V _{REF}	I _{DD6}	90		90	90	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = t _{RCD} (I _{DD}) - 1 x t _{CK} (I _{DD}); t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RRD} = t _{RRD} (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I _{DD7}	1530		1395	1395	mA

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I _{DD} MEASUREMENT CONDITIONS					
SYMBOL	6400-555	6400-666	5300-555	4200-444	Unit
CL (I _{DD})	5	6	5	4	t _{CK}
t _{RCD} (I _{DD})	12.5	15	15	15	ns
t _{RC} (I _{DD})	57.5	60	60	60	ns
t _{RRD} (I _{DD})	7.5	7.5	7.5	7.5	ns
t _{CK} (I _{DD})	2.5	2.5	3.0	3.7	ns
t _{RAS} MIN (I _{DD})	45	45	45	45	ns
t _{RAS} MAX (I _{DD})	70,000	70,000	70,000	70,000	ns
t _{RP} (I _{DD})	12.5	15	15	15	ns
t _{RFC} (I _{DD})	105	105	105	105	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS			6400-555		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock cycle time	CL = 6	$t_{\text{CK}}(6)$	-	-	2.5	8.0	-	+	-	-	ps
	CL = 5	$t_{\text{CK}}(5)$	2.5	8.0	3.0-	8.0-	3.0	8.0	-	-	ps
	CL = 4	$t_{\text{CK}}(4)$	3.75	8.0	3.75	8.0	3.75	8.0	3.75	8.0	ps
	CL = 3	$t_{\text{CK}}(3)$	5.0	8.0	-	-	5.0	8.0	5.0	8.0	ps
CK high-level width	t_{CH}	0.48	0.52	0.48	0.52	0.45	0.55	0.45	0.55	t_{CK}	
CK low-level width	t_{CL}	0.48	0.52	0.48	0.52	0.45	0.55	0.45	0.55	t_{CK}	
Half clock period	t_{HP}	min ($t_{\text{CH}}, t_{\text{CL}}$)		min ($t_{\text{CH}}, t_{\text{CL}}$)		min ($t_{\text{CH}}, t_{\text{CL}}$)		min ($t_{\text{CH}}, t_{\text{CL}}$)			ps
Access window (output) of DQs from CK/CK#	t_{AC}	-0.40	+0.40	-0.40	+0.40	-0.45	+0.45	-0.50	+0.50	ns	
Data-out high-impedance window from CK/CK#	t_{HZ}		$t_{\text{AC max}}$		$t_{\text{AC max}}$		+0.45 (= $t_{\text{AC max}}$)		+0.50 (= $t_{\text{AC max}}$)	ns	
Data-out low-impedance window from CK/CK#	t_{LZ}	$t_{\text{AC min}}$	$t_{\text{AC max}}$	$t_{\text{AC min}}$	$t_{\text{AC max}}$	-0.45 (= $t_{\text{AC min}}$)	+0.45 (= $t_{\text{AC max}}$)	-0.50 (= $t_{\text{AC min}}$)	+0.50 (= $t_{\text{AC max}}$)	ns	
DQ and DM input setup time relative to DQS	t_{DS}	0.05		0.05		0.10		0.10		ns	
DQ and DM input hold time relative to DQS	t_{DH}	0.125		0.125		0.30		0.35		ns	
DQ and DM input pulse width (for each input)	t_{DIPW}	0.35		0.35		0.35		0.35		t_{CK}	
Data hold skew factor	t_{QHS}		0.3		0.3		0.34		0.4	ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	$t_{\text{HP}} - t_{\text{QHS}}$		$t_{\text{HP}} - t_{\text{QHS}}$		$t_{\text{HP}} - t_{\text{QHS}}$		$t_{\text{HP}} - t_{\text{QHS}}$		ns	
Data valid output window	t_{DVW}	$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		$t_{\text{QH}} - t_{\text{DQSQ}}$		ns	
DQS input high pulse width	t_{DQSH}	0.35		0.35		0.35		0.35		t_{CK}	
DQS input low pulse width	t_{DQSL}	0.35		0.35		0.35		0.35		t_{CK}	
DQS falling edge to CK rising - setup time	t_{DSS}	0.2		0.2		0.2		0.2		t_{CK}	
DQS falling edge from CK rising - hold time	t_{DSH}	0.2		0.2		0.2		0.2		t_{CK}	
DQS -DQ skew, DQS to last DQ valid, per group, per access	t_{DQSQ}		0.2		0.2		0.24		0.30	ns	
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS write preamble	t_{WPRES}	0.35		0.35		0.35		0.25		t_{CK}	
DQS write preamble setup time	t_{WPRES}	0		0		0		0		ns	
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Positive DQS latching edge to associated clock edge	t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}	
Write command to first DQS latching transition		WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	t_{CK}	
Address and control input pulse width (for each input)	t_{IPW}	0.6		0.6		0.6		0.6		t_{CK}	
Address and control input setup time	t_{ISa}	0.175		0.175		0.4		0.5		ns	

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS		6400-555		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	Min	Max	Min	Max	MIN	MAX	MIN	MAX	
Address and control input hold time	t_{IH}	0.25		0.25		0.4		0.5		ns
CAS# to CAS# command delay	t_{CCD}	2		2		2		2		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	57.5		60		55		55		ns
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	t_{RRD}	7.5		7.5		7.5		7.5		ns
ACTIVE to READ or WRITE delay	t_{RCD}	12.5		15		15		15		ns
Four bank Activate period	t_{FAW}	37.5		37.5		37.5		37.5		ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	40	70,000	40	70,000	ns
Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		7.5		ns
Write recovery time	t_{WR}	15		15		15		15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{\text{WR}} + t_{\text{RP}}$		$t_{\text{WR}} + t_{\text{RP}}$		$t_{\text{WR}} + t_{\text{RP}}$		$t_{\text{WR}} + t_{\text{RP}}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		7.5		7.5		ns
PRECHARGE command period	t_{RP}	12.5		15		15		15		ns
PRECHARGE ALL command period	t_{RPA}	$t_{\text{RP}} + t_{\text{CK}}$		$t_{\text{RP}} + t_{\text{CK}}$		$t_{\text{RP}} + t_{\text{CK}}$		$t_{\text{RP}} + t_{\text{CK}}$		ns
LOAD MODE command cycle time	t_{MRD}	2		2		2		2		t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		$t_{\text{IS}} + t_{\text{CK}} + t_{\text{IH}}$		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	105	70,000	105	70,000	105	70,000	105	70,000	ns
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8		7.8	μs
Exit SELF REFRESH to non-READ command	t_{XSNR}	$t_{\text{RFC}}(\text{min}) + 10$		$t_{\text{RFC}}(\text{min}) + 10$		$t_{\text{RFC}}(\text{min}) + 10$		$t_{\text{RFC}}(\text{min}) + 10$		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		200		t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}		t_{IS}		t_{IS}		t_{IS}		ps
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	$t_{\text{AC}}(\text{min})$	$t_{\text{AC}}(\text{max}) + 600$	ps
ODT turn-on (power-down mode)	t_{AONPD}	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	$t_{\text{AC}}(\text{min}) + 2,000$	$2.5 \times t_{\text{CK}} + t_{\text{AC}}(\text{max}) + 1,000$	ps
ODT to power-down entry latency	t_{ANPD}	3		3		3		3		t_{CK}

**DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED
AC OPERATING CONDITIONS (Continued)**
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.8\text{V} \pm 0.1\text{V}, V_{\text{DD}} = +1.8\text{V} \pm 0.1\text{V})$

AC CHARACTERISTICS		6400-555		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	MIN	MAX	Min	Max	MIN	MAX	MIN	MAX	
ODT power-down exit latency	t_{AXPD}	8		8		8		8		t_{CK}
ODT enable from MRS command	T_{MOD}	12		12		12		12		ns
Exit active power-down to READ command, MR [bit 12 = 0]	t_{XARD}	2		2		2		2		t_{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t_{XARDS}	8 – AL		8 – AL		7 – AL		6 – AL		t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2		2		2		2		t_{CK}
CKE minimum high/low time	t_{CKE}	3		3		3		3		t_{CK}

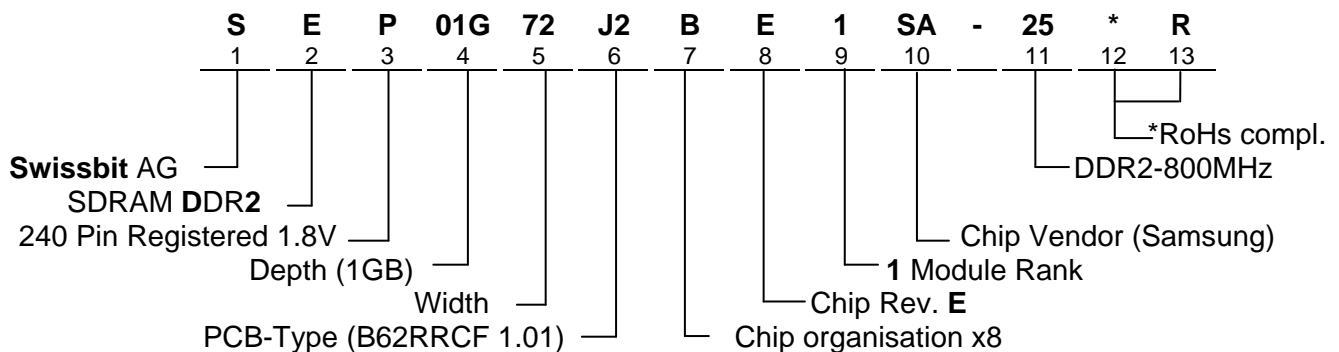
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	6400-555	6400-666	5300-555	4200-444
0	NUMBER OF SPD BYTES USED	0x80			
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08			
2	FUNDAMENTAL MEMORY TYPE	0x08			
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0E			
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A			
5	DIMM HIGHT AND MODULE RANKS	0x60			
6	MODULE DATA WIDTH	0x48			
7	MODULE DATA WIDTH (continued)	0x00			
8	MODULE VOLTAGE INTERFACE LEVELS (V _{DDQ})	0x05			
9	SDRAM CYCLE TIME, (t _{CK}) [max CL] CAS LATENCY = 5 (5300), CL = 4 (4200)	0x25		0x30	0x3D
10	SDRAM ACCESS FROM CLOCK, (t _{AC}) [max CL] CAS LATENCY = 5 (5300); CL = 4 (4200)	0x40		0x45	0x50
11	MODULE CONFIGURATION TYPE	0x06			
12	REFRESH RATE / TYPE	0x82			
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08			
14	ERROR- CHECKING SDRAM DATA WIDTH	0x08			
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00			
16	BURST LENGTHS SUPPORTED	0x0C			
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08			
18	CAS LATENCIES SUPPORTED	0x30	0x70	0x38	0x18
19	MODULE THICKNESS	0x01			
20	DDR2 DIMM TYPE	0x01			
21	SDRAM MODULE ATTRIBUTES	0x04			
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x07			0x01
23	SDRAM CYCLE TIME, (t _{CK}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x3D	0x30	0x3D	0x50
24	SDRAM ACCESS FROM CK, (t _{AC}) [max CL – 1] CAS LATENCY = 4 (5300), CL = 3 (4200)	0x45		0x50	0x60
25	SDRAM CYCLE TIME, (t _{CK}) [max CL – 2] CAS LATENCY = 3 (5300)	0x00	0x3D	0x50	0x00
26	SDRAM ACCESS FROM CK, (t _{AC}) [max CL – 2] CAS LATENCY = 3 (5300)	0x00	0x50	0x60	0x00
27	MINIMUM ROW PRECHARGE TIME, (t _{RP})	0x32	0x3C		
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t _{RRD})	0x1E			
29	MINIMUM RAS# TO CAS# DELAY, (t _{RCD})	0x32	0x3C		
30	MINIMUM RAS# PULSE WIDTH, (t _{RAS})	0x2D			
31	MODULE BANK DENSITY	0x01			

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	6400-555	6400-666	5300-555	4200-444
32	ADDRESS AND COMMAND SETUP TIME, (t _{ISb})	0x17		0x20	0x25
33	ADDRESS AND COMMAND HOLD TIME, (t _{IHb})	0x25		0x27	0x37
34	DATA / DATA MASK INPUT SETUP TIME, (t _{DSb})	0x05		0x10	
35	DATA / DATA MASK INPUT HOLD TIME, (t _{DHb})	0x12		0x17	0x22
36	WRITE RECOVERY TIME, (t _{WR})	0x3C			
37	WRITE to READ Command Delay, (t _{WTR})	0x1E			
38	READ to PRECHARGE Command Delay, (t _{RTP})	0x1E			
39	Mem Analysis Probe	0x00			
40	Extension for Bytes 41 and 42	0x36	0x06		
41	MIN ACTIVE AUTO REFRESH TIME, (t _{RC})	0x39	0x3C		
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t _{RFC})	0x7F			
43	SDRAM DEVICE MAX CYCLE TIME, (t _{CKMAX})	0x80			
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t _{DQSQ})	0x14		0x18	0x1E
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t _{QHS})	0x1E		0x22	0x28
46	PLL Relock Time	0x00			
47-61	Optional Features, not supported	0x00			
62	SPD REVISION	0x12			
63	CHECKSUM FOR BYTES 0-62	0x52	0xF9	0x2F	0xC0
64-66	MANUFACTURER'S JEDEC ID CODE	0x7F			
67	MANUFACTURER'S JEDEC ID CODE (continued)	0xDA			
68-71	RESERVED	0x00			
72	MANUFACTURING LOCATION	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)			
73-90	MODULE PART NUMBER (ASCII)	"SEP01G72J2BE1SA-XX"			
91	PCB IDENTIFICATION CODE	0x52			
92	IDENTIFICATION CODE (continued)	0x00			
93	YEAR OF MANUFACTURE IN BCD	x			
94	WEEK OF MANUFACTURE IN BCD	x			
95-98	MODULE SERIAL NUMBER	x			
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00			
128-255	Open for customer use	0xff			

Part Number Code



* optional / additional information

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