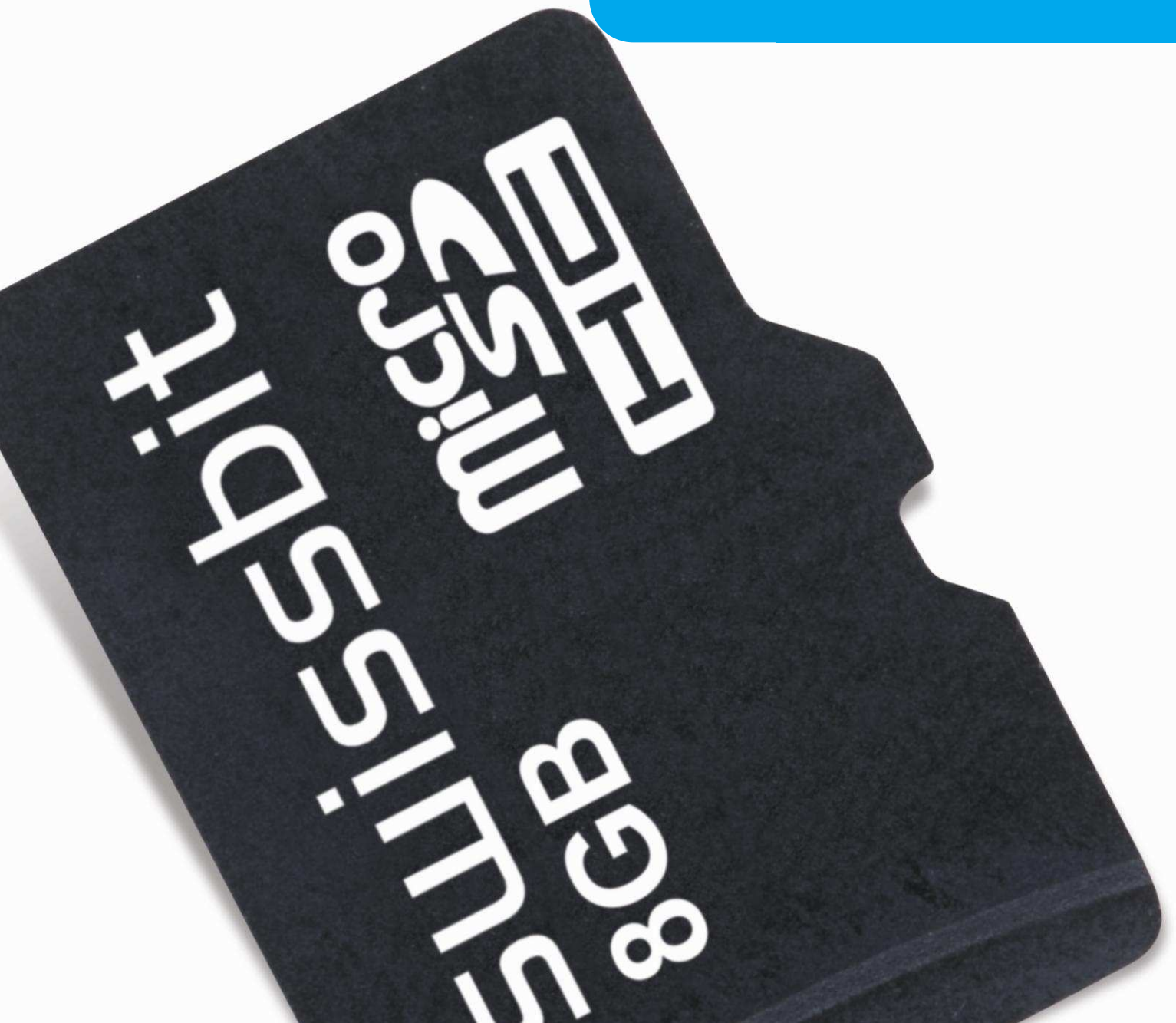


swissbit®

Product Data Sheet

Industrial  
MICRO SD Memory Card

**S-300u Series**  
SPI, SD and SDHC compliant



# S-300U SERIES

## MICRO SD Memory Card

### 1 Feature summary

- Highly-integrated memory controller
  - Fully compliant with SD Memory Card specification SD1.01, SD1.1, SD2.0 and SD3.01 and MICRO SD Memory Card Addendum 4.00
- Standard MICRO SD Memory Card form factor
  - 15.0mm x 11.0mm x 0.7mm
- Operating voltage 2.7...3.6V
- Low-power CMOS technology
- High reliability
  - MTBF: > 3,000,000 hours
  - Number of insertions: > 10,000
  - Extended Temperature range -25° up to 85°C
- Hot swappable
- High performance
  - Speed class
    - 2GB Card class 6
    - 4GB to 8GB class 10
  - SD burst up to 25MB/s
  - SD Low speed 0...25MHz clock rate
  - SD High speed 25...50MHz clock rate
  - Flash burst up to 40MB/s
  - Flash Bus interleave
- Operating bus modes: SD 1 & 4bit and SPI
- Error Correction up to 24bit/1KB BCH ECC
- Wear Leveling: equal wear leveling of static and dynamic data  
The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Write Endurance: Due to advanced wear leveling an even use of the entire flash is guaranteed, regardless how much "static" (0S) data is stored. Example: If the average file size is 10MByte and the total capacity is 8GByte, 48Mio write cycles can be performed.
- Available densities
  - 2, 4 and 8GBytes (SLC NAND Flash)
- Controlled BOM
- Life Cycle Management



### 2 Order Information

#### 2.1 Standard product list

Table 1: Standard Product List

Density	Part Number
2GB	SFSD2048NgBW1MT-E-ME-1x1-STD
4GB	SFSD4096NgBW1MT-E-DF-1x1-STD
8GB	SFSD8192NgBW1MT-E-QG-1x1-STD

g defines the product generation

x defines the FW

#### 2.2 Current product generation

Table 2: Standard Product List

Density	Part Number
2GB	SFSD2048N1BW1MT-E-ME-111-STD
4GB	SFSD4096N1BW1MT-E-DF-111-STD
8GB	SFSD8192N1BW1MT-E-QG-111-STD

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## 4 Product Specification

The MICRO SD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.

The card operates in two basic modes:

- **SD/SDHC card mode**
- **SPI mode**

The MICRO SD Memory Card also supports SD **High Speed mode** with up to 50MHz clock frequency.

The cards are compliant with

- SD Memory card Specification Part 1, Physical layer Specification V3.01
- SD Memory card Specification Part 2, File System Specification V3.00
- SD Memory card Specification Part 3, Security Specification V3.00
- MICRO SD Memory Card Addendum V4.00

Simplified specifications are available at [https://www.sdcard.org/downloads/pls/simplified\\_specs/](https://www.sdcard.org/downloads/pls/simplified_specs/)

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware **BCH Error Correction Code (ECC), defect handling, diagnostics and clock control**. The **advanced wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time. The hardware BCH-code ECC allows to **detect and correct up to 24 defect bits per 1kByte**.

The card has a **power-loss management feature** to prevent data corruption after power-down. The power consumption is very low.

The cards are RoHS compliant and lead-free.

### 4.1 System Performance

**Table 3: Performance**

System Performance		typ	max	Unit
Burst Data transfer Rate (max SD clock 50MHz)			25	MB/s
Sustained Sequential Read	2GB	19 <sup>(1)(2)</sup>	24 <sup>(1)(3)</sup>	
	4...8GB	19 <sup>(1)(2)</sup>	24 <sup>(1)(3)</sup>	
Sustained Sequential Write	2GB	11 <sup>(1)(2)</sup>	12 <sup>(1)(3)</sup>	
	4...8GB	17 <sup>(1)(2)</sup>	22 <sup>(1)(3)</sup>	

1. All values refer to Micron Flash 8Gb MICRO SD Memory Card in SD mode 50MHz, cycle time 20ns,
2. Sustained Speed measured with USB-SD Memory Card reader. It depends on burst speed, flash number, and file size.
3. Maximum values were measured with Testmetrix tester.

### 4.2 Environmental Specifications

#### 4.2.1 Recommended Operating Conditions

**Table 4: MICRO SD Memory Card Recommended Operating Conditions**

Parameter	min	typ	max	unit
Extended Operating Temperature	-25	25	85	°C
Power Supply VCC (3.3V)	2.7	3.3	3.6	V

**Table 5: Current consumption**

Current Consumption (typ)	typ	max	Unit
Write	60	70	mA
Read	50	60	
Sleep Mode	0.15	2	

#### 4.2.2 Recommended Storage Conditions

**Table 6: MICRO SD Memory Card Recommended Storage Conditions**

Parameter	min	typ	max	unit
Extended Storage Temperature	-25	25	85	°C

#### 4.2.3 Humidity & ESD

**Table 7: Humidity & ESD**

Parameter	Operating	Non Operating
Humidity (non-condensing)	operation: 95% RH @25°C storage: 93% RH @40°C, 500h	
EMC / EMI	<b>Non Contact Pads area:</b> ±8 kV (air discharge) Human body model according to IEC61000-4-2	<b>Contact Pads:</b> ±4 kV, Human body model according to IEC61000-4-2

#### 4.2.4 Environmental Conditions

**Table 8: Environmental Conditions**

Parameter	Operating	Non Operating
UV light exposure	UV: 254nm, 15Ws/cm <sup>2</sup> according to ISO7816-1	
Durability	10,000 mating cycles	
Drop test	1.5m free fall	
Bending / Torque	10N / 0.10Nm ±2.5° max	

#### 4.3 Physical Dimensions

**Table 9: Physical Dimensions**

Outer Physical Dimensions	Value	Unit
Length	15.0±0.1	mm
Width	11.0±0.1	
Thickness	0.7 (1.0)±0.1	
Weight (typ.)	0.4	g

#### 4.4 Reliability

**Table 10: Reliability**

Parameter	Value
Data Retention @ 25°C	10 years (JEDEC47G)

## 5 Capacity specification

**Table 11: MICRO SD Memory Card capacity specification**

Capacity	Sectors	Total addressable capacity (Byte)
2GB	4'016'128	2'056'257'536
4GB	8'042'496	4'117'757'952
8GB	16'136'192	8'261'730'304

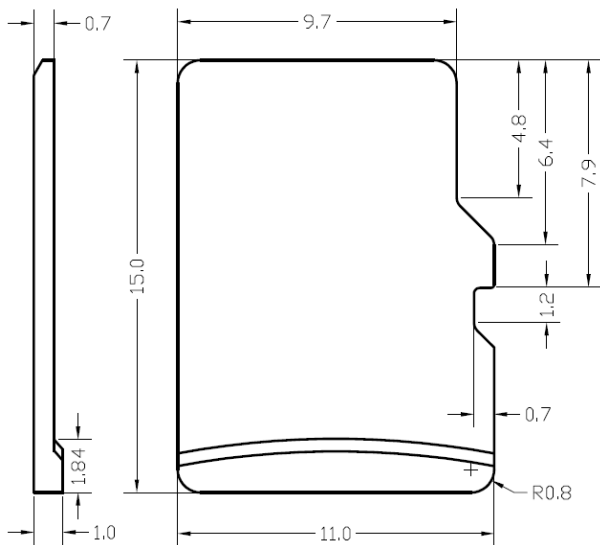
## 6 Card physical

### 6.1 Physical description

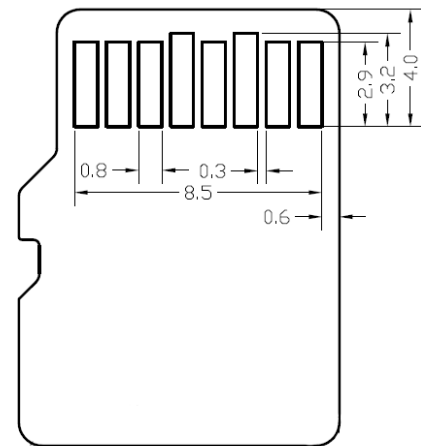
The MICRO SD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).

Figure 1 and Figure 2 show card dimensions.

**Figure 1: Mechanical Dimensions MICRO SD Memory Card (side and top, simplified)**



**Figure 2: Mechanical Dimensions MICRO SD Memory Card (bottom side with connector)**



# 7 Electrical interface

## 7.1 Electrical description

Figure 3: MICRO SD Memory Card Block Diagram

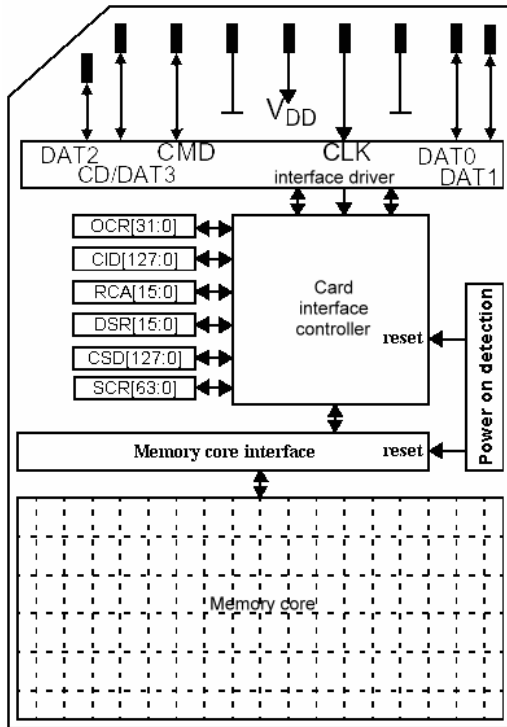


Figure 4: MICRO SD Memory Card Shape and Interface (Bottom View)

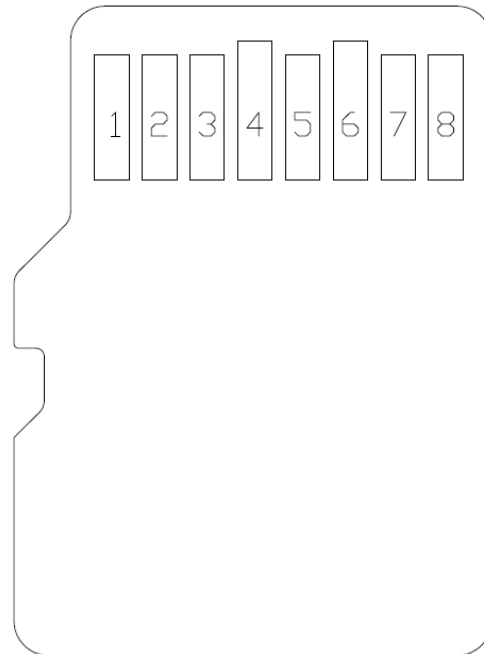


Table 12: MICRO SD Memory Card Pad Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type <sup>1</sup>	Description	Name	Type <sup>1</sup>	Description
1	DAT2 <sup>5</sup>	I/O/PP	Data Line [Bit 2]	RSV		
2	CD/DAT3 <sup>2</sup>	I/O/PP <sup>3</sup>	Card Detect/ Data Line [Bit 3]	CS	I <sup>3</sup>	Chip Select (negative true)
3	CMD	PP	Command/Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1 <sup>4</sup>	I/O/PP	Data Line [Bit 1]	RSV		

Notes:

- 1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
- 2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET\_BUS\_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
- 3) At power up this line has a 50kOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET\_CLR\_CARD\_DETECT (ACMD42) command
- 4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
- 5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).



## 7.2 DC characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

**Table 13: DC Characteristics**

Symbol	Parameter	min	typ	max	unit	notes
	Peak Voltage on all Lines	-0.3		VDD+0.3	V	
VIL	Input LOW Voltage	-0.3		0.25*VDD	V	
VIH	Input HIGH Voltage	0.625*VDD		VDD+0.3	V	
VOL	Output LOW Voltage			0.125*VDD	V	at 100µA
VOH	Output HIGH Voltage	0.75*VDD			V	at 100µA
IDD	Operating Current		35	50	mA	
	Pre-initialization Standby Current			3	mA	
	Post-initialization Standby Current		100	200	µA	
ILI	Input Leakage Current	-10		10	µA	without pull up R
ILO	Output Leakage Current	-10		10	µA	

**Table 14: MICRO SD Memory Card Recommended Operating Conditions**

Symbol	Parameter		min	typ	max	unit
VDD	Supply Voltage	Normal Operating Status	2.7		3.6	V
		Basic Communication (CMD0, CMD15, CMD55, ACMD41)	2.0	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

## 7.3 Signal Loading

The total capacitance  $C_L$  is the sum of the bus master capacitance  $C_{HOST}$ , the bus capacitance  $C_{BUS}$ , and the capacitance  $C_{CARD}$  of the card connected to the line:

$$C_L = C_{HOST} + C_{BUS} + C_{CARD}$$

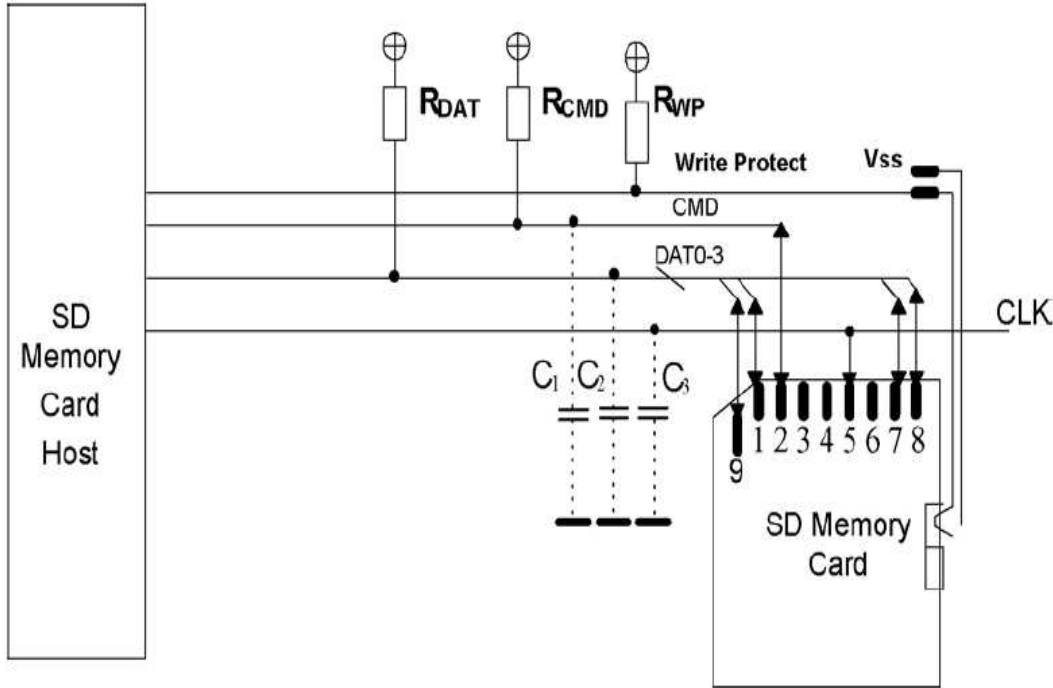
To allow the sum of the host and bus capacitances to be up to 20pF for the card, the following conditions in the table below are met by the card.

**Table 15: Signal loading**

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance	$R_{CMD}$	10	100	k0hm	To prevent bus floating
Pull up resistance	$R_{DAT}$	10	100	k0hm	To prevent bus floating
Bus signal line capacitance	$C_L$		40	pF	Single card
Signal card capacitance	$C_{card}$		10	pF	Single card
Signal line inductance			16	nH	$f \leq 20$ MHz



Figure 5: Signal Loading (MICRO SD Memory Card has no WP slider)



### 7.4 AC characteristics

Table 16: AC Characteristics Low Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	fPP	0	25	MHz	CL≤100pF
Clock frequency in card id mode	fOD	0	400	KHz	CL≤250pF
Clock low time	tWL	10/50		ns	CL≤100/250pF
Clock high time	tWH	10/50		ns	
Clock rise time	tTLH		10/50	ns	
Clock fall time	tTHL		10/50	ns	
CMD, DAT input setup time	tISU	5		ns	CL≤25pF
CMD, DAT input hold time	tIH	5		ns	
CMD, DAT output delay time	tODLY	0	14	ns	CL≤25pF, data transfer
CMD, DAT output delay time	tODLY	0	50	ns	CL≤25pF, identification

Notes

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required
5. Specified for one card

Figure 6: AC Characteristics Low Speed Mode

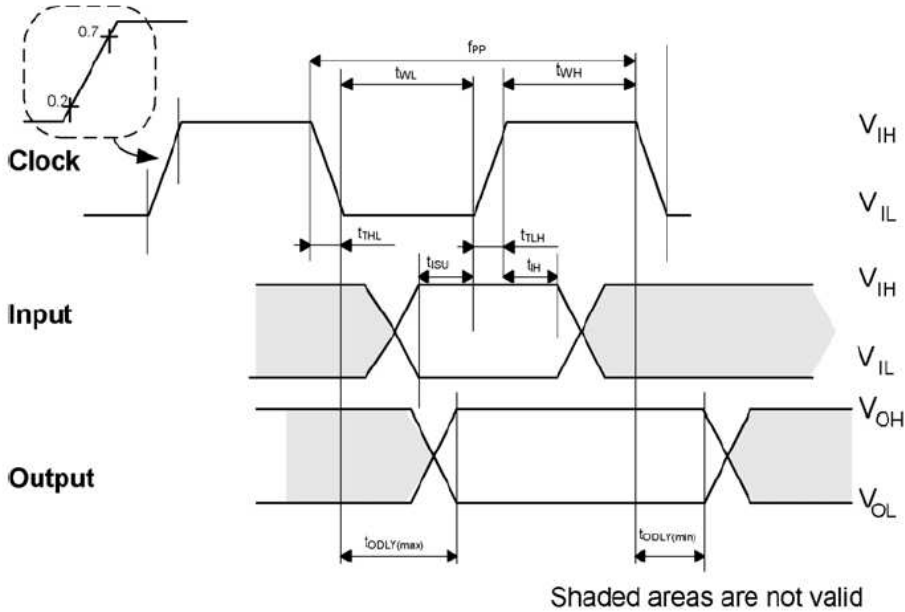


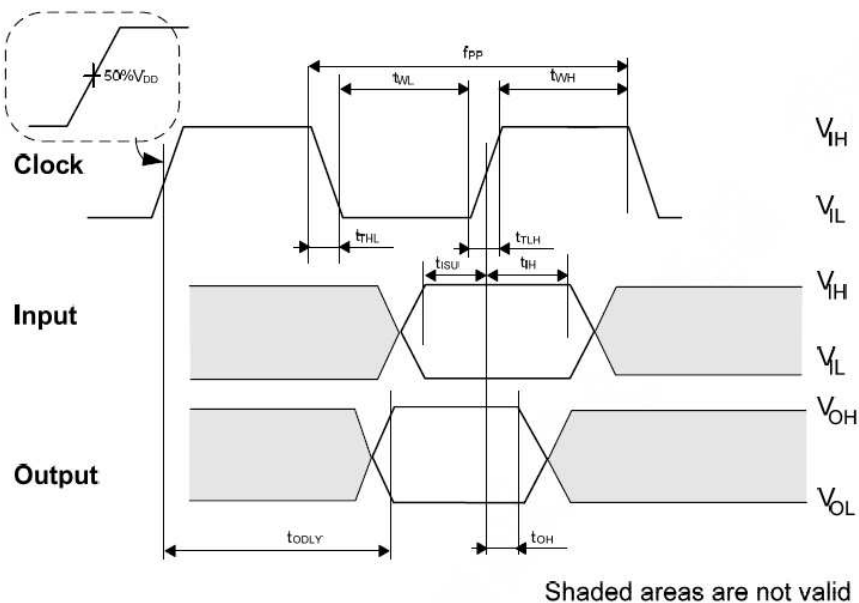
Table 17: AC Characteristics High Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	fPP	0	50	MHz	CL≤10pF
Clock low time	tWL	7.0		ns	
Clock high time	tWH	7.0		ns	
Clock rise time	tTLH		3	ns	
Clock fall time	tTHL		3	ns	
CMD, DAT input setup time	tISU	6		ns	
CMD, DAT input hold time	tIH	2		ns	
CMD, DAT output delay time during data transfer mode	tODLY		14	ns	
CMD, DAT output hold time	tOH	2.5		ns	

Notes

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to  $V_{IH}$  min and  $V_{IL}$  max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. In order to satisfy severe timing, the host shall drive only one card with max 40pF total at each line.

Figure 7: AC Characteristics High Speed Mode



## 8 Host access Specification

The following chapters summarize how the host accesses the card:

- Chapter 8.1 summarizes the SD and SPI buses.
- Chapter 8.2 summarizes the registers.

### 8.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

#### 8.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

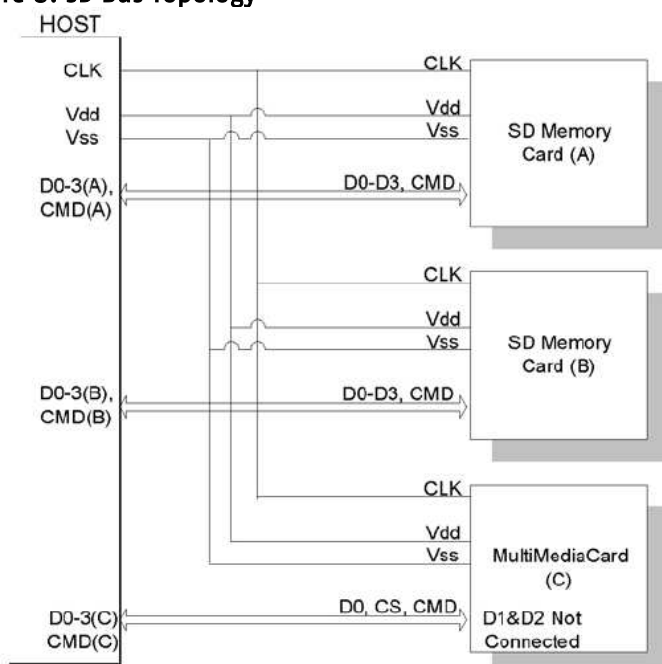
- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

The SD bus signals are listed in Table 18, and the SD bus topology is illustrated in Figure 8: SD Bus Topology.

**Table 18: SD Bus Signals**

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT0-DAT3	4 Bidirectional data signals
Vdd, Vss	Power and Ground

**Figure 8: SD Bus Topology**



### 8.1.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.

While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal. The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

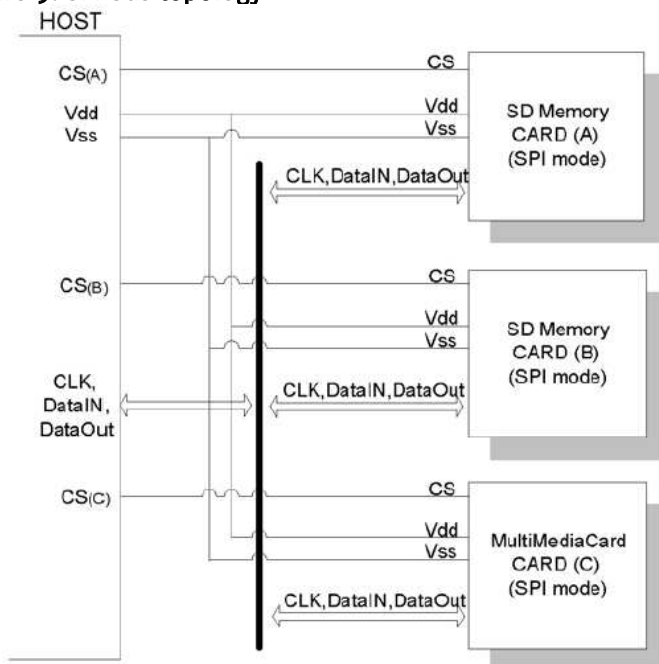
The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table 19 and the SPI bus topology is illustrated in Figure 9.

**Table 19: SPI Bus Signals**

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

**Figure 9: SPI bus topology**



### 8.1.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle\_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.

If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.

The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available. During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should re-start the card as Multimedia Card using CMD0 and CMD1.

## 8.2 Card Registers

The MICRO SD Memory Card has five registers. Refer to Table 20 to Table 25 for detail.

**Table 20: MICRO SD Memory Card registers**

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address is SD Card mode.

**Table 21: CID register**

Register Name	Bit Width	Description	typ. value
MID	8	Manufacture ID	TBD (0x5d)
OID	16	OEM/Application ID	TBD (0x5342)
PNM	40	Product Name	TBD ("NgBWc") g=generation c=number of channels
PRV	8	Product Revision	oxgg
PSN	32	Product Serial Number	xxxxxxxx
—	4	Reserved	0x0
MDT	12	Manufacture Date	oxyym
CRC	7	Check sum of CID contents	chksum
—	1	Not used; always=1	1

**Table 22: OCR register**

OCR bit position	VDD voltage window	typ. value	OCR bit position	VDD voltage window	typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	
13	2.5-2.6	0	30	Card Capacity Status (CCS)	*1)
14	2.6-2.7	0	31	o=busy; 1=ready	*2)

**Notes**

1. This bit is valid only when the card power up status bit is set.
2. This bit is set to LOW if the card has not finished the power up routine.

**Table 23: CSD register**

Register Name	Bits	Bit Width	Description	typ. Value 2GB	typ. Value 4GB, 8GB
CSD_STRUCTURE	127:126	2	CSD structure	00	01
–	125:120	6	Reserved	000000	000000
TAAC	119:112	8	Data read access time 1	01011110	00001110
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010	00110010
CCC	95:84	12	Card command classes	010110110101	010110110101
READ_BLK_LEN	83:80	4	Read data block length	1010	1001
READ_BLK_PARTIAL	79	1	Partial blocks for read allowed	1	0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0	0
DSR_IMP	76	1	DSR implemented	0	0
–	75:74	2	Reserved	00	–
C_SIZE	73:62	12	Device size	xxx*)	–
VDD_R_CURR_MIN	61:59	3	VDD min read current	101	–
VDD_R_CURR_MAX	58:56	3	VDD max read current	101	–
VDD_W_CURR_MIN	55:53	3	VDD min write current	101	–
VDD_W_CURR_MAX	52:50	3	VDD max write current	101	–
C_SIZE_MULT	49:47	3	Device size multiplier	111*)	–
–	75:70	6	Reserved	–	000000
C_SIZE	69:48	22	Device size	–	xxx*)
–	47	1	Reserved	–	0
ERASE_BLK_EN	46	1	Erase single block enable	1	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0111111*)	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	0	0
–	30:29	2	Reserved	00	00
R2W_FACTOR	28:26	3	Write speed factor	101	010
WRITE_BLK_LEN	25:22	4	Write data block length	1010*)	1001*)
WRITE_BLK_PARTIAL	21	1	Partial blocks for write allowed	0	0
–	20:16	5	Reserved	00000	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)	0 W(1)
COPY	14	1	Copy flag	0 W(1)	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)	00 W(1)
–	9:8	2	Reserved	00 W	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx W	xxxxxxx W
–	0	1	Always=1	1	1

\*) Drive Size and block sizes vary with card capacity

≤2Gb

memory capacity = BLOCKNR \* BLOCK\_LEN

Where

BLOCKNR = (C\_SIZE+1) \* MULT

MULT =  $2^{C\_SIZE\_MULT+2}$  (C\_SIZE\_MULT < 8)

BLOCK\_LEN =  $2^{READ\_BL\_LEN}$ , (READ\_BL\_LEN < 12)

>2Gb

memory capacity = (C\_SIZE+1) \* 512kByte

W value can be changed with CMD27 (PROGRAM\_CSD)

W(1) value can be changed ONCE with CMD27 (PROGRAM\_CSD)

**Table 24: SCR register**

Field	Bit Width	typ Value	remark
SCR_STRUCTURE	4	0000	SCR 1.01...2.00
SD_SPEC	4	0010	SD 2.0 or 3.0
DATA_STAT_AFTER_ERASE	1	0	0
SD_SECURITY	3	010 or 011	Version 1.01 (SD) or 2.00 (SDHC)
SD_BUS_WIDTHS	4	0101	1 or 4 bit
Reserved	16	0	0
Reserved	32	0	0

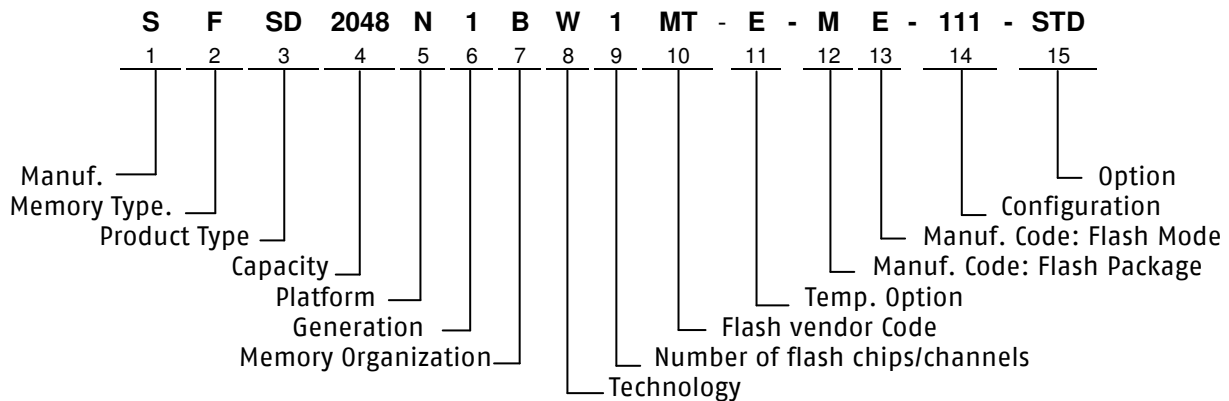
**Table 25: RCA register**

Field	Bit Width	typ Value
RCA	16	0x0000*)

\*) After Initialization the card can change the RCA register.



## 9 Part Number Decoder



### 9.1 Manufacturer

Swissbit code	S
---------------	---

### 9.2 Memory Type

Flash	F
-------	---

### 9.3 Product Type

SD Memory Card	SD
----------------	----

### 9.4 Capacity

2 GByte	2048
4 GByte	4096
8 GByte	8192

### 9.5 Platform

MICRO SD Memory Card	N
----------------------	---

### 9.6 Generation

Generation	1
------------	---

### 9.7 Memory Organization

x8	B
----	---

### 9.8 Technology

SD Memory Card controller	S-3x0 series	W
---------------------------	--------------	---

### 9.9 Channels

1 Flash Channel	1
-----------------	---

### 9.10 Flash Code

Micron	MT
--------	----

### 9.11 Temp. Option

Extended Temp. Range -25°C to 85°C	E
---------------------------------------	---

### 9.12 DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (dual die package)	Q
MLC MONO (single die package)	G
MLC DDP (dual die package)	L

### 9.13 PIN Mode

Single nCE & R/nB	E
Dual nCE & Dual R/nB	F
Quad nCE & Quad R/nB	G

### 9.14 Configuration XYZ

#### X → Configuration

Configuration	X
default	1

#### Y → FW Revision

FW Revision	Y
Version 1	1

#### Z → optional

Optional	Z
optional	1

### 9.15 Option

Swissbit / Standard	STD
---------------------	-----

## 10 Swissbit Label specification

### 10.1 Front side marking

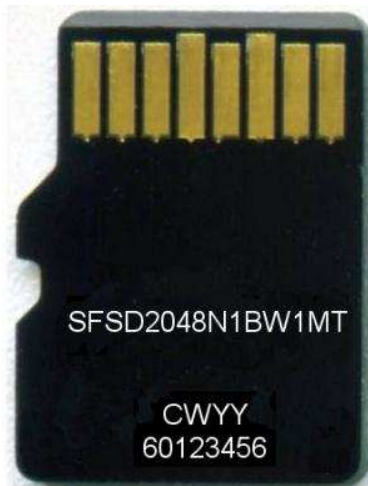


Swissbit

Density

SD Memory Card logo

### 10.2 Back side marking



Part Number

Calendar week and year  
Lot code

## 11 Revision History

**Table 26: Document Revision History**

Date	Revision	Revision Details
April 19, 2012	1.00	Initial release

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