swissbit®

Product data sheet

Parallel ATA (PATA) 2.5"-Solid State Drive

P-120 Series

up to UDMA4 / MDMA2 / PIO4

Standard and industrial temperature grade

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Parallel ATA (PATA) 2.5-inch Solid State Drive (SSD)
2 to 32GByte, 5V (or 3.3V) supply

1 Feature summary

- 2.5-inch ATA Solid State Drive (SSD)
  - 100.2mm x 70.0mm x 9.0mm
- Replacement of a standard IDE/ATA-compliant Hard Disk Drive (HDD)
- Highly-integrated memory controller
  - True IDE mode compatible
  - max. UDMA4 supported
  - max. PIO mode 4, MDMA2 supported
  - Hardware RS-code ECC (4 Bytes/528 Bytes correction)
  - fix drive configuration
- Low-power CMOS technology
- 3.3V / 5.0V power supply
- Power saving mode (with automatic wake-up)
- No mechanical noise
- Wear Leveling: equal wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Data retention 10 years @ 25°C
- S.M.A.R.T. support
- Host Protected Area (HPA) support
- Security Feature set support
- Write endurance: Due to intelligent wear leveling an even use of the entire flash is guaranteed, regardless how much "static" (OS) data is stored.
  Example: If the average file size is 10MByte and the total capacity is 8GByte, 80Mio write cycles can be performed.
- patented power-off reliability
  - No data loss of older sectors
  - Max. 32 sectors data loss (old data kept) if power off before card is not ready after last write command.
- High reliability
  - MTBF > 2,500,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Number of connector insertions/removals: >1,000
- High performance
  - Up to 66MB/s burst transfer rate in UDMA4
  - Sustained Write performance: up to 35MB/s
  - Sustained Read Performance: up to 40MB/s
- Available densities
  - 2 to 32GBytes
- Controlled BOM
- RoHS compatible

2 Contents

3 Order Information

Available Standard part numbers

FIX / PIO4, MDMA2, UDMA4 / 0°C – 70°C

Density	Part Number
2GB	SFPA2048QxBO2TO-**C**-MS-2y3-STD
4GB	SFPA4096QxBO2TO-**C**-DT-2y3-STD
8GB	SFPA8192QxBO2TO-**C**-QT-2y3-STD
16GB	SFPA16GBQxBO4TO-**C**-QT-2y3-STD
32GB	SFPA32GBQxBO8TO-**C**-QT-2y3-STD

Table 1: Standard temperature product list
x depends on product generation, y depends on the firmware generation

FIX / PIO4, MDMA2, UDMA4 / -40°C – +85°C

Density	Part Number
2GB	SFPA2048QxBO2TO-I-MS-2y3-STD
4GB	SFPA4096QxBO2TO-I-DT-2y3-STD
8GB	SFPA8192QxBO2TO-I-QT-2y3-STD
16GB	SFPA16GBQxBO4TO-I-QT-2y3-STD
32GB	SFPA32GBQxBO8TO-I-QT-2y3-STD

Table 2: Industrial temperature product list
x depends on product generation, y depends on the firmware generation

3.1 Offered OEM options

- Disabling MDMA and/or UDMA modes
- Customer specified drive size and drive geometry (C/H/S – cylinder/head/sector)
- Customer specified drive ID (Strings)
- Preload service (also images with any file system)
- Customized labels
- 2 Temperature ranges
  - Commercial Temperature range 0 ... +70°C
  - Industrial Temperature range -40 ... +85°C
- ROM mode (write protected with uploaded software)
- Special Firmware solutions for additional customer requirements
- ...

4 Product Specification

The Solid State Drive (SSD) is a small form factor non-volatile memory drive which provides high capacity data storage.
The drive with the IDE interface (2.00mm pitch) operates in three transfer modes:

- **UDMA (Ultra Direct Memory Access) up to Mode 4 66MB/s burst**
- **MDMA (Multi Word Direct Memory Access) up to Mode 2 16MB/s burst**
- **PIO (Programmed Input / Output) up to Mode 4 16MB/s burst**

The drive behaves as a standard ATA (IDE) disk drive. It can be set as master or slave by a jumper.
The drive has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.
The drive has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The specification has been realized and approved by the ATA/ATAPI-7 specification.
The system highlights are shown in Table 3 ...Table 10.

Related Documentation

- Parallel Transport Protocols and Physical Interconnect (ATA/ATAPI-7)
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994

4.1 System Performance

Table 3: System Performance

System Performance		Typ.	Max.	Unit
Sleep to write			5	ms
Sleep to read			5	
Power-on to Ready[3]		<500	1000	
Reset to Ready [3]			500	
Data transfer Rate (UDMA4 burst)			66 [1]	MB/s
Sustained Sequential Read (measured) UDMA4 128kB Block size	2..32GB	37 [1][2]	40 [1]	
Sustained Sequential Write (measured) UDMA4 128kB Block size	2..32GB	32 [1][2]	35 [1]	
Sustained Random Read (measured) UDMA4 4kB Block size	2..32GB	11 [1][2]	15 [1]	MB/s
Sustained Random Write (measured) UDMA4 4kB Block size	2..32GB	0.12 [1][2]	0.2 [1]	
Command to DRQ	Read	100	2000	µs
	Write	30	1000	

1. All values refer to Toshiba flash chips in UDMA4 mode with Sequential write/read test (256 sectors multiple commands) or Random write/read test (8 sectors multiple commands) with Firmware 090617.
2. Sustained Speed depends on flash type and number, file size, and burst speed
3. In case of IDE-Master with no slave drive additional max. 500ms
   In case of IDE-Master with additional slave drive depending on the slave handshaking (max. 31s)

4.2 Environmental Specifications

4.2.1 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage (5V)	4.5V to 5.5V – 5.0V ±10%
Power Supply VCC Voltage (3.3V)	2.97V to 3.63V – 3.3V ±10%

Table 5: Current consumption (1)

Current Consumption (type)	5V	Unit
Read (typ/max)	145/160	mA
Write (typ/max)	140/160	
Sleep/Idle Mode (typ/max) (2)	7/10	

1. All values are typical at 25° C and nominal supply voltage and refer to 8GByte SSD.
2. The card goes to Sleep/idle mode 20ms (default) after last host command.

4.2.2 Recommended Storage Conditions

Table 6: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-50°C to 100°C
Industrial Storage Temperature	-50°C to 100°C

4.2.3 Shock, Vibration, and Humidity

Table 7: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20G Peak, 10...2000Hz
Shock	1500G, 0.5ms duration, half sine wave

4.3 Physical Dimensions

Table 8: Physical Dimensions

Physical Dimensions		Unit
Length	100.20±0.2	mm
Width	69.85±0.2	
Thickness	9.00±0.1	
Weight (typ.)	85	g

4.4 Reliability

Table 9: System Reliability and Maintenance (1)

Parameter	Value
MTBF (at 25°C)	> 3,000,000 hours
Insertions/Removals	> 10,000
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read
Data Retention	10 years

1. Dependent on final system qualification data.

4.5 Drive geometry / CHS parameter

Table 10: SSD capacity specification

Capacity	Default_cylinders	Default_heads	Default_sectors _track	Sectors_drive	Total addressable capacity (Byte)
4GB	7,732	16	63	7,793,856	3,990,454,272
8GB	15,880	16	63	15,621,984	7,998,455,808
16GB	16,383*)	16	63	31,277,232	16,013,942,784
32GB	16,383*)	16	63	62,586,720	32,044,400,640

*) The CHS access is limited to about 8GB. Above 8GB the drive must be addressed in LBA mode.

4.6 Physical description

The Solid State Drive (SSD) contains a single chip controller and Flash memory modules. The controller interfaces with a host system allowing data to be written to and read from the Flash memory modules. The SSD is offered in a 2.5'' package with a standard 2.0mm pitch 44-pin connector consisting of two rows of 22 male contacts with a key pin. Beside the connector the SSD can configured with a Jumper as Master/Slave/Cable Select. Figure 14 and Figure 15 show SSD dimensions and connector location.

5 Electrical interface

5.1 Electrical description

The SSD is connected with a standard IDE 44 pin connector (pitch 2.00mm). The power is connected at pin 41-44. The Master card can be configured as Master or slave with a jumper at pins A – D.

The signal/pin assignments and descriptions are listed in Table 11 Low active signals have a '-' prefix. Pin types are Input, Output or Input/Output. Inputs are signals sourced from the host while Outputs are signals sourced from the Drive.

The configuration of the SSD is controlled using the standard IDE configuration registers starting at address 200h in the Attribute Memory space of the memory drive.

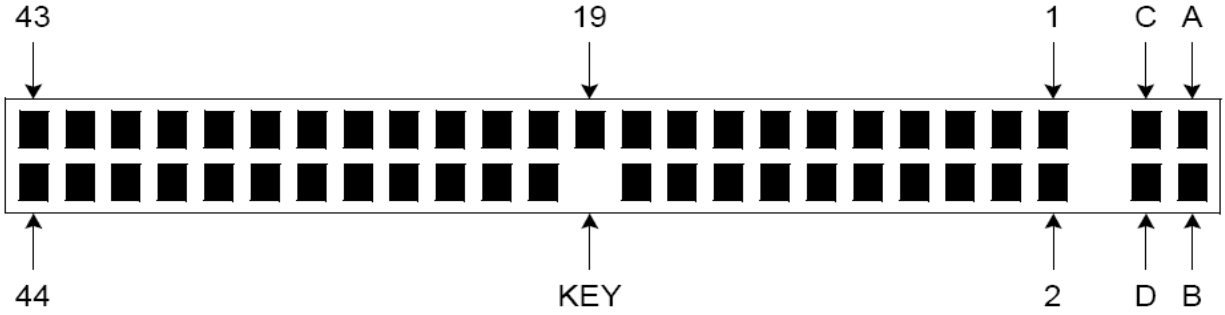


Table 11: Pin Assignment, Type, and description

Signal description	Pin Type	Signal Name	Pin Num		Signal Name	Pin Type	Signal description
Reset signal from host. Reset is active on power up and inactive thereafter.	I	-RESET	1	2	GND		Ground
Pins 3 through 18 (16 lines (15-0) carry the data between the controller and the host. The low 8 lines transfer commands and the ECC information between the host and the controller.	I/O	D07	3	4	D08	I/O	Pins 3 through 18 (16 lines (15-0) carry the data between the controller and the host. The low 8 lines transfer commands and the ECC information between the host and the controller.
	I/O	D06	5	6	D09	I/O	
	I/O	D05	7	8	D10	I/O	
	I/O	D04	9	10	D11	I/O	
	I/O	D03	11	12	D12	I/O	
	I/O	D02	13	14	D13	I/O	
	I/O	D01	15	16	D14	I/O	
	I/O	D00	17	18	D15	I/O	
Ground		GND	19	20	Key		Connector key
Not used.	0	DMARQ	21	22	GND		Ground
This I/O Write strobe pulse is used to clock I/O data or commands on the drive data bus into the drive controller registers when the drive is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).	I	-IOWR/ STOP	23	24	GND		Ground
This is a Read strobe generated by the host. The signal gates I/O data or status on the host bus and strobes the data from the controller into the host on the low to high transition (trailing edge).	I	-IORD HSTROBE - HDMARDY	25	26	GND		Ground

Signal description	Pin Type	Signal Name	Pin Num		Signal Name	Pin Type	Signal description
This is IORDY from the card from the drive to the host	O	IORDY – DDMARDY DSTROBE	27	28	CSEL	I	This internally pulled up signal is used to configure the drives as the Primary or the Secondary device. When the pin is grounded, the device is configured as the Primary device (master). When the pin is open, the device is configured as a Secondary device (slave).
Not used.	I	-DMACK	29	30	GND		Ground
This is an interrupt request from the drive to the host, asking for service. This signal is the active high Interrupt Request to the host.	O	INTRQ	31	32	(IOCS16)	O	Not used.
The address lines A1 and A0 are used to select one of eight registers in the controller Task File.	I	A1	33	34	-PDIAG	I/O	After an Executive diagnostic command to indicate that the Primary device has passed its diagnostics, this bi-directional open drain signal is asserted by the Secondary device.
	I	A0	35	36	A2	I	The address line A2 is used to select one of eight registers in the controller Task File.
The chip select signal used to select the Task File register.	I	-CS0	37	38	-CS1	I	The chip select signal used to select the Alternate Status register and the Device Control register.
This input/output is the Disk Active/Secondary Present signal in the Primary/ Secondary handshake protocol.	O	-DASP	39	40	GND		Ground
5V Power Supply		VCC	41	42	VCC		5V Power Supply
Ground		GND	43	44	NC		

5.2 Master-Slave configuration

The SSD can be configured as IDE Master or Slave Device with a Jumper beside the 44-pin connector (pins A, B, C, and D).

Table 12: Master Slave configuration

Jumper	Device configuration
No Jumper	Master
A to C	
C to D	
A to B	Slave
B to D	Cable Select*

*) The Device is master, if it is connected at the end,
or slave, if it is connected at the middle connector of a standard IDE cable

5.3 Electrical Specification

Table 15 – Table 18 define the DC Characteristics SSD. Unless otherwise stated, conditions are:

- Vcc = 5V ± 10%
- 0°C to +70°C

The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 14.

Table 13: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 6.5V
Voltage on any pin except VCC with respect to GND	V	-0.5V to VCC+0.5V

Table 14: Input Power write and read tests

Mode	Maximum Average RMS Current	Conditions
UDMA4	140mA	-40... +85 °C
MDMA2	110mA	

Table 15: Input Leakage current[1]

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current	IL	V_{IH} =Vcc V_{IL} = GND	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50		500	kOhm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50		500	kOhm

1. x refers to the characteristics described in Table 16 For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 16: Input characteristics

Type	Parameter	Symbol	Min.	Typ.	Max.	Units
1	Input Voltage CMOS	V_{IH}	2.0		5.3	V
		V_{IL}	-0.3		0.8	
2	Input Voltage CMOS	V_{IH}	2.0		5.3	V
		V_{IL}	-0.3		0.8	
3	Input Voltage CMOS Schmitt Trigger	V_{TH}	2.0		5.3	V
		V_{TL}	-0.3		0.8	

Table 17: Output Drive Type[1]

Type	Output Type	Valid Conditions
0tx	Totempole	I_{OH} & I_{OL}
0zx	Tri-State N-P Channel	I_{OH} & I_{OL}
0px	P-Channel Only	I_{OH} only
0nx	N-Channel Only	I_{OL} only

1. x refers to the characteristics described in Table 16 For example, 0T3 refers to totem pole output with a type 3 output drive characteristic.

Table 18: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
1	Output Voltage	V_{OH}	I_{OH}= -1mA	2.4			V
		V_{OL}	I_{OL} = 4mA			0.45	
2	Output Voltage	V_{OH}	I_{OH} = -1mA	2.4			V
		V_{OL}	I_{OL} = 4mA			0.45	
3	Output Voltage	V_{OH}	I_{OH}= -1mA	2.4			V
		V_{OL}	I_{OL} = 4mA			0.45	
	Tri-State	I_{OZ}	V_{OL}= Gnd	-10		10	µA
X	Leakage Current		V_{OH} = Vcc				

6 Command Interface

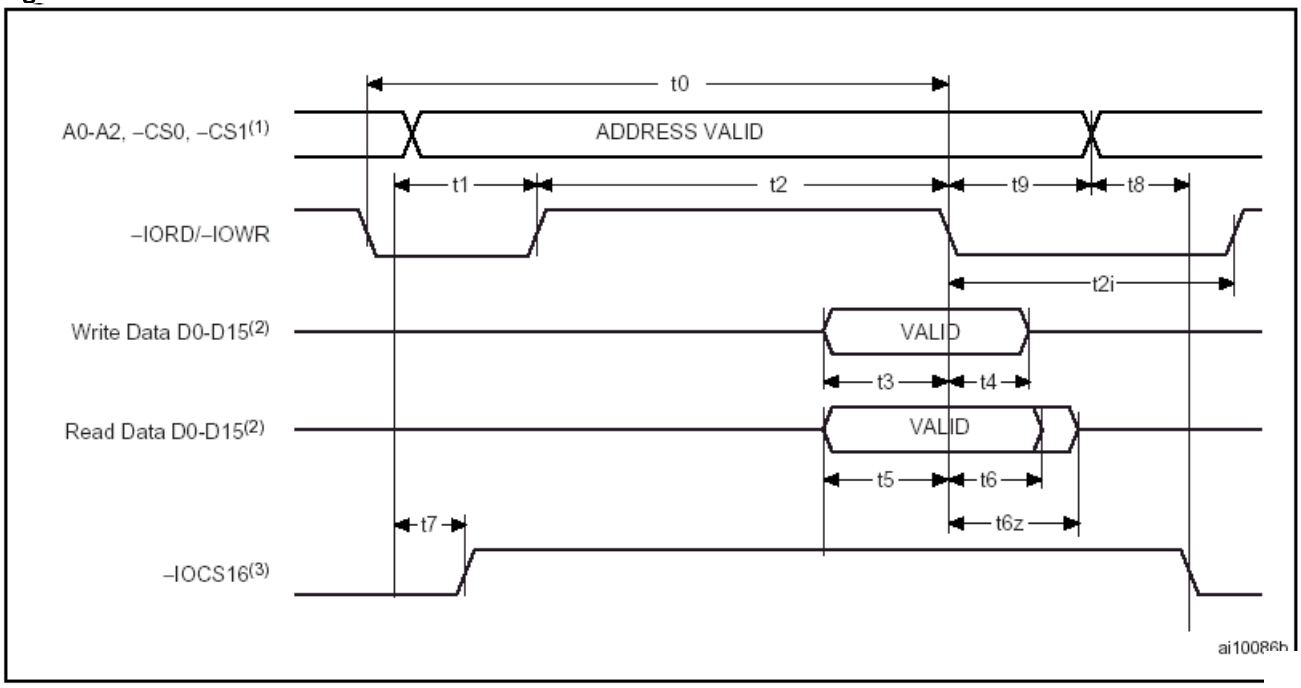
There are two types of bus cycles and timing sequences that occur in the IDE interface, PIO and Multi-Word DMA (MDMA) as well as Ultra DMA (UDMA).

Figure 1 and Figure 2 show the read and write timing diagrams. Table 19, and Table 20 specify the read and write timing parameters for PIO and MDMA mode, respectively.

6.1 PIO Mode

The timing waveforms for True IDE mode and True IDE DMA mode of operation in this section are drawn using the conventions in the ATA-7 specification. Signals are shown with their asserted state as High regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the –IOWR and the –IOCS16 signals are shown in the waveforms inverted from their electrical states on the bus.

Figure 1: True IDE PIO mode Read/Write waveforms



1. The device addresses consists of –CS0, –CS1, and A2-A0.
2. The Data I/O consist of D15-D0 (16-bit) or D7-D0 (8 bit).
3. –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

Table 19: True IDE PIO mode Read/Write timing(1)

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)
Cycle time (min)	t_0(2)	600	383	240	180	120
Address Valid to –IORD/–IOWR setup (min)	t_1	70	50	30	30	25
–IORD/–IOWR (min)	t_2(2)	165	125	100	80	70
–IORD/–IOWR (min) Register (8 bit)	t_2(2)	290	290	290	80	70
–IORD/–IOWR recovery time (min)	t_{2i}(2)	–	–	–	70	25
–IOWR data setup (min)	t_3	60	45	30	30	20
–IOWR data hold (min)	t_4	30	20	15	10	10
–IORD data setup (min)	t_5	50	35	20	20	20
–IORD data hold (min)	t_{6z}(3)	5	5	5	5	5
–IORD data tri-state (max)	t_7(4)	30	30	30	30	30
Address valid to –IOCS16 assertion (max)	t_8(4)	90	50	40	NA	NA
Address valid to –IOCS16 released (max)	t_7	60	45	30	NA	NA
–IORD/–IOWR to address valid hold	t_9	20	15	10	10	10

1. The maximum load on –IOCS16 is 1 LSTTL with a 50pF total load.
2. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command inactive time. The three timing requirements of to, t_2, and t_{2i} have to be met. The requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can ensure that to is equal to or greater than the value reported in the devices identify drive implementation should support any legal host implementation.
3. This parameter specifies the time from the falling edge of –IORD to the moment when the drive (tri-state).
4. t_7 and t_8 apply only to modes 0, 1 and 2. The –IOCS16 signal is not valid for other modes.

6.2 MDMA Mode

Figure 2: True IDE Multi-Word DMA Mode Read/Write waveforms

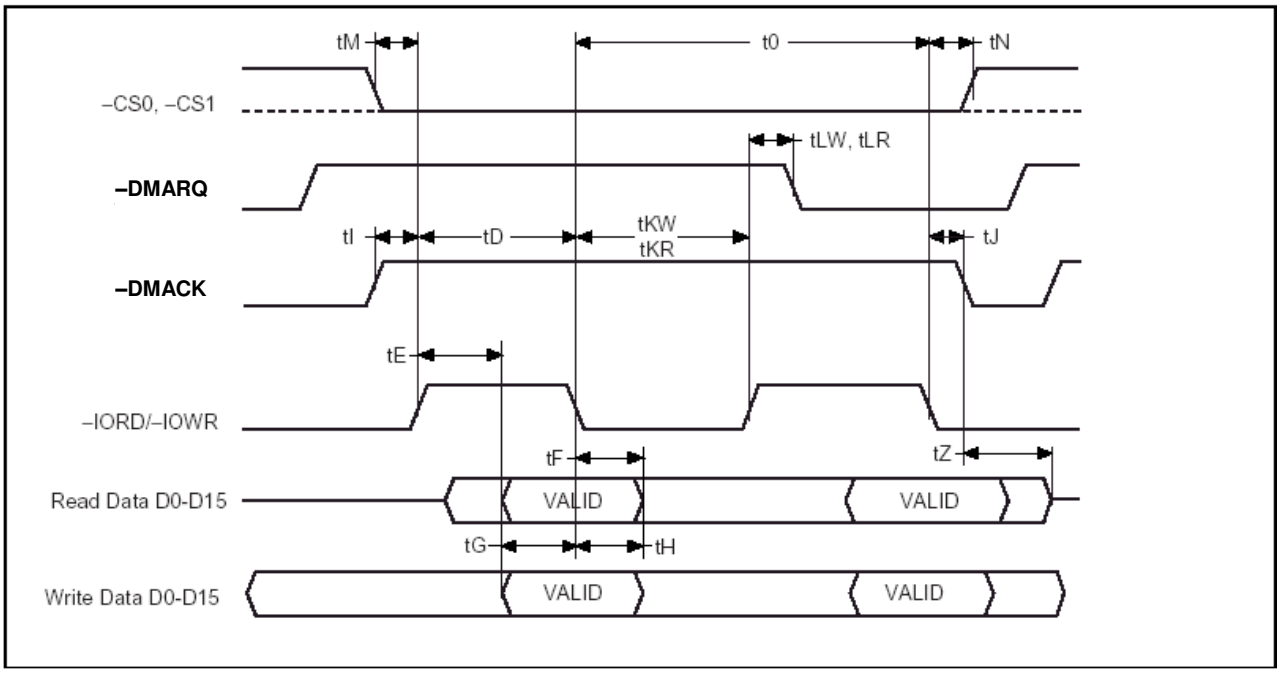


Table 20: True IDE Multi-Word DMA Mode Read/Write timing

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)
Cycle time (min)	t_0 (1)	480	150	120
-IORD / -IOWR asserted width (min)	t_D (1)	215	80	70
-IORD data access (max)	t_E	150	60	50
-IORD data hold (min)	t_F	5	5	5
-IORD/-IOWR data setup (min)	t_G	100	30	20
-IOWR data hold (min)	t_H	20	15	10
DMACK to –IORD/-IOWR setup (min)	t_I	0	0	0
-IORD / -IOWR to –DMACK hold (min)	t_J	20	5	5
-IORD Low width (min)	t_{KR} (1)	50	50	25
-IOWR Low width (min)	t_{KW} (1)	215	50	25
-IORD to DMARQ delay (max)	t_{LR}	120	40	35
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35
CS(1:0) valid to –IORD / -IOWR	t_M	50	30	25
CS(1:0) hold	t_N	15	10	10
-DMACK	t_Z	20	25	25

1. t_0 is the minimum total cycle time. T_D is the minimum command active time. T_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles, respectively. The actual cycle time is the sum of the actual command active time and the actual command inactive time. The timing requirements of t_0, t_D, t_{KR}, and t_{KW} must be respected. T_0 is higher than $t_D + t_{KR}$ or $t_D + t_{KW}$, for input and output cycles respectively. This means the host can lengthen either t_0 or t_{KR}/t_{KW}, or both, to ensure that t_0 is equal to or higher than the value reported in the devices identify device data. A Drive implementation shall support any legal host implementation.

6.3 Ultra DMA Mode

6.3.1 Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).
The usage of signals in each of the modes is shown in Table 21: Signal Usage in PIO/MDMA vs. UDMA Mode

Table 21: Signal Usage in PIO/MDMA vs. UDMA Mode

UDMA Signal	Pin	Type	PIO / MDMA	UDMA	Remark
DMARQ	21	Output	DMARQ		
DMACK	29	Input	-DMACK		
STOP	23	Input	-IOWR	STOP [1]	
HDMARDY(R) HSTROBE(W)	25	Input	-IORD	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]	UDMA write clock from host
DDMARDY(W) DSTROBE(R)	27	Output	IORDY	-DDMARDY(W) [1, 3] DSTROBE(R) [1. 2. 4]	UDMA read clock from drive
DATA	3 - 18	Bidir	D[15:00]		
ADDRESS	33, 35, 36	Input	A[02:00]		
CSEL	28	Input	-CSEL		
INTRQ	31	Output	INTRQ		
Card Select	37, 38	Input	-CS0, -CS1		

Notes:

1. The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2. The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.
3. The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4. The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.

Several signal lines are redefined to provide different functions during an Ultra DMA burst. These lines assume these definitions when:

1. an Ultra DMA mode is selected, and
2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and
3. the device asserts (-)DMARQ, and
4. the host asserts -DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA burst.
With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.
During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.
Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.
An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any

previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.
Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.
NOTE – If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

6.3.1.1 UDMA Address and Card Select Signals

The Card Select signals -CS0 and -CS1) shall remain negated during Ultra DMA data bursts.
The Address bus (A[2:0]) shall not transition unnecessarily during the UDMA command and shall remain fixed during an Ultra DMA data burst. In True IDE mode, the address lines (A[2:0]) shall be held to all zeros. This will reduce unnecessary noise during the UDMA command.

6.3.1.2 Task File registers shall not be written during an Ultra DMA command

The task file registers shall not be written after an Ultra DMA command is issued by the host and before the command completes. Writing to the device control register is permitted between bursts, but is expected to occur only to reset the drive after an unrecoverable protocol error.

6.3.1.3 Ultra DMA transfers shall be 16 bits wide

All transfers during an Ultra DMA data burst are 16 bit wide transfers. The Set Features command that controls the bus width for PIO transfers does not affect the width of Ultra DMA transfers.

6.3.2 Ultra DMA Phases of Operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see: 6.3.2.4 , for the detailed protocol descriptions for each of these phases. Table 22: Ultra DMA Data Burst Timing Requirements and Table 23: Ultra DMA Data Burst Timing Descriptions define the specific timing requirements). In the following rules -DMARDY is used in cases that could apply to either -DDMARDY or -HDMARDY, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1. An Ultra DMA burst is defined as the period from an assertion of -DMACK by the host to the subsequent negation of -DMACK.
2. When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused. When operating in Ultra DMA modes 6, 5, 4, or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA burst is paused.

6.3.2.1 Ultra DMA Burst Initiation Phase Rules

1. An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.
2. An Ultra DMA burst shall always be requested by a device asserting DMARQ.
3. When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting -DMACK.
4. A host shall never assert -DMACK without first detecting that DMARQ is asserted.
5. For Ultra DMA data-in bursts: a device may begin driving D[15:00] after detecting that -DMACK is asserted, STOP negated, and -HDMARDY is asserted.
6. After asserting DMARQ or asserting -DDMARDY for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.
7. After negating STOP or asserting -HDMARDY for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

6.3.2.2 Ultra DMA Data transfer phase rules

1. The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.
2. A recipient pauses an Ultra DMA burst by negating –DMARDY and resumes an Ultra DMA burst by reasserting –DMARDY.
3. A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
4. A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate –DMARDY and wait the required period before signaling a termination request.
5. A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

6.3.2.3 Ultra DMA Burst Termination Phase Rules

1. Either a sender or a recipient may terminate an Ultra DMA burst.
2. Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.
3. An Ultra DMA burst shall be paused before a recipient requests a termination.
4. A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
5. A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.
6. Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
7. A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.
8. Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
9. A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

6.3.2.4 Ultra DMA Data Transfers Timing

Table 22 and Table 23 define the timings associated with all phases of Ultra DMA bursts.

Table 22: Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)		Measurement location (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note 3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note 4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes:

1. All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2. All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and –DMARDY transitions are measured at the sender connector.
3. The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4. The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
5. The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.
6. See the AC Timing requirements in Table 23: Ultra DMA Data Burst Timing Descriptions.

Table 23: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1. The parameters t_{UI}, t_{MLI} (in Figure 6: Ultra DMA Data-In Burst Device Termination Timing and Figure 7: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
2. 80-conductor cabling shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.
3. Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
4. For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
5. The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

Table 24: Ultra DMA Sender and Recipient IC Timing Requirements

Name	Comments	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8		4.8		4.8	
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0		9.0		9.0	

Notes:

1. All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.
2. The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
3. The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 25: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note:

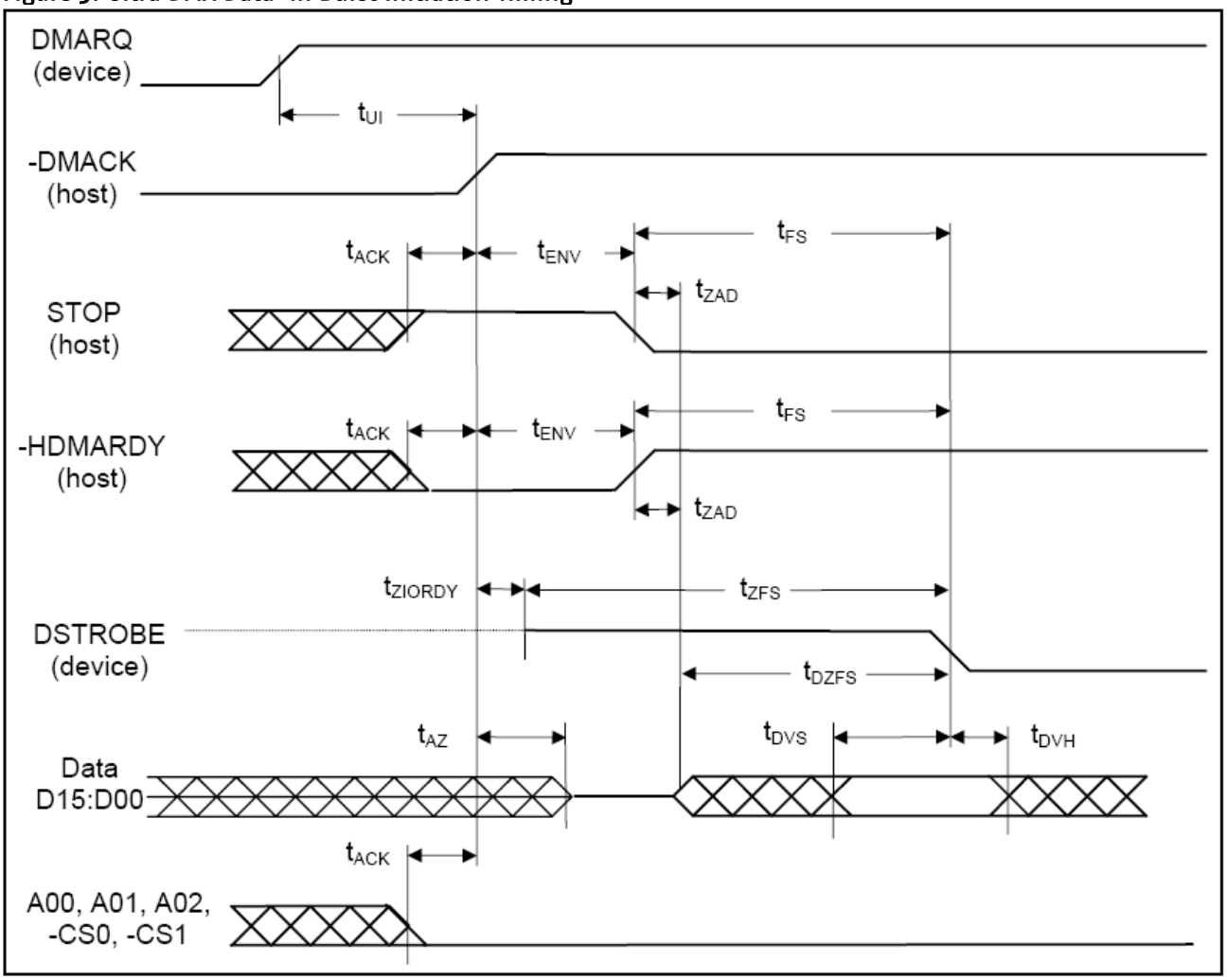
1. The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.
   The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.
   Measurements shall be taken at the test point using a <1 pF, >100 kOhm, 1 GHz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 ns apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

6.3.2.4.1 Initiating an Ultra DMA Data-In Burst

a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 3: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.
b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:
c) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
d) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
e) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
f) The host shall negate -HDMARDY.
g) The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.
h) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
i) The host shall release D[15:00] within t_{AZ} after asserting -DMACK.

j) The device may assert DSTROBE t_{ZIORDY} after the host has asserted -DMACK. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA burst.
k) The host shall negate STOP and assert -HDMARDY within t_{ENV} after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
l) The device shall drive D[15:00] no sooner than t_{ZAD} after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY.
m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).
n) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto D[15:00].

Figure 3: Ultra DMA Data-In Burst Initiation Timing



Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted.

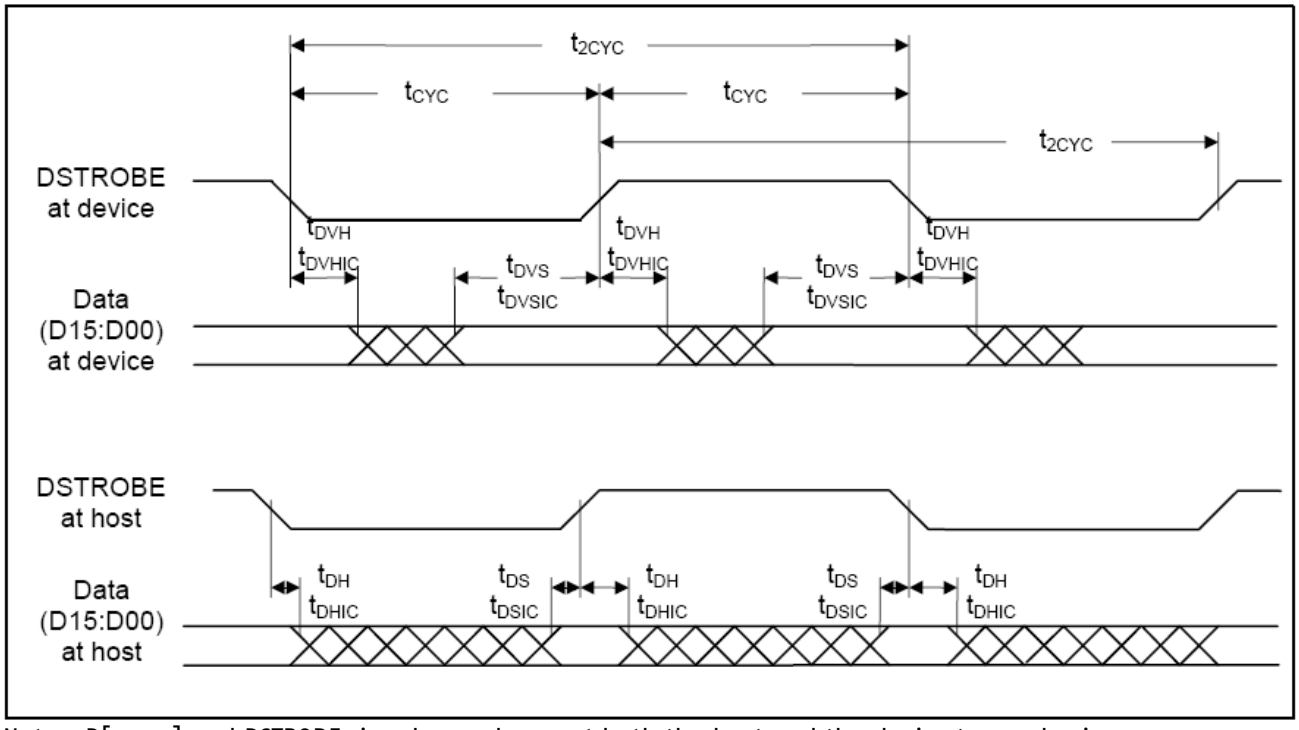
6.3.2.4.2 Sustaining an Ultra DMA Data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 4: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].
b) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.
c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.
d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

Figure 4: Sustained Ultra DMA Data-In Burst Timing



Notes: D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

6.3.2.4.3 Host Pausing an Ultra DMA Data-In Burst

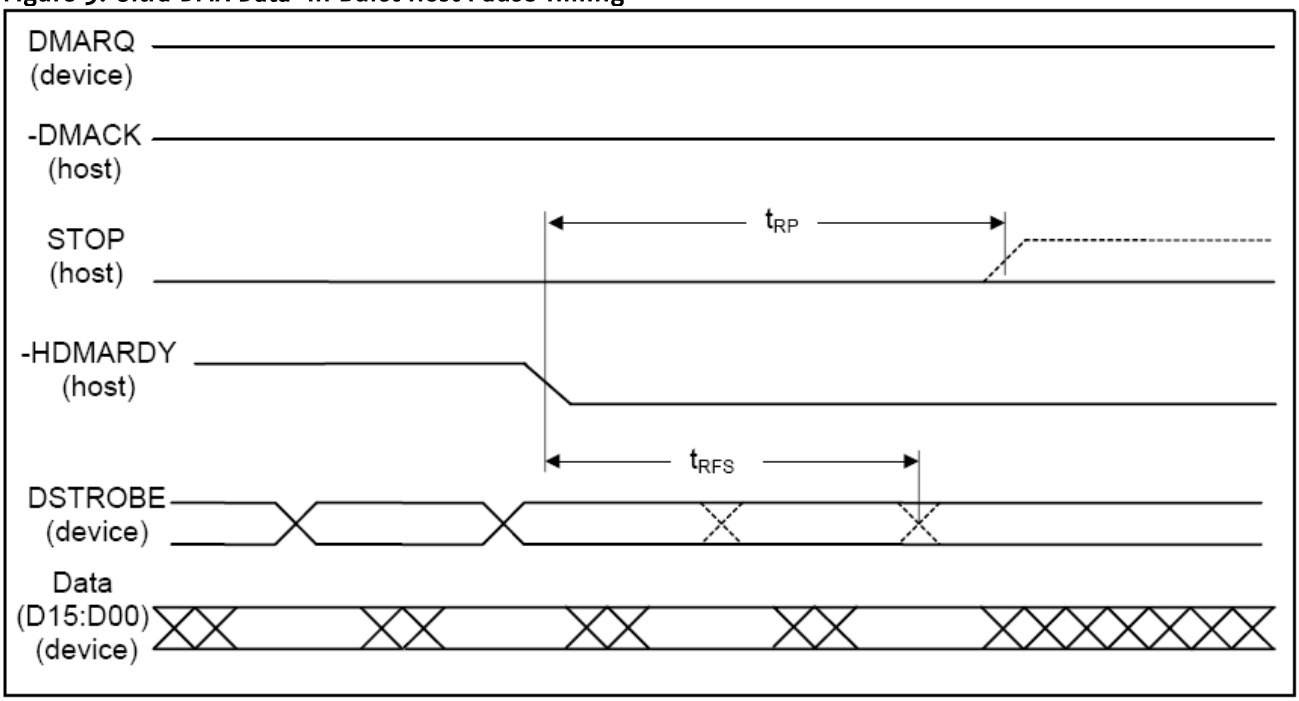
The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 5: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The host shall pause an Ultra DMA burst by negating -HDMARDY.
c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY.
d) If the host negates -HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates -HDMARDY greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.

e) The host shall resume an Ultra DMA burst by asserting -HDMARDY.

Figure 5: Ultra DMA Data-In Burst Host Pause Timing



Notes:

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after -HDMARDY is negated.
2. After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

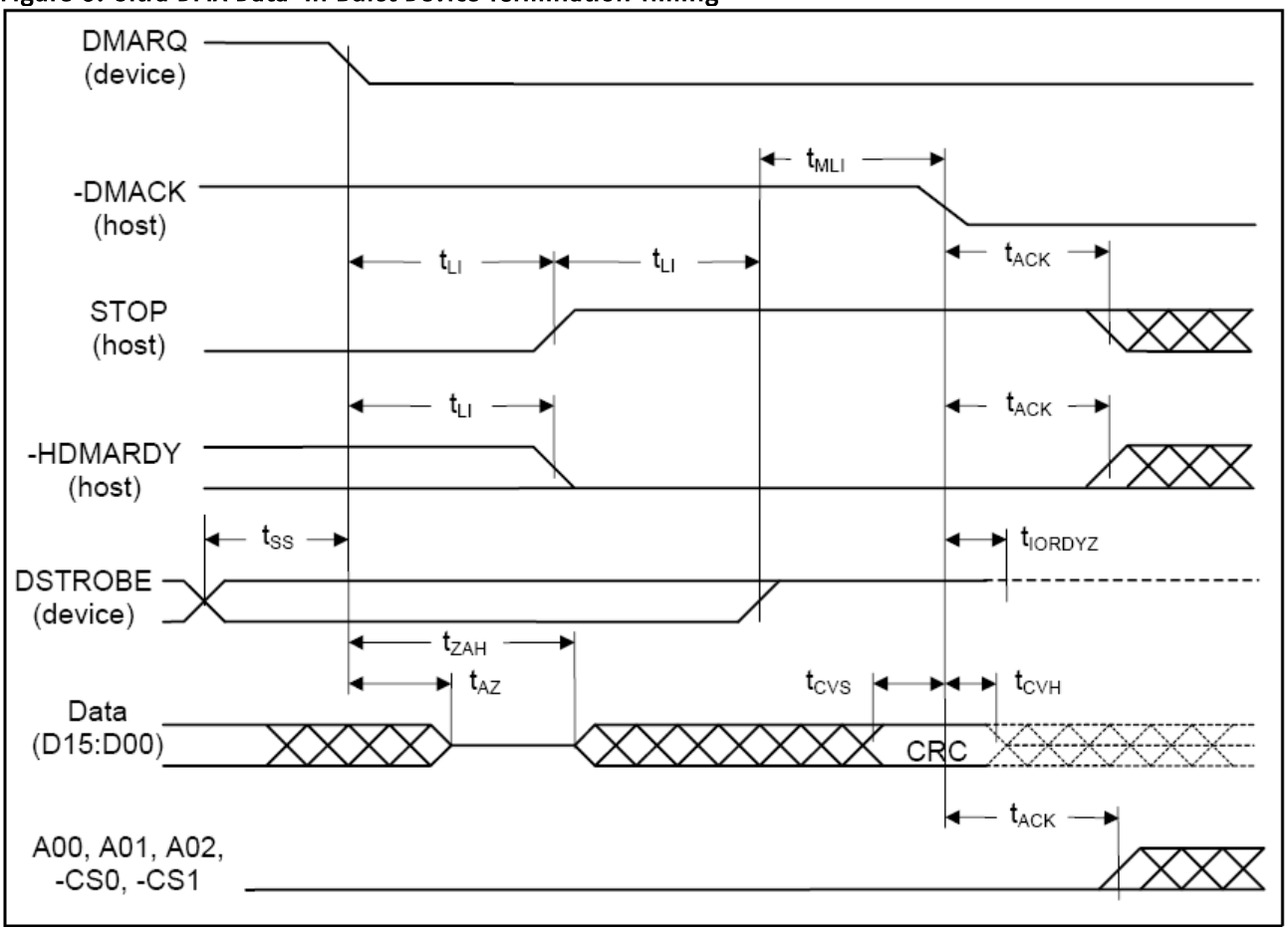
6.3.2.4.4 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 6: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra
b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.
c) NOTE – The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate
d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

Figure 6: Ultra DMA Data-In Burst Device Termination Timing



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

6.3.2.4.5 Host Terminating an Ultra DMA Data-In Burst

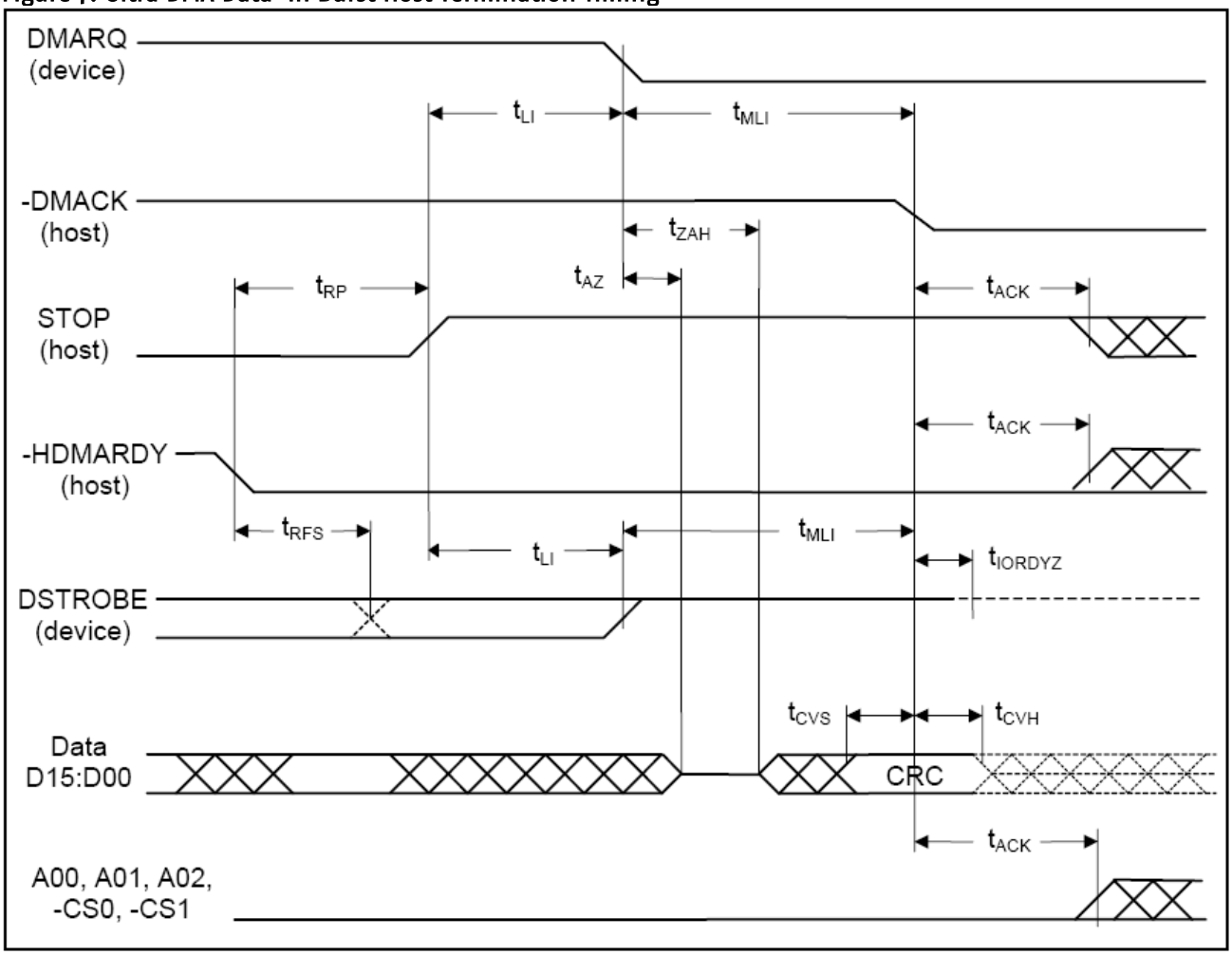
The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 7: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
b) The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.
c) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating -HDMARDY
d) If the host negates -HDMARDY within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDYgreater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
e) The host shall assert STOP no sooner than t_{RP} after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
f) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
g) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h) The device shall release D[15:00] no later than t_{AZ} after negating DMARQ.
i) The host shall drive DD D[15:00] no sooner than t_{ZAH} after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation (see 6.3.2.5).

j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00] (see 6.3.2.5).
k) The host shall negate -DMACK no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than t_{DVS} after the host places the result of its CRC calculation on D[15:00].
l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred (see 6.3.2.5).
n) The device shall release DSTROBE within t_{IORDYZ} after the host negates -DMACK.
o) The host shall neither negate STOP nor assert -HDMARDY until at least t_{ACK} after the host has negated -DMACK.
p) The host shall not assert -IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

Figure 7: Ultra DMA Data-In Burst Host Termination Timing



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

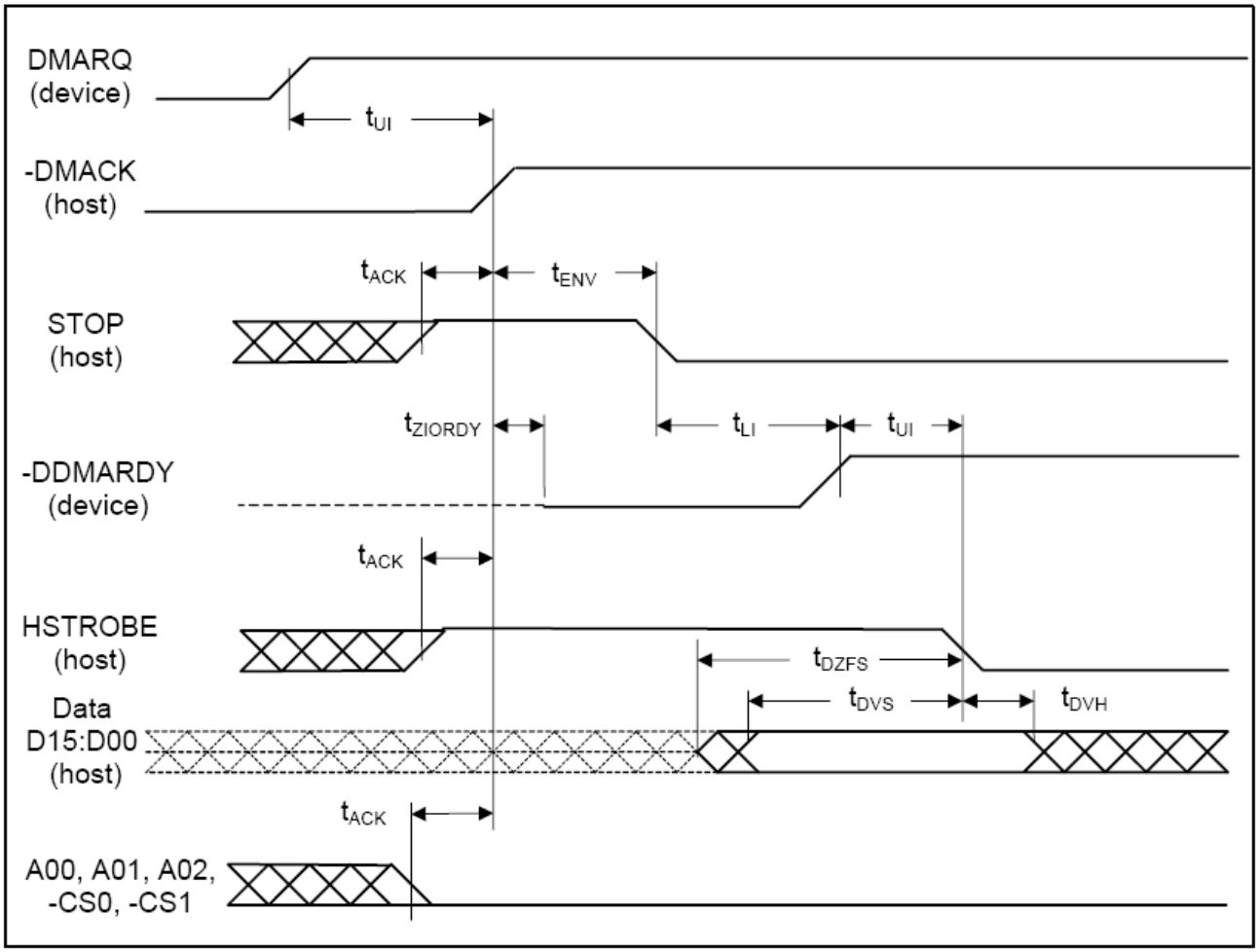
6.3.2.4.6 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 8: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:
a) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
b) The device shall assert DMARQ to initiate an Ultra DMA burst.
c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
d) The host shall assert HSTROBE.

e) The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.
f) Steps (c), (d), and (e) shall have occurred at least t_{ACK} before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
g) The device may negate -DDMARDY t_{ZIORDY} after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.
h) The host shall negate STOP within t_{ENV} after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.
i) The device shall assert -DDMARDY within t_{LI} after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.
j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.
k) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto D[15:00].

Figure 8: Ultra DMA Data-Out Burst Initiation Timing



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

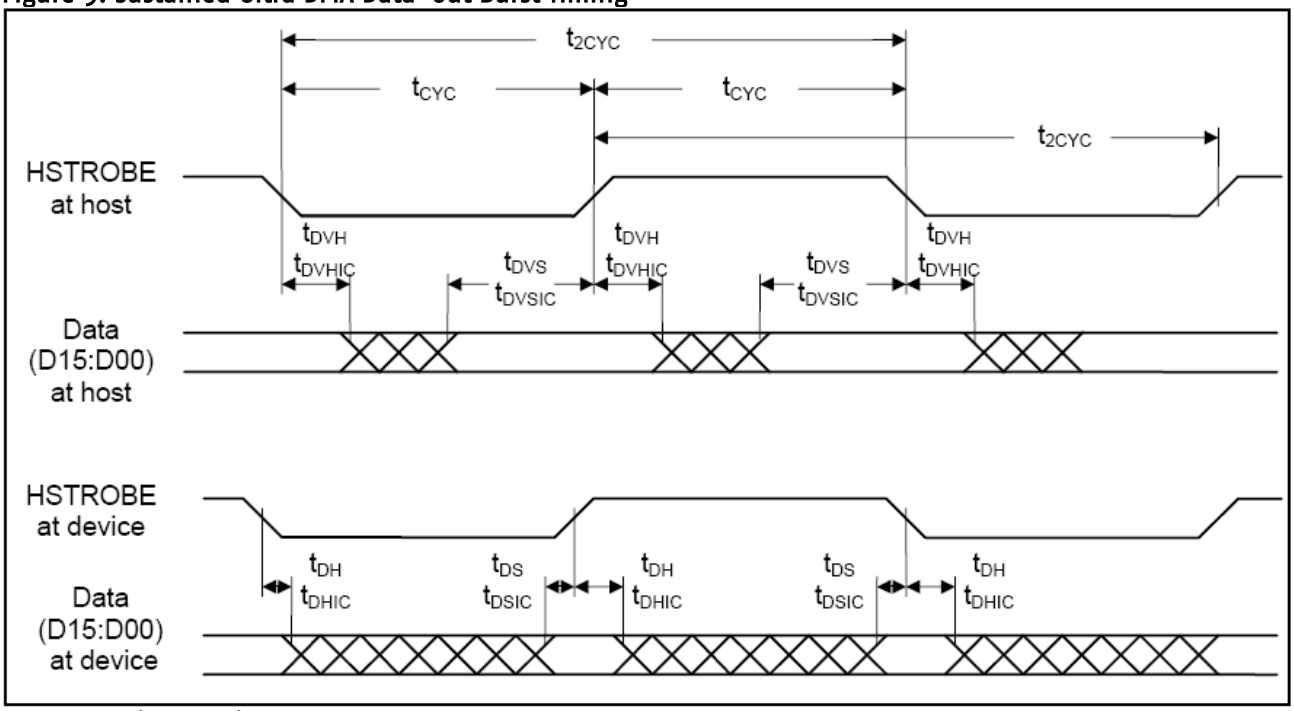
6.3.2.4.7 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in
Figure 9: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall drive a data word onto D[15:00].
b) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than $2t_{cyc}$ for the selected Ultra DMA mode.
c) The host shall not change the state of D[15:00] until at least t_{DVH} after generating an HSTROBE edge to latch the data.
d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

Figure 9: Sustained Ultra DMA Data-Out Burst Timing



Note: Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

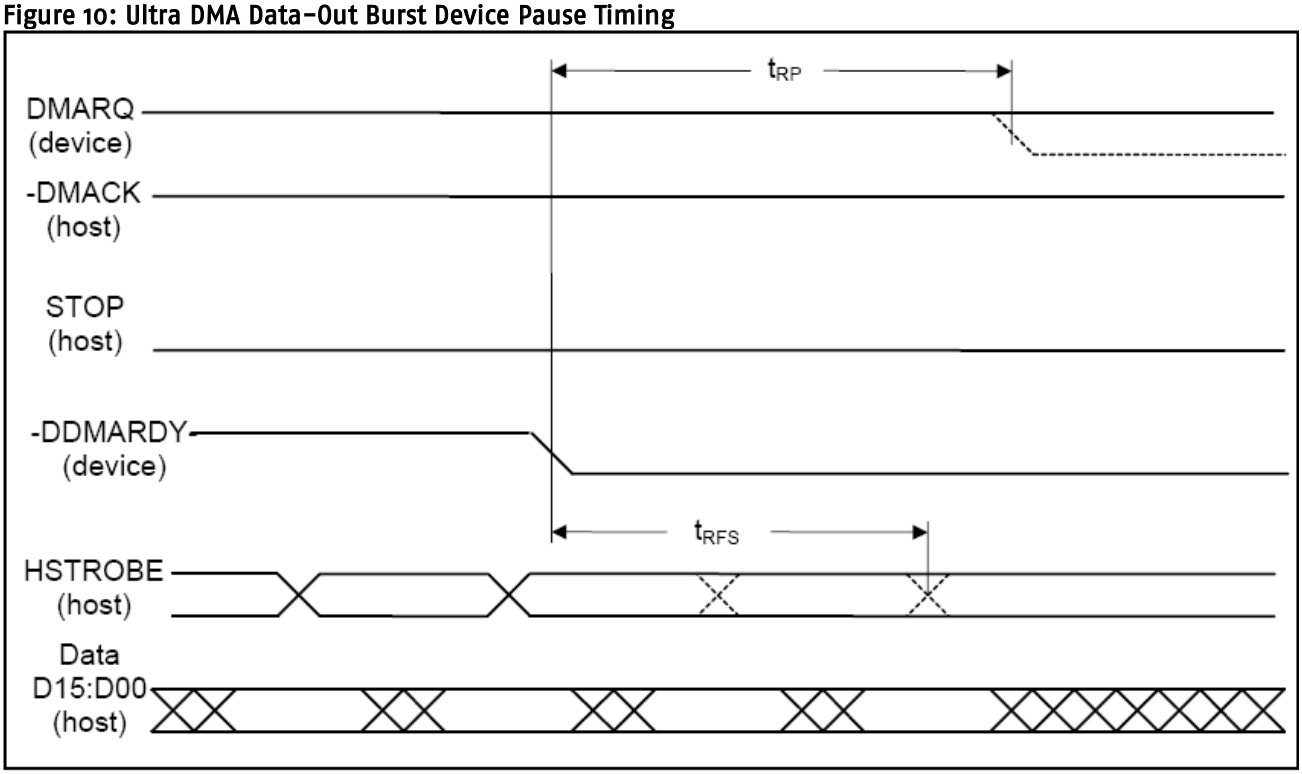
6.3.2.4.8 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 10: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall pause an Ultra DMA burst by negating -DDMARDY.
c) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating -DDMARDY.
d) If the device negates -DDMARDY within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
e) The device shall resume an Ultra DMA burst by asserting -DDMARDY.

Figure 10: Ultra DMA Data-Out Burst Device Pause Timing



Notes:

1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than tRP after -DDMARDY is negated.
2. After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

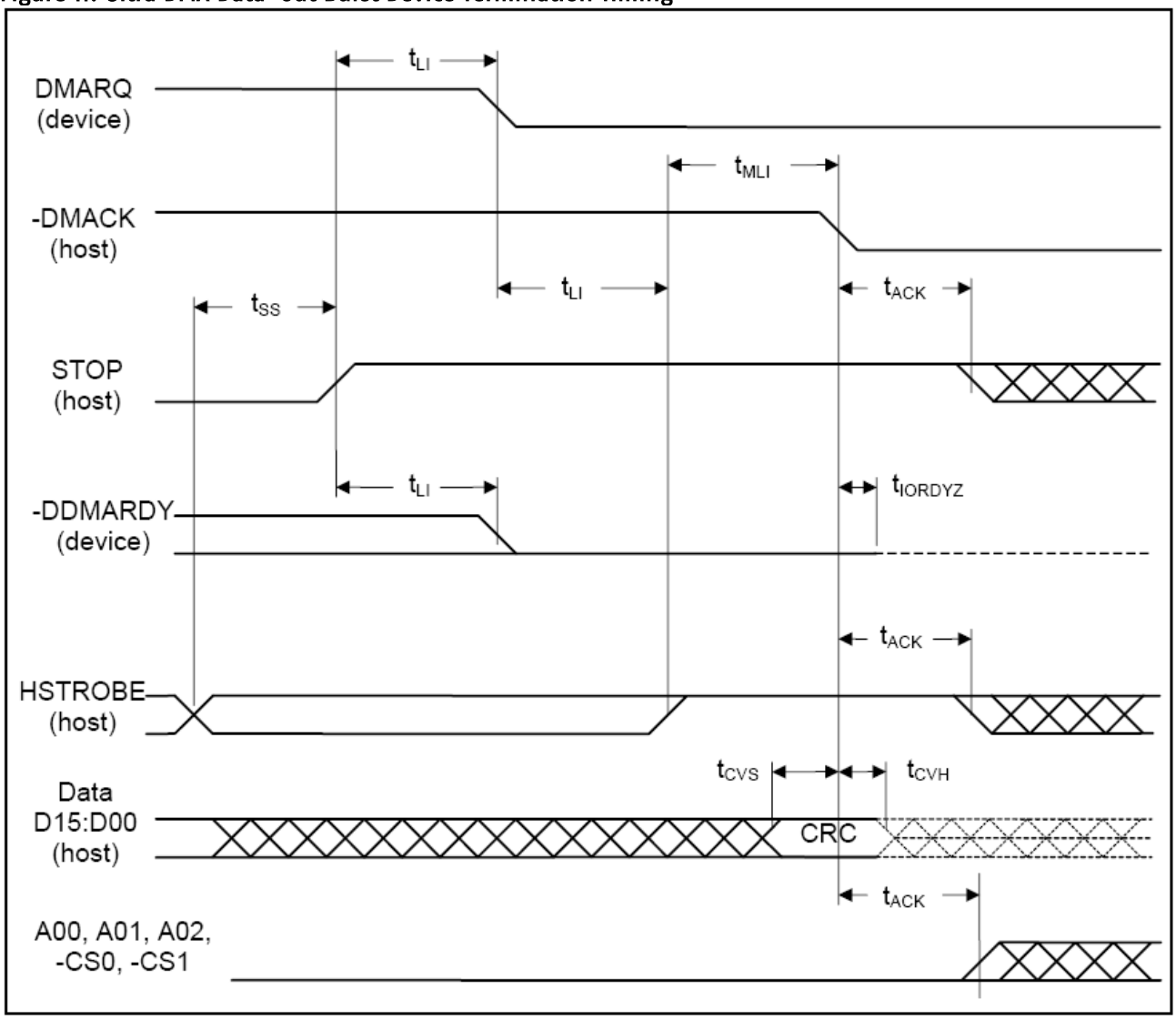
6.3.2.4.9 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 11: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
b) The device shall initiate Ultra DMA burst termination by negating -DDMARDY.
c) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating -DDMARDY.
d) If the device negates -DDMARDY within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than t_{SR} after the host has generated anHSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
e) The device shall negate DMARQ no sooner than t_{RP} after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
f) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
g) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h) The host shall place the result of its CRC calculation on D[15:00] (see 6.3.2.5).
i) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].
j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command.

Figure 11: Ultra DMA Data-Out Burst Device Termination Timing



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

6.3.2.4.10 Host Terminating an Ultra DMA Data-Out Burst

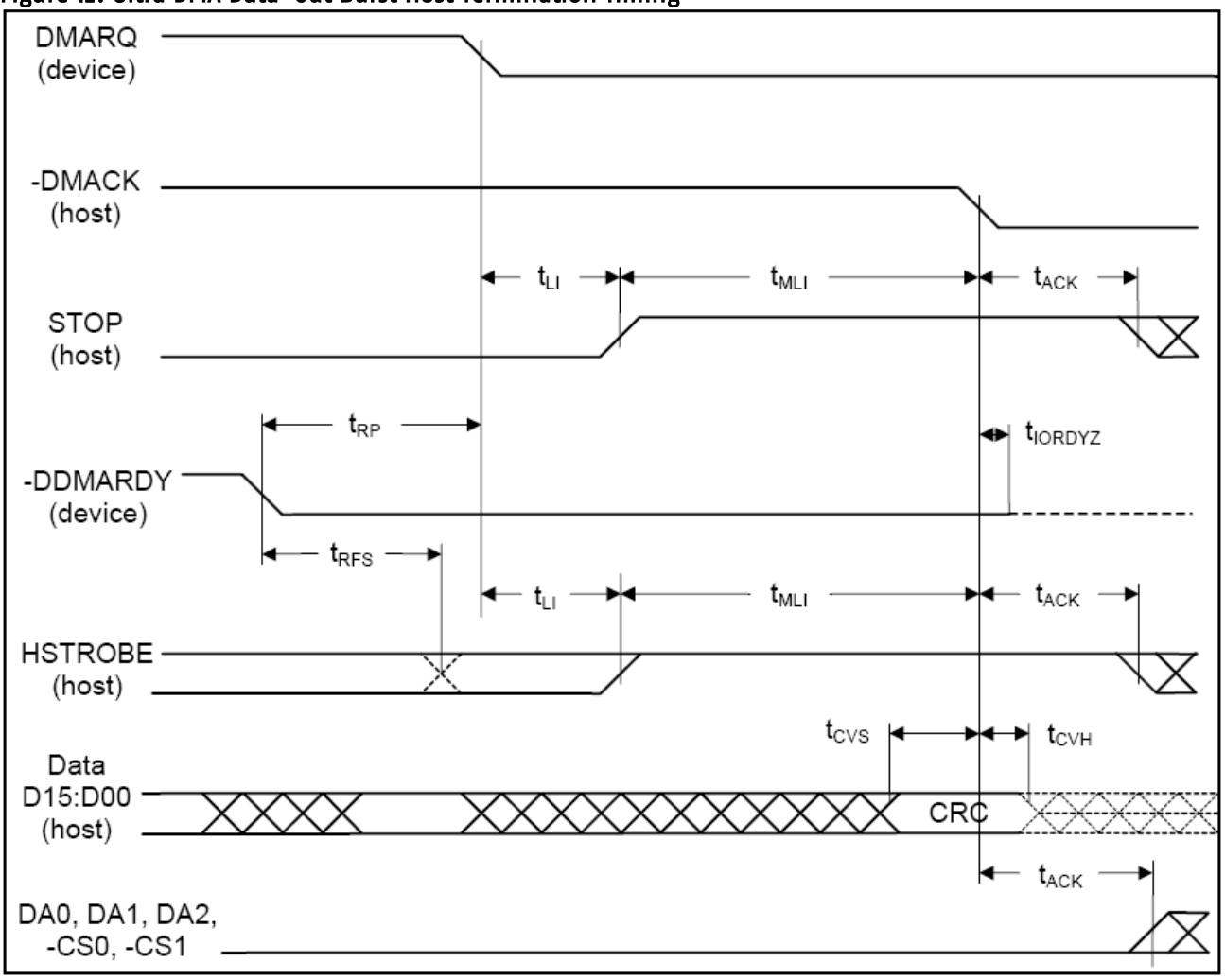
Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 12: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 23: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
b) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
c) The device shall negate DMARQ within tLI after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
d) The device shall negate -DDMARDY within t_{LI} after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.
e) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
f) The host shall place the result of its CRC calculation on D[15:00] (see 6.3.2.5).
g) The host shall negate -DMACK no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than t_{DVS} after placing the result of its CRC calculation on D[15:00].

h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 6.3.2.5).
j) The device shall release -DDMARDY within t_{IORDYZ} after the host has negated -DMACK.
k) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating -DMACK.
l) The host shall not assert -IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating -DMACK.

Figure 12: Ultra DMA Data-Out Burst Host Termination Timing



Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

6.3.2.5 Ultra DMA CRC Calculation

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

1. Both the host and the device shall have a 16-bit CRC calculation function.
2. Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
3. The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
4. For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
5. At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on D[15:00] with the negation of -DMACK.

6. The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
7. For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands:
   When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the "Interface CRC Error" bit. The host shall respond to this error by re-issuing the command.
8. For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.
9. For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.
   NOTE – If excessive CRC errors are encountered while operating in Ultra mode 2 or 1, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.
10. A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.
11. 11. The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 26 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).
    NOTE – Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where D00 is shifted in first and D15 is shifted in last.

Table 26: Equations for parallel generation of an Ultra DMA CRC

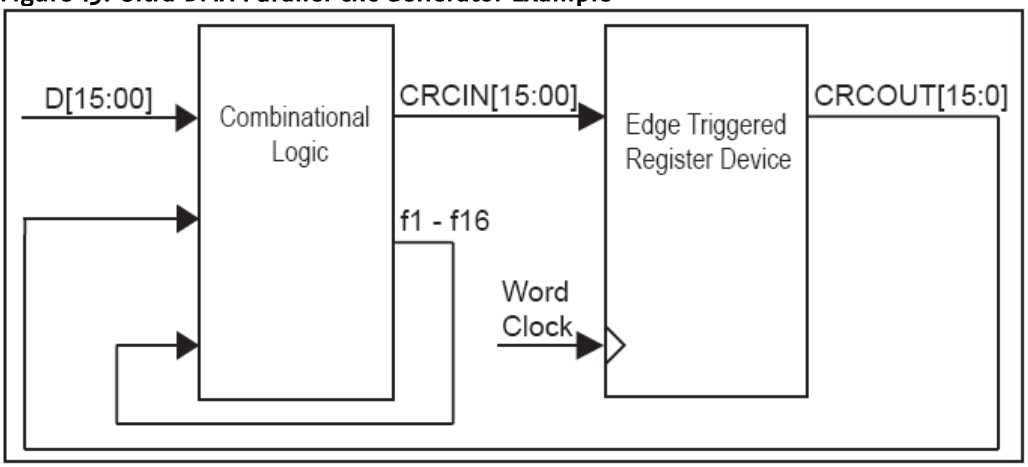
CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes:

1. f=feedback
2. D[15:0] = Data to or from the bus
3. CRCOUT = 16-bit edge triggered result (current CRC)
4. CRCOUT[15:0] are sent on matching order bits of D[15:00]

An example of a CRC generator implementation is provided below in Figure 13: Ultra DMA Parallel CRC Generator Example.

Figure 13: Ultra DMA Parallel CRC Generator Example



7 Software interface

The following section describes the hardware registers used by the host software to issue commands to the Drive.

7.1 ATA Drive Register Set Definition and Protocol

The drive can be used as a high performance I/O device through:

- Standard PC-AT disk I/O address spaces
  - 1F0h-1F7h, 3F6h-3F7h (primary);
  - 170h-177h, 376h-377h (secondary)

7.2 True IDE Mode Addressing

The Drive registers for reading and writing are specified in Table 27.

Table 27: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0
1	0	0	0	0	1	PIO RD Data	PIO WR Data
1	1	X	X	X	0	DMA RD Data	DMA WR Data
1	0	0	0	1	1	Error Register	Features
1	0	0	1	0	1	Sector Count	Sector Count
1	0	0	1	1	1	Sector No.	Sector No.
1	0	1	0	0	1	Cylinder Low	Cylinder Low
1	0	1	0	1	1	Cylinder High	Cylinder High
1	0	1	1	0	1	Select Card/Head	Select Card/Head
1	0	1	1	1	1	Status	Command
0	1	1	1	0	1	Alt Status	Control Register

7.3 Data Register

The Data register is located at address 1F0h [170h], offset 0h, 8h, and 9h.
The Data Register is a 16 bit register used to transfer data blocks between the Drive data buffer and the Host. This register overlaps the Error Register. Table 28 describes the combinations of Data register access and explain the overlapped Data and Error/Feature Registers. Because of the overlapped registers, access to the 1F1h, 171h or offset 1 are not defined for Word (-CS1 and –CS0 set to '0') operations, and are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed.

Table 28: Data Register Access (True IDE mode)

Data Register	-CS1	-CS0	A0	-DMACK	Offset	Data Bus
PIO Word Data Register	1	0	0	1	0h	D15 to D0
DMA Word Data Register	1	1	X	0	X	D15 to D0
PIO Byte Data Register (Selected Using Set Features Command)	1	0	0	1	0h	D7 to D0

7.4 Error Register

The Error register is a read-only register, located at address 1F1h [171h], offset 1h, 0Dh.
This read only register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined in Table 29 This register is accessed on data bits D15 to D8 during a write operation to offset 0 with –CS1 Low and –CS0 High.

7.4.1 Bit 7 (BBK)

This bit is set when a Bad Block is detected.

7.4.2 Bit 6 (UNC)

This bit is set when an Uncorrectable Error is encountered.

7.4.3 Bit 5
This bit is '0'.

7.4.4 Bit 4 (IDNF)
This bit is set if the requested sector ID is in error or cannot be found.

7.4.5 Bit 3
This bit is '0'.

7.4.6 Bit 2 (Abort)
This bit is set if the command has been aborted because of a Drive status condition (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

7.4.7 Bit 1
This bit is '0'.

7.4.8 Bit 0 (AMNF)
This bit is set when there is a general error.

Table 29: Error Register

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

7.5 Feature Register
The Feature register is a write-only register, located at address 1F1h [171h], offset 1h, Dh.
This write-only register provides information on features that the host can utilize. It is accessed on data bits D15 to D8 during a write operation to Offset 0 with –CS1 Low and –CS0 High.

7.6 Sector Count Register
The Sector Count register is located at address 1F2h [172h], offset 2h.
This register contains the number of sectors of data to be transferred on a read or write operation between the host and Drive. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request. The default value is 01h.

7.7 Sector Number (LBA 7-0) Register
The Sector Number register is located at address 1F3h [173h], offset 3h.
This register contains the starting sector number or bits 7 to 0 of the Logical Block Address (LBA), for any data access for the subsequent sector transfer command.

7.8 Cylinder Low (LBA 15-8) Register
The Cylinder Low register is located at address 1F4h [174h], offset 4h.
This register contains the least significant 8 bits of the starting cylinder address or bits 15 to 8 of the Logical Block Address.

7.9 Cylinder High (LBA 23-16) Register
The Cylinder High register is located at address 1F5h [175h], offset 5h.
This register contains the most significant bits of the starting cylinder address or bits 23 to 16 of the Logical Block Address.

7.10 Drive/Head (LBA 27-24) Register
The Driver/Head register is located at address 1F6h [176h], offset 6h.
The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined in Table 30.

7.10.1 Bit 7

This bit is set to '1'.

7.10.2 Bit 6 (LBA)

LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA is set to '0', Cylinder/Head/Sector mode is selected. When LBA is set to'1', Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

- LBA7–LBA0: Sector Number Register D7 to D0
- LBA15–LBA8: Cylinder Low Register D7 to D0
- LBA23–LBA16: Cylinder High Register D7 to D0
- LBA27–LBA24: Drive/Head Register bits HS3 to HS0

7.10.3 Bit 5

This bit is set to '1'.

7.10.4 Bit 4 (DRV)

DRV is the drive number. When DRV is '0', drive 0 is selected (Master). When DRV is '1', drive 1 is selected (Slave). The Drive is set to Drive 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

7.10.5 Bit 3 (HS3)

When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

7.10.6 Bit 2 (HS2)

When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

7.10.7 Bit 1 (HS1)

When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

7.10.8 Bit 0 (HS0)

When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

Table 30: Drive/Head Register

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

7.11 Status & Alternate Status Registers

The Status & Alternate Status registers are located at addresses 1F7h [177h] and 3F6h [376h], respectively. Offsets are 7h and Eh.
These registers return the Drive status when read by the host.
Reading the Status Register clears a pending interrupt. Reading the Auxiliary Status Register does not clear a pending interrupt.
The Status Register should be accessed in Byte mode; in Word mode it is recommended that Alternate Status Register is used. The status bits are described as follows

7.11.1 Bit 7 (BUSY)

The busy bit is set when only the Drive can access the command register and buffer, The host is denied access. No other bits in this register are valid when this bit is set to '1'.

7.11.2 Bit 6 (RDY)

This bit indicates whether the device is capable of performing Drive operations. This bit is cleared at power up and remains cleared until the Drive is ready to accept a command.

7.11.3 Bit 5 (DWF)

When set this bit indicates a Write Fault has occurred.

7.11.4 Bit 4 (DSC)

This bit is set when the Drive is ready.

7.11.5 Bit 3 (DRQ)

The Data Request is set when the Drive requires information be transferred either to or from the host through the Data register. The bit is cleared by the next command.

7.11.6 Bit 2 (CORR)

This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

7.11.7 Bit 1 (IDX)

This bit is always set to '0'.

7.11.8 Bit 0 (ERR)

This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. In case of read or write access commands that end with an error, the address of the first sector with an error is in the command block registers. This bit is cleared by the next command.

Table 31: Status & Alternate Status Register

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

7.12 Device Control Register

The Device Control register is located at address 3F6h [376h], offset Eh.
This Write-only register is used to control the Drive interrupt request and to issue an ATA soft reset to the Drive. This register can be written even if the device is BUSY. The bits are defined as follows:

7.12.1 Bit 7 to 3

Don't care. The host should reset this bit to '0'.

7.12.2 Bit 2 (SW Rst)

This bit is set to 1 in order to force the Drive to perform an AT Disk controller Soft Reset operation. This clears Status Register and writes Diagnostic Code in Error register after a Write or Read Sector error. The Drive remains in Reset until this bit is reset to '0.'

7.12.3 Bit 1 (-Ien)

When the Interrupt Enable bit is set to '0', -IREQ interrupts are enabled. When the bit is set to '1', interrupts from the Drive are disabled. This bit also controls the Int bit in the Drive Configuration and Status Register. It is set to '0' at Power On.

7.12.4 Bit 0

This bit is set to '0'.

Table 32: Device Control Register

D7	D6	D5	D4	D3	D2	D1	D0
X(0)	X(0)	X(0)	X(0)	X(0)	SW Rst	-Ien	0

7.13 Drive (Drive) Address Register

The Drive Address register is located at address 3F7h [377h], offset Fh.

This read-only register is provided for compatibility with the AT disk drive interface and can be used for confirming the drive status. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

7.13.1 Bit 7

This bit is don't care.

7.13.2 Bit 6 (-WTG)

This bit is '0' when a write operation is in progress; otherwise, it is '1'.

7.13.3 Bit 5 (-HS3)

This bit is the negation of bit 3 in the Drive/Head register.

7.13.4 Bit 4 (-HS2)

This bit is the negation of bit 2 in the Drive/Head register.

7.13.5 Bit 3 (-HS1)

This bit is the negation of bit 1 in the Drive/Head register.

7.13.6 Bit 2 (-HS0)

This bit is the negation of bit 0 in the Drive/Head register.

7.13.7 Bit 1 (-nDS1)

This bit is '0' when drive 1 is active and selected.

7.13.8 Bit 0 (-nDS0)

This bit is '0' when the drive 0 is active and selected.

Table 33: Drive Address Register

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

8 ATA command description

This section defines the software requirements and the format of the commands the Host sends to the Drive. Commands are issued to the Drive by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. There are three classes of command acceptance, all dependent on the host not issuing commands unless the Drive is not busy (BSY is '0').

- **Class 1:** Upon receipt of a Class 1 command, the Drive sets BSY within 400ns.
- **Class 2:** Upon receipt of a Class 2 command, the Drive sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 700µs, and clears BSY within 400ns of setting DRQ.
- **Class 3:**Upon receipt of a Class 3 command, the Drive sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 20ms (assuming no re-assignments), and clears BSY within 400ns of setting DRQ.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP. summarizes the Drive command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 34: ATA Command Set[1]

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h					D	
1	Erase Sector(s)	C0h		Y	Y	Y	Y	Y
1	Execute Drive Diagnostic	90h					D	
1	Flush cache	E7h					D	
2	Format track	50h		Y		Y	Y	Y
1	Identify Drive	ECh					D	
1	Idle	E3h or 97h		Y			D	
1	Idle Immediate	E1h or 95h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	Media Lock	DEh					D	
1	Media unlock	DFh					D	
1	NOP	00h					D	
1	Read Buffer	E4h					D	
1	Read DMA	C8		Y	Y	Y	Y	Y
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read native max address	F8h					D	
1	Read Sector(s)	20h or 21h		Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
1	Recalibrate	1Xh					D	
1	Request Sense	03h					D	
1	Security Disable Password	F6h					D	
1	Security Erase Prepare	F3h					D	
1	Security Erase Unit	F4h					D	
1	Security Freeze Lock	F5h					D	
1	Security Set Password	F1h					D	
1	Security Unlock	F2h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	EFh	Y				D	
1	Set max address	F9h		Y	Y	Y	Y	Y
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	E6h or 99h					D	
1	S.M.A.R.T.	B0h	Y	Y		Y	D	
1	Stand By	E2h or 96h					D	
1	Stand By Immediate	E0h or 94h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
2	Write Buffer	E8h					D	
2	Write DMA	CA		Y	Y	Y	Y	Y
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h		Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y

1. FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use), Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the Drive and head parameters are used. D – only the Drive parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

8.1 Check Power Mode (98h or E5h)

This command checks the power mode.
Issuing the command while the Drive is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.
Issuing the command when the Drive is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.
Table 35 defines the Byte sequence of the Check Power Mode command.

Table 35: Check Power Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h or E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.2 Erase Sector(s) (C0h)

This command is used to pre-erase and condition data sectors prior to a Write Sector without Erase command or a Write Multiple Without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur. Table 36 defines the Byte sequence of the Erase Sector command.

Table 36: Erase Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to erase							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to erase							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	nu							

8.3 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Drive.
The Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.
Table 37 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 38 are returned in the Error Register at the end of the command.

Table 37: Execute Drive Diagnostic

Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 38: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

8.4 Flush Cache (E7h)

This command causes the drive to complete writing data from its cache. The drive returns status with RDY=1 and DSC=1 after the data in the write cache buffer is written to the media. If the drive does not support the Flush Cache command, the drive shall return command aborted.

Table 39: Flush Cache

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E7h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.5 Format track (50h)

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the Drive expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the Drive. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

Table 40: Format track

Task File Register	7	6	5	4	3	2	1	0
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count (LBA only)							
FEATURES	nu							

8.6 Identify Device (ECh)

The Identify Device command enables the host to receive parameter information from the Drive. This command has the same protocol as the Read Sector(s) command. Table 41 defines the Identify Device command Byte sequence. All reserved bits or Words are zero. Table 42 shows the definition of each field in the Identify Drive Information.

Table 41: Identify Device

Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 42: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	**045Ah***	2	Standard Configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0200h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per Drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0002h	2	Buffer type (dual ported multi-sector)
21	0001h	2	Buffer Size in 512byte increment
22	0004h	2	# ECC bytes passed on Read/Write Long Commands
23-26	**YYYY***	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	**YYYY***	40	Model number in ASCII (right justified) Big Endian Byte Order in Word ("SFPAxxxxQxB0xT0-x-xx-xxx-xxx")
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double word not supported
49	**0F00h*** **0E00h***	2	Capabilities with DMA, LBA, IORDY supported without DMA LBA, IORDY supported
50	4001h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode 2
52	0000h	2	Obsolete
53	**0007h***	2	Field validity (Bytes 54-58, 64-70, 88)
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010Xh*	2	Multiple sector setting (can be changed by host).
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Obsolete
63	**0007h*** **0000h***	2	Multi-Word DMA transfer support and selection (can be changed by host). no multi-word DMA
64	0003h	2	Advanced PIO modes 3 and 4 supported
65	**0078h***	2	Minimum Multi-Word DMA transfer cycle time per Word.
66	**0078h***	2	Recommended Multi-Word DMA transfer cycle time.
67	**0078h***	2	Minimum PIO transfer cycle time without flow control
68	**0078h***	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0020h 0000h	4	ATA version 5
82 -84	740Bh* 5000h* 4000h*	6	Features/command sets supported
85-87	7409h* 1000h* 4000h*	6	Features/command sets enabled (can change in operation)
88	**101Fh***	2	Ultra DMA Mode Supported and Selected 0,1,2,3,4 (changes in operation)
89-91	0000h*	6	Reserved
92	**FFFE***	2	Master Password Revision Code
93	**XXXXh***	2	Hardware test result (changes in operation), if supported, esp. 40/80 cable detection
94-127	0000h*	68	Reserved
128	0XXXh	2	Security Status
129	XX00h	2	Write Protect Status. Bit 15 = permanent write protect, no more spare blocks
130-255	YYYYh	252	Vendor unique bytes / Reserved

* Standard values for full functionality, depending on configuration
XXXX Depending on drive capacity and drive geometry
YYYY Depending on drive configuration

8.6.1 Word 0: General Configuration

This field indicates the general characteristics of the device.
The default value for Word 0 is set to **045Ah**.
Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the drive as the root storage device.

8.6.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

8.6.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

8.6.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

8.6.5 Word 7-8: Number of Sectors per Drive

This field contains the number of sectors per Drive. This double Word value is also the first invalid address in LBA translation mode.

8.6.6 Word 10-19: Memory Drive Serial Number

The contents of this field are right justified and padded without spaces (20h).

8.6.7 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

8.6.8 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

8.6.9 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

8.6.10 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.
- Bit 11: IORDY Supported
  If bit 11 is set to 1 then this drive supports IORDY operation.
  If bit 11 is set to 0 then this drive may support IORDY operation.
- Bit 10: IORDY may be disabled
  If bit 10 is set to 1 then IODRDY may be disabled.
- Bit 9 LBA support: drive support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

8.6.11 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15-8: are set to 02H.

8.6.12 Word 53: Translation Parameter Valid

- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid
- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid
- Bit 2 shall be set to 1 indicating that word 88 is valid and reflects the supported True IDE UDMA

8.6.13 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

8.6.14 Word 57-58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

8.6.15 Word 59: Multiple Sector Setting

- Bits 15-9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7-0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

8.6.16 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Drive in LBA mode only.

8.6.17 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of word 63 of the Identify Device parameter information is defined as the Multiword DMA mode selected field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Only one of bits may be set to one in this field by the drive to indicate the multiword DMA mode which is currently selected.
Of these bits, bits 15 through 11 are reserved. Bit 8, if set to one, indicates that Multiword DMA mode 0 has been selected. Bit 9, if set to one, indicates that Multiword DMA mode 1 has been selected. Bit 10, if set to one, indicates that Multiword DMA mode 2 has been selected.
Selection of Multiword DMA modes 3 and above are specific to Drive are as described in Word 163.
Bits 7 through 0 of word 63 of the Identify Device parameter information is defined as the Multiword DMA data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the drive to indicate the Multiword DMA modes it is capable of supporting.
Of these bits, bits 7 through 2 are reserved. Bit 0, if set to one, indicates that the drive supports Multiword DMA mode 0. Bit 1, if set to one, indicates that the drive supports Multiword DMA modes 1 and 0. Bit 2, if set to one, indicates that the Drive supports Multiword DMA modes 2, 1 and 0.
Support for Multiword DMA modes 3 and above are specific to Drive are reported in word 163 as described in Word 163.

8.6.18 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the drive to indicate the advanced PIO modes it is capable of supporting.

1. Bits 7-2 are reserved for future advanced PIO modes.
2. Bit 1 is set to '1', indicates that the Drive supports PIO mode 4.
3. Bit 0 is set to '1' to indicate that the Drive supports PIO mode 3.

Support for PIO modes 5 and above are specific to Drive are reported in word 163 as described in Word 163.

8.6.19 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer.
If this field is supported, bit 1 of word 53 shall be set to one. The value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

8.6.20 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the cycle time that, if used by the host, may optimize the data transfer from by reducing the probability that the Drive will need to negate the DMARQ signal during the transfer of a sector.

If this field is supported, bit 1 of word 53 shall be set to one. The value in word 66 shall not be less than the value in word 65. This field shall be supported by all Drives supporting DMA modes 1 and above. If bit 1 of word 53 is set to one, but this field is not supported, the Drive shall return a value of zero in this field.

8.6.21 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the Drive guarantees data integrity during the transfer without utilization of flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

8.6.22 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the Drive supports while performing data transfers while utilizing IORDY flow control.
If this field is supported, Bit 1 of word 53 shall be set to one.
Any Drive that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the Drive.
If bit 1 of word 53 is set to one because a Drive supports a field in words 64-70 other than this field and the Drive does not support this field, the Drive shall return a value of zero in this field.

8.6.23 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported.
- If bit 1 of word 82 is set to one, the Security Mode feature set is supported.
- Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 82 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported.
- If bit 5 of word 82 is set to one, write cache is supported.
- If bit 6 of word 82 is set to one, look-ahead is supported.
- Bit 7 of word 82 shall be set to zero; release interrupt is not supported.
- Bit 8 of word 82 shall be set to zero; Service interrupt is not supported.
- Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 82 is obsolete.
- Bit 12 of word 82 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 82 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 82 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 82 is obsolete.

- Bit 0 of word 83 shall be set to zero; the Drive does not support the Download Microcode command.
- Bit 1 of word 83 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- Bit 2 of word 83 shall be set to zero; the Drive does not support the CFA feature set.
- If bit 3 of word 83 is set to one, the Drive supports the Advanced Power Management feature set.
- Bit 4 of word 83 shall be set to zero; the Drive does not support the Removable Media Status feature set.

8.6.24 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by Drives prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers.

- Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled.
- If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security
- Set Password command.
- Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported.
- Bit 3 of word 85 shall be set to one; the Power Management feature set is supported.
- Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled.
- If bit 5 of word 85 is set to one, write cache is enabled.
- If bit 6 of word 85 is set to one, look-ahead is enabled.
- Bit 7 of word 85 shall be set to zero; release interrupt is not enabled.
- Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled.
- Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported.
- Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported.
- Bit 11 of word 85 is obsolete.
- Bit 12 of word 85 shall be set to one; the Drive supports the Write Buffer command.
- Bit 13 of word 85 shall be set to one; the Drive supports the Read Buffer command.
- Bit 14 of word 85 shall be set to one; the Drive supports the NOP command.
- Bit 15 of word 85 is obsolete.
- Bit 0 of word 86 shall be set to zero; the Drive does not support the Download Microcode command.
- Bit 1 of word 86 shall be set to zero; the Drive does not support the Read DMA Queued and Write DMA Queued commands.
- If bit 2 of word 86 shall be set to zero, the Drive does not support the CFA feature set.
- If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command.
- Bit 4 of word 86 shall be set to zero; the Drive does not support the Removable Media Status feature set.

8.6.25 Word 88: True IDE Ultra DMA Modes Supported and Selected

Word 88 identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected. If a Multiword DMA mode is selected, then no Ultra DMA mode shall be selected. Support of this word is mandatory if Ultra DMA is supported. Word 88 shall return a value of 0 if the device is not in True IDE mode or if it does not support UDMA in True IDE Mode.

- Bit 15: Reserved
- Bit 14: 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
- Bit 13: 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
- Bit 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
- Bit 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
- Bit 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
- Bit 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
- Bit 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
- Bit 7: Reserved
- Bit 6: 1 = Ultra DMA mode 6 and below are supported. Bits 0-5 shall be set to 1.
- Bit 5: 1 = Ultra DMA mode 5 and below are supported. Bits 0-4 shall be set to 1.
- Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 shall be set to 1.
- Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 shall be set to 1.
- Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 shall be set to 1.
- Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 shall be set to 1.
- Bit 0: 1 = Ultra DMA mode 0 is supported

8.6.26 Word 93: Ultra DMA Modes Supported and Selected (if supported)

Word 93 shows Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset. Especially Bit 13 shows cable detection 1 80 cable or 0 40 cable.

- Bit 15 0 Shall be cleared to zero.
- Bit 14 1 Shall be set to one.
- Bit 13 1 = device detected CBLID- above ViH → 80 wired cable
  0 = device detected CBLID- below ViL
- Bit 12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero.
  Device 1 shall set these bits as follows:
- Bit 12 0 Reserved.
- Bit 11 0 = Device 1 did not assert PDIAG-
  1 = Device 1 asserted PDIAG-.
- Bit 10-9 These bits indicate how Device 1 determined the device number:
  00 = Reserved.
  01 = a jumper was used.
  10 = the CSEL signal was used.
  11 = some other method was used or the method is unknown.
- Bit 8 Shall be set to one.
- Bit 7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:
- Bit 7 Reserved.
- Bit 6 0 = Device 0 does not respond when Device 1 is selected.
  1 = Device 0 responds when Device 1 is selected.
- Bit 5 0 = Device 0 did not detect the assertion of DASP-.
  1 = Device 0 detected the assertion of DASP-.
  Bit 4 0 = Device 0 did not detect the assertion of PDIAG-.
  1 = Device 0 detected the assertion of PDIAG-.
- Bit 3 0 = Device 0 failed diagnostics.
  1 = Device 0 passed diagnostics.
- Bit 2-1 These bits indicate how Device 0 determined the device number:
  00 = Reserved.
  01 = a jumper was used.
  10 = the CSEL signal was used.
  11 = some other method was used or the method is unknown.
- Bit 0 Shall be set to one.

8.6.27 Word 128: Security status

Word 128 shall have the content described for word 128 of the IDENTIFY DEVICE command. Support of this word is mandatory if the Security feature set is supported.

- Bit 15-9 0 Reserved
- Bit 8 Security level 0 = High, 1 = Maximum
- Bit 7-6 0 Reserved
- Bit5 1 = Enhanced security erase supported
- Bit4 1 = Security count expired
- Bit3 1 = Security frozen
- Bit2 1 = Security locked
- Bit1 1 = Security enabled
- Bit0 1 = Security supported

8.7 Idle (97h or E3h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification. Table 43 defines the Byte sequence of the Idle command.

Table 43: Idle

Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h or E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Timer Count (5ms increments)							
FEATURES	nu							

8.8 Idle Immediate (95h or E1h)

This command causes the Drive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 44 defines the Idle Immediate command Byte sequence.

Table 44: Idle Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h or E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.9 Initialize Drive Parameters (91h)

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.
Table 45 defines the Initialize Drive Parameters command Byte sequence.

Table 45: Initialize Drive Parameters

Task File Register	7	6	5	4	3	2	1	0
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Number of Sectors per Track							
FEATURES	nu							

8.10 Media Lock/Media Unlock (DEh/DFh)

This command is effective an NOP command and always fails with the Drive returning command aborted. Table 46 defines the Byte sequence of the commands.

Table 46: Media Lock/Media Unlock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	DEh/DFh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.11 NOP (ooh)

This command always fails with the Drive returning command aborted. Table 47 defines the Byte sequence of the NOP command.

Table 47: NOP

Task File Register	7	6	5	4	3	2	1	0
COMMAND	ooh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.12 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Drive's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 48 defines the Read Buffer command Byte sequence.

Table 48: Read buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.13 Read DMA (C8h)

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The Drive asserts DMAREQ while data is available to be transferred. The host then reads the (512 * sector-count) bytes of data from the Drive using DMA. While DMAREQ is asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and
asserts -IORD once for each 16 bit word to be transferred to the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error.
At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The

Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.

Table 49: Read DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.14 Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.
Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Table 50 defines the Read Multiple command Byte sequence.

Table 50: Read Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C4h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.15 Read Native max address (F8h)

The Read Native max address command reads the max native address of the drive. It is related to the Host protected Area feature set. Table 51 defines the Read max native address command Byte sequence.

Table 51: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device. The native drive size is given in Drive/Head, Cyl Hi, Cyl Low and Sector num register as LBA value.

8.16 Read Sector(s) (20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Drive sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer. Table 52 defines the Read Sector command Byte sequence.

Table 52: Read sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h or 21h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.17 Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Drive sets BSY. When the requested sectors have been verified, the Drive clears BSY and generates an interrupt.
If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

Table 53 defines the Read Verify Sector command Byte sequence.

Table 53: Read Verify Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h or 41h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.18 Recalibrate (1Xh)

This command is effectively a NOP command to the Drive and is provided for compatibility purposes. Table 54 defines the Recalibrate command Byte sequence.

Table 54: Recalibrate

Task File Register	7	6	5	4	3	2	1	0

COMMAND	1Xh							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.19 Request Sense (03h)

This command requests extended error information for the previous command. Table 55 defines the Request Sense command Byte sequence. Table 56 defines the valid extended error codes. The extended error code is returned to the host in the Error Register.

Table 55: Request sense

Task File Register	7	6	5	4	3	2	1	0
COMMAND	03h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 56: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed

8.20 Security Disable Password (F6h)

This command requests a transfer of a single sector of data from the host. Table 57 defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 57: Security Disable Password

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F6h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 58: Security Password Data Content

Word	Content
0	Control word Bit 0: identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

8.21 Security Erase Prepare (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable device erasing and unlocking. This command prevents accidental erase of the SSD.

Table 59: Security Erase Prepare

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F3h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.22 Security Erase Unit (F4h)

This command requests transfer of a single sector of data from the host. Table 58 defines the content of this sector of information. If the password does not match the password previously saved by the SSD, the SSD rejects the command with command aborted. The Security Erase Prepare command shall be completed immediately prior to the Security Erase Unit command. If the SSD receives a Security Erase Unit command without an immediately prior Security Erase Prepare command, the SSD command aborts the Security Erase Unit command.

Table 60: Security Erase Unit

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F4h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.23 Security Freeze Lock (F5h)

The Security Freeze Lock command sets the SSD to Frozen mode. After command completion, any other commands that update the SSD Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If Security Freeze Lock is issued when the SSD is in Frozen mode, the command executes and the SSD remains in Frozen mode. After command completion, the Sector Count Register shall be set to 0.
Commands disabled by Security Freeze Lock are:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

If security mode feature set is not supported, this command shall be handled as Wear Level command.

Table 61: Security Freeze Lock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.24 Security Set Password (F1h)

This command requests a transfer of a single sector of data from the host. Table 63 defines the content of the sector of information. The data transferred controls the function of this command.
Table 64 defines the interaction of the identifier and security level bits.

Table 62: Security Set Password

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F1h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 63: Security Set Password Data Content

Word	Content
0	Control word Bit 0: identifier 0=set User password 1=set Master password Bit 1-7: Reserved Bit 8: Security level 0=High 1=Maximum Bits 9-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

Table 64: Identifier and Security Level Bit Interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The SSD shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The SSD shall then be unlocked by only the User password. The Master password previously set is still stored in the SSD shall not be used to unlock the SSD.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

8.25 Security Unlock (F2h)

This command requests transfer of a single sector of data from the host. Table 58 defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in the maximum security level, then the unlock command shall be rejected. If the identifier bit is set to user, then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when Security Unlock is issued and the device is locked. Once this counter reaches zero, the Security Unlock and Security Erase Unit commands are command

aborted until after a power-on reset or a hardware reset is received. Security Unlock commands issued when the device is unlocked have no effect on the unlock counter.

Table 65: Security Unlock

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F2h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.26 Seek (7Xh)

This command is effectively a NOP command to the Drive although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range. Table 66 shows the Seek command Byte sequence.

Table 66: Seek

Task File Register	7	6	5	4	3	2	1	0
COMMAND	7Xh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	nu (LBA7-0)							
SECTOR COUNT	nu							
FEATURES	nu							

8.27 Set Features (EFh)

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the SSD returns command aborted. Table 68 defines all features that are supported.

Table 67: Set Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	EFh							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Config							
FEATURES	Feature							

Table 68: Features Supported

Feature	Operation
01h/81h	Enable/Disable 8-bit data transfers.
02h/82h	Enable/Disable write cache.
03h	Set transfer mode based on value in Sector Count register.
05h/85h	Enable/Disable advance power management.
09h/89h	Enable/Disable extended power operations.
0Ah/8Ah	Enable/Disable power level 1 commands.
55h/AAh	Disable/Enable Read Look Ahead.
66h/CCh	Disable/Enable Power On Reset (POR) established of defaults at Soft Reset.
69h	NOP Accepted for backward compatibility.
96h	NOP Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows trade-off between current drawn and read/write speed.
BBh	4 bytes of data apply on Read/Write Long commands

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers shall occur on the low order D[7:0] data bus and the -IOIS16 signal shall not be asserted for data register accesses. The host shall not enable this feature for DMA transfers.
Features 02h and 82h allow the host to enable or disable write cache in SSD that implement write cache. When the subcommand disable write cache is issued, the SSD shall initiate the sequence to flush cache to non-volatile memory before command completion.
Feature 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Table 69: Transfer Mode Values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode(1)
Reserved	00010b	N/A
Multi-Word DMA mode	00100b	Mode(1)
Ultra DMA mode	01000b	Mode(1)
Reserved	1000b	N/A

(1)Mode = transfer mode number

Notes: Multiword DMA is not permitted for devices configured in the PC Card Memory or the PC Card I/O interface mode.

If a SSD supports PIO modes greater than 0 and receives a Set Features command with a Set Transfer Mode parameter and a Sector Count register value of "00000000b", it shall set its default PIO mode. If the value is "00000001b" and the SSD supports disabling of IORDY, then the SSD shall set its default PIO mode and disable IORDY. A SSD shall support all PIO modes below the highest mode supported, e.g., if PIO mode 1 is supported PIO mode 0 shall be supported.
Support of IORDY is mandatory when PIO mode 3 or above is the current mode of operation.
A SSD reporting support for Multiword DMA modes shall support all Multiword DMA modes below the highest mode supported. For example, if Multiword DMA mode 2 support is reported, then modes 1 and 0 shall also be supported. Note that Multiword DMA shall not be supported while PC Card interface modes are selected.
A SSD reporting support for Ultra DMA modes shall support all Ultra DMA modes below the highest mode supported. For example, if Ultra DMA mode 2 support is reported then modes 1 and 0 shall also be supported.
If an Ultra DMA mode is enabled, any previously enabled Multiword DMA mode shall be disabled by the device. If a Multiword DMA mode is enabled any previously enabled Ultra DMA mode shall be disabled by the device. Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a Set Features command with subcommand code 05h. The power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh.
Table 70: Advanced power management levels shows these values.

Table 70: Advanced power management levels

Level	Sector Count Value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	FFh
Reserved	00h

In the current version the advanced power management levels are accepted, but don't influence performance and power consumption.
Device performance may increase with increasing power management levels. Device power consumption may increase with increasing power management levels. The power management levels may contain discrete bands. For example, a device may implement one power management method from 80h to A0h and a higher performance, higher power consumption method from level A1h to FEh. Advanced power management levels 80h and higher do not permit the device to spin down to save power.

Feature 85h disables Advanced Power Management. Subcommand 85h may not be implemented on all devices that implement Set Features subcommand 05h.
Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the SSD with extended power as they require Power Level 1 to perform their full set of functions. Power Enhanced SSD are required to power up and execute all supported commands and protocols in Power Level 0, their default feature shall be 8Ah: Disable Power Level 1 Commands. No commands are actually excluded for such cards in Power Level 0 because no commands require Power Level 1.
Features 55h and BBh are the default features for the SSD; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.
Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register were set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card shall accept values outside this programmable range, but shall operate at either the lowest power or highest performance as appropriate.
Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults shall be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

8.28 Set max address (F9h)

The Set max address command sets the max address of the drive. It is related to the Host protected Area feature set. Table 71 defines the Set max address command Byte sequence.

Table 71: Read native max address

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F8h							
DRIVE/HEAD	nu	LBA	nu	D	Set max LBA (27:24)			
CYLINDER HI	Set max LBA (23:16)							
CYLINDER LOW	Set max LBA (15:8)							
SECTOR NUM	Set max LBA (7:0)							
SECTOR COUNT	nu							VV
FEATURES	nu							

The LBA bit shall be set to one to specify the address is an LBA. DEV shall specify the selected device.

VV =Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hardware reset. If bit 0 is cleared to zero, the device shall revert to the most recent nonvolatile maximum address value setting over power-up or hardware reset.

Typical use of the Set max address (F9h) and Read native max address (F8h) commands would be:

On reset
BIOS receives control after a system reset;
1. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
2. BIOS issues a SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
3. BIOS reads configuration data from the highest area on the disk;
4. BIOS issues a READ NATIVE MAX ADDRESS command followed by a SET MAX ADDRESS command to reset the device to the size of the file system.

On save to disk
1. BIOS receives control prior to shut down;
2. BIOS issues a READ NATIVE MAX ADDRESS command to find the max capacity of the device;
3. BIOS issues a volatile SET MAX ADDRESS command to the values returned by READ NATIVE MAX ADDRESS;
4. Memory is copied to the reserved area;
5. Shut down completes;
6. On power-on or hardware reset the device max address returns to the last non-volatile setting.

These commands are intended for use only by system BIOS or other low-level boot time process.

Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device. Devices should return command aborted if a subsequent non-volatile SET MAX ADDRESS command is received after a power-on or hardware reset.

8.29 Set Multiple Mode (C6h)

This command enables the Drive to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the Drive sets BSY and checks the Sector Count Register.
If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains '0' when the command is issued, Read and Write Multiple commands are disabled. At power on the default mode is Read and Write Multiple disabled, unless it is disabled by a Set Feature command. Table 72 defines the Set Multiple Mode command Byte sequence.

Table 72: Set Multiple Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.30 Set Sleep Mode (99h or E6h)

This command causes the Drive to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command. Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5ms) is different from the ATA Specification. Table 73 defines the Set Sleep Mode command Byte sequence.

Table 73: Set Sleep Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h or E6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.31 S.M.A.R.T. (Boh)

The intent of self-monitoring, analysis, and reporting technology (the SMART feature set) is to protect user data and minimize the likelihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in the IDENTIFY DEVICE data (Word 82 bit 0).

Table 74: S.M.A.R.T. Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	XXh							
FEATURES	Feature							

Details of S.M.A.R.T. features are described in Section 9.

8.32 Standby (96h or E2)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command. Table 75 defines the Standby command Byte sequence.

Table 75: Standby

Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h or E2h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.33 Standby Immediate (94h or E0h)

This command causes the Drive to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.
Recovery from Sleep mode is accomplished by issuing another command. Table 76 defines the Standby Immediate Byte sequence.

Table 76: Standby Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	94h or E0h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.34 Translate Sector (87h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a '00h' indicating Translate Sector is not needed.
Table 77 defines the Translate Sector command Byte sequence.

Table 77: Translate Sector

Task File Register	7	6	5	4	3	2	1	0
COMMAND	87h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	nu (LBA7-0)							
SECTOR COUNT	nu							
FEATURES	nu							

8.35 Wear Level (F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 'ooh' indicating Wear Level is not needed.
defines the Wear Level command Byte sequence.

Table 78: Wear level

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Completion Status							
FEATURES	nu							

8.36 Write Buffer (E8h)

The Write Buffer command enables the host to overwrite contents of the Drive's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes.
Table 79 defines the Write Buffer command Byte sequence.

Table 79: Write Buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

8.37 Write DMA (CAh)

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the Drive sets BSY, puts all or part of the sector of data in the buffer. The Drive is then permitted, although not required, to set DRQ, clear BSY. The Drive asserts DMAREQ while data is available to be transferred. The host then writes the (512 * sector-count) bytes of data to the Drive using DMA. While DMAREQ is asserted by the Drive, the Host asserts -DMACK while it is ready to transfer data by DMA and asserts -IOWR once for each 16 bit word to be transferred from the Host.
Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector written. If an error occurs, the write terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The amount of data transferred is indeterminate.
When a Write DMA command is received by the Drive and 8 bit transfer mode has been enabled by the Set Features command, the Drive shall return the Aborted error.

Table 80: Write DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	CAh							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.38 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The Drive sets BSY within 400ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.
DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.
When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.
Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.
The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command. For example, each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.
Note: The current revision of the Drive only supports a block count of 1 as indicated in the Identify Drive Command information. The Write Multiple command is provided for compatibility with future products which may support a larger block count.
Table 81 defines the Write Multiple command Byte sequence.

Table 81: Write Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.39 Write Multiple without Erase (CDh)

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. Table 82 defines the Write Multiple without Erase command Byte sequence.

Table 82: Write Multiple without Erase

Task File Register	7	6	5	4	3	2	1	0
COMMAND	CDh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.40 Write Sector(s) (30h or 31h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Drive sets BSY, sets DRQ and clears BSY, then waits for the host to fill the sector

buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.
For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. Table 83 defines the Write Sector(s) command Byte sequence.

Table 83: Write Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h or 31h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.41 Write Sector(s) without Erase (38h)

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased a normal write sector operation will occur. Table 84 defines the Write Sector(s) without Erase command Byte sequence.

Table 84: Write Sector(s) without Erase

Task File Register	7	6	5	4	3	2	1	0
COMMAND	38h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

8.42 Write Verify (3Ch)

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command. Table 85 defines the Write Verify command Byte sequence.

Table 85: Write Verify

Task File Register	7	6	5	4	3	2	1	0
COMMAND	3Ch							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

9 S.M.A.R.T. Functionality

The SSD support the following SMART commands, determined by the Feature Register value.

Table 86: S.M.A.R.T. Features Supported

Feature	Operation
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute
D8h	SMART Enable Operations
D9h	Autosave SMART Disable Operations
DAh	SMART Return Status

SMART commands with Feature Register values not mentioned in the above table are not supported, and will be aborted.

9.1 S.M.A.R.T. Enable / Disable operations

This command enables / disables access to the SMART capabilities of the SSD.
The state of SMART (enabled or disabled) is preserved across power cycles.

Table 87: S.M.A.R.T. Enable / Disable operations (Feature D8h / D9h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D8h / D9h							

9.2 S.M.A.R.T. Enable / Disable Attribute Autosave

This command is effectively a no-operation as the data for the SMART functionality is always available and kept current in the SSD.

Table 88: S.M.A.R.T. Enable / Disable Attribute Autosave (Feature D0h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	00h or F1h							
FEATURES	D2h							

9.3 S.M.A.R.T. Read data

This command returns one sector of SMART data.

Table 89: S.M.A.R.T. read data (Feature D0h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D0h							

The data structure returned is:

Table 90: S.M.A.R.T. Data Structure

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364..365	0000h	Total time to complete off-line data collection
366	00h	
367	00h	Off-line data collection capability (no off-line data collection)
368..369	0003h	SMART capabilities
370	00h	Error logging capability (no error logging)
371	00h	
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374..385	00h	Reserved
386..387	0002h	SMART Swissbit Structure Version
388..391		"Commit" counter
392..395		Wear Level Threshold
396		Global Wear Leveling active
397		Global Bad Block Management active
398..510	00h	
511		Data structure checksum

The byte order for the multi-byte values is little endian (least significant byte first), unless specified otherwise.

There are six attributes that are defined in the SSD. These return their data in the attribute section of the SMART data, using a 12 byte data field.
The field at offset 386 gives a version number for the contents of the SMART data structure.
In version 0, the spare block counts (offsets 4 to 11) in the Spare Block Count attribute need to be byte-swapped.
In versions 0 and 1, the information at offsets 396 and 397 is not available.
The byte at offset 396 is 0 if the wear leveling has not yet started its global operation, and 1 if the global wear leveling has started. This happens when the most used chip has reached the erase count threshold (typically 100 000 erase cycles).
The byte at offset 397 is 0 if the bad block management is still working chip local, and 1 if the global bad block management has started. This happens when one of the flash chips runs out of spare blocks, in this case spare blocks from different flash chips are used.

9.3.1 Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

Table 91: Spare Block Count Attribute

Offset	Value	Description
0	C4h	Attribute ID – Reallocation Count
1..2	0003h	Flags – Pre-fail type, value is updated during normal operation
3		Attribute value. The value returned here is the minimum percentage of remaining spare blocks over all flash chips, i.e. min over all chips (100 × current spare blocks / initial spare blocks)
4..5		initial number of spare blocks of the flash chip that has been used for the attribute value calculation
6..7		current number of spare blocks of the flash chip that has been used for the attribute value calculation
8..9		sum of the initial number of spare blocks for all flash chips
10..11		sum of the current number of spare blocks for all flash chips

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold, the SMART Return Status command will indicate a threshold exceeded condition.

9.3.2 Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

Table 92: Erase Count Attribute

Offset	Value	Description
0	E5h	Attribute ID – Erase Count Usage (vendor specific)
1..2	0002h	Flags –Advisory type, value is updated during normal operation
3		Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block.
4..11		Estimated total number of block erases

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold, the SMART Return Status command will indicate a threshold exceeded condition.

9.3.3 Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 93: Total ECC Errors Attribute

Offset	Value	Description
0	CBh	Attribute ID – Number of ECC errors
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of ECC errors (correctable and uncorrectable)
8..11		-

9.3.4 Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 94: Correctable ECC Errors Attribute

Offset	Value	Description
0	CCh	Attribute ID – Number of corrected ECC errors
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of correctable ECC errors
8..11		-

9.3.5 Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. This can be useful for the interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

Table 95: Total Number of Reads Attribute

Offset	Value	Description
0	E8h	Attribute ID – Number of Reads (vendor specific)
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..11		Total number of flash read commands

9.3.6 UDMA CRC Errors Attribute

This attribute gives information about the total number of UDMA CRC errors that have occurred on flash read commands. This attribute is not used for the SMART Return Status command.

Table 96: UDMA CRC Errors Attribute

Offset	Value	Description
0	C7h	Attribute ID – UDMA CRC error rate
1..2	0002h	Flags – Advisory type, value is updated during normal operation
3	64h	Attribute value. This value is fixed at 100.
4..7		Total number of UDMA CRC errors
8..11		-

9.4 S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute thresholds.

Table 97: S.M.A.R.T. read data (Feature D1h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	D1h							

The data structure returned is:

Table 98: S.M.A.R.T. Data Structure

Offset	Value	Description
0..1	0004h	SMART structure version
2..361		Attribute threshold entries 1 to 30 (12 bytes each)
362..379	00h	Reserved
380..510	00h	-
511		Data structure checksum

Table 99: Spare Block Count Attribute Threshold

Offset	Value	Description
0	C4h	Attribute ID – Reallocation Count
1		Spare Block Count Threshold
2..11	00h	Reserved

Table 100: Erase Count Attribute Threshold

Offset	Value	Description
0	E5h	Attribute ID – Erase Count Usage (vendor specific)
1		Erase Count Threshold
2..11	00h	Reserved

Table 101: Total ECC Errors Attribute Threshold

Offset	Value	Description
0	CBh	Attribute ID – Number of ECC errors
1	00h	No threshold for the Total ECC Errors Attribute
2..11	00h	Reserved

Table 102: Correctable ECC Errors Attribute

Offset	Value	Description
0	CCh	Attribute ID – Number of corrected ECC errors
1	00h	No threshold for the Correctable ECC Errors Attribute
2..11	00h	Reserved

Table 103: Total Number of Reads Attribute

Offset	Value	Description
0	E8h	Attribute ID – Number of Reads (vendor specific)
1	00h	No threshold for the Total Number of Reads Attribute
2..11	00h	Reserved

Table 104: UDMA CRC Errors Attribute

Offset	Value	Description
0	C7h	Attribute ID – UDMA CRC error rate
1	00h	No threshold for the UDMA CRC Errors Attribute
2..11	00h	Reserved

9.5 S.M.A.R.T. Return Status

This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

Table 105: S.M.A.R.T. read data (Feature D1h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	DAh							

9.6 S.M.A.R.T. Read Remap Data

This command returns one sector of spare block information. The information is the initial number of blocks (directly after the preformat) per flash chip available for bad block remap, and the current number of blocks per flash chip available for bad block remap.

Table 106: S.M.A.R.T. read remap data (Feature E0h)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	B0h							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	01h							
FEATURES	E0h							

The layout of the returned sector is:

Table 107: Replacement block information

Offset	Value	Description
0..31		Initial number of replacement blocks for chips 0..15, 2 bytes per entry
32..63		Current number of replacement blocks for chips 0..15, 2 bytes per entry
64..511		Reserved

9.7 S.M.A.R.T. Read Wear Level Data

This command returns four sectors of information regarding the status of the wear leveling. The information returned is the distribution of the blocks into the 1024 possible wear level classes. For each of the wear level classes, the number of blocks that have this class is returned in the data sectors.

Table 108: S.M.A.R.T. read remap data (Feature Eoh)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Boh							
DRIVE/HEAD	1	1	1	D	nu			
CYLINDER HI	C2h							
CYLINDER LOW	4Fh							
SECTOR NUM	nu							
SECTOR COUNT	04h							
FEATURES	E1h							

The layout of the returned sectors is, with n the sector number from 0 to 3:

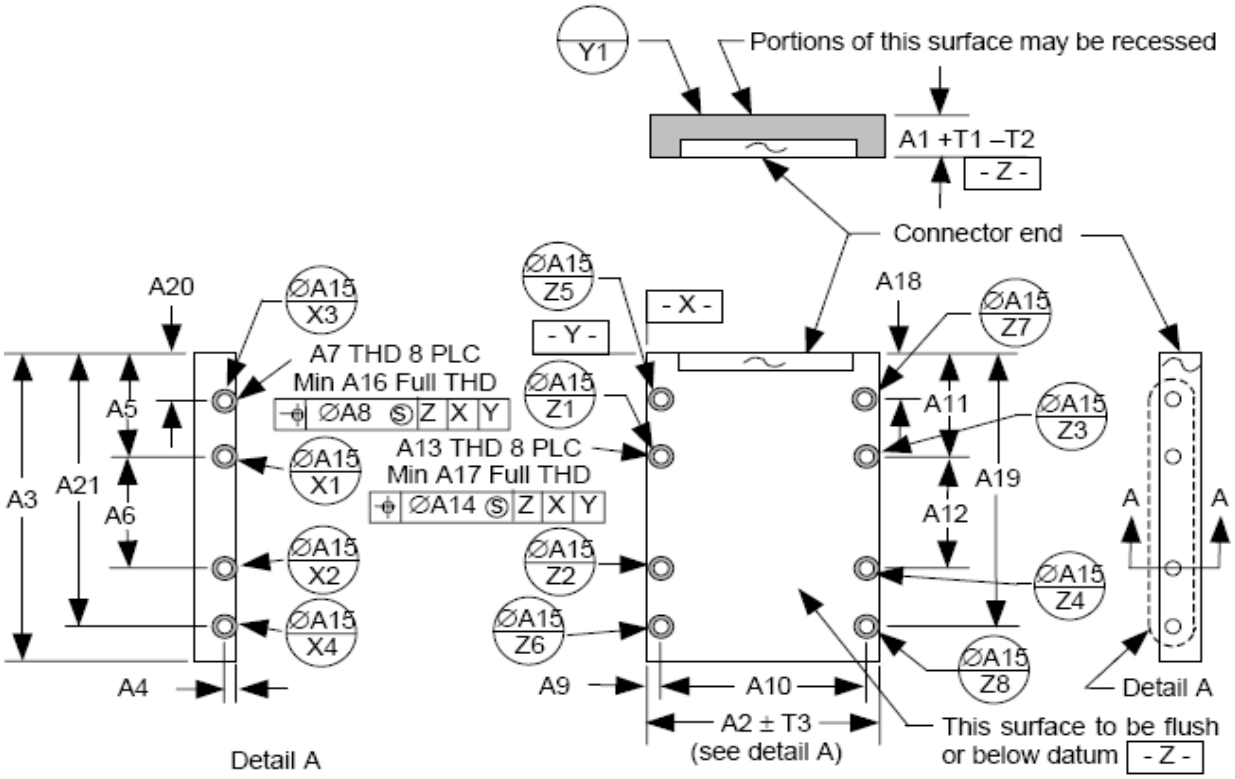
Table 109: Replacement block information

Offset	Value	Description
0..1		Number of flash blocks that have wear level class 256*n+0
2..3		Number of flash blocks that have wear level class 256*n+1
...		...
508..509		Number of flash blocks that have wear level class 256*n+254
510..511		Number of flash blocks that have wear level class 256*n+255

i.e. the first sector returns the information for wear level classes 0 to 255, the second sector returns the information for wear level classes 256 to 511, and so on.
A block moves from one wear level class into the next when it reaches the number of erases that is specified as the "Wear Level Threshold" in the preformat. A common threshold number is 4095, this means that blocks in wear level class 0 have seen 0 to 4095 erases, blocks in wear level class 1 have seen 4096 to 8191 erases, and so on. Using this information, statements about the wear of the card, and of the estimated remaining life can be made. The useful range of wear level classes is 0 to 1022, class 1023 has blocks that are not subject to wear leveling, like the Anchor block.

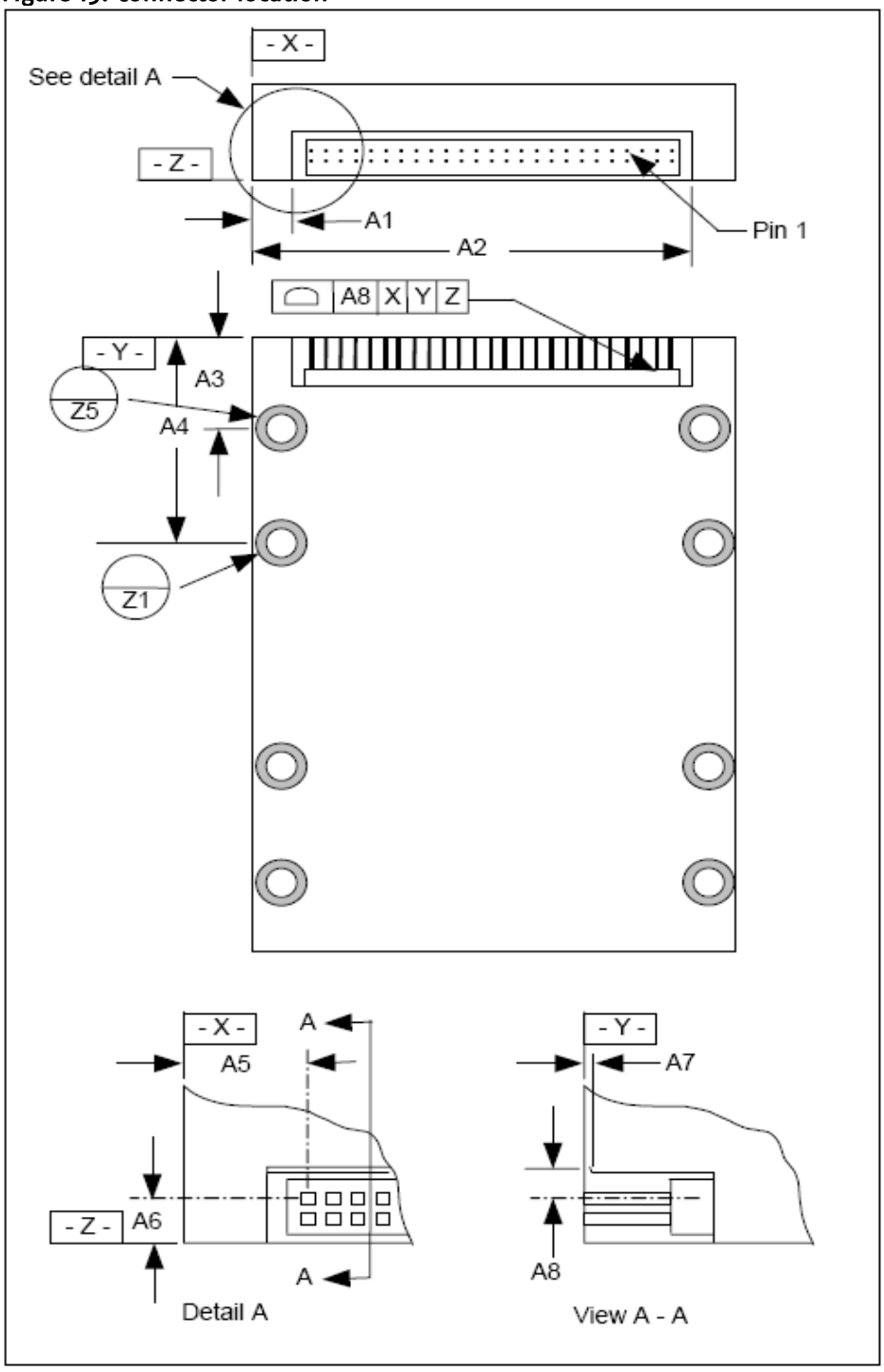
10 Package mechanical

Figure 14: SSD Drive Dimensions



Dimension		mm	inches
Height	A1	9.0	0.354
Width	A2	69.9	2.752
Max. Length	A3	100.30	3.94
Hole height	A4	3.0	0.118
2. hole	A5	34.9	1.375
3. hole	A6	38.1	1.5
	A7	n/a	n/a
	A8	0.5	0.02
Hole position	A9	4.1	0.16
Hole distance	A10	61.7	2.43
2. hole	A11	34.9	1.375
3. hole	A12	38.1	1.5
	A13	n/a	n/a
	A14	0.05	0.02
Screw head diameter	A15	6.0	0.315
Hole depth bottom	A16 min	5.0	0.2
Hole depth side	A17 min	5.0	0.2
1. hole	A18	14.0	0.551
4. hole	A19	90.6	3.567
1. hole	A20	14.0	0.551
4. hole	A21	90.6	3.567
+Height tolerance	T1	0.1	0.005
-Height tolerance	T2	0.25	0.01
Width tolerance	T3	0.25	0.01

Figure 15: Connector location



Dimension	mm	inches
A1	5.5	0.216
A2	65.0	2.559
A3	14.0	0.551
A4	34.9	1.374
A5	10.1	0.399
A6	4.0	0.157
A8	min 3.5	min 0.138

11 Declaration of Conformity

Product Type:	Solid State Drive (SSD)
Brand Name:	SWISSMEMORY™ SSD
Model Designation:	SFPAxxxxQxxxxxx-x-xx-xxx-xxx
Manufacturer:	Swissbit AG Industriestrasse 4 CH-9552 Bronschhofen Switzerland

The product complies with the requirements of the following directives:

CENELEC EN 55022B :2000 + CISPR22B :2000
CENELEC EN 55024 :2001 + CISPR24 :2001
FCC47 Part 15 Subpart B

The product was tested according all EMC requirements necessary for CE-mark

Year of the first marking: 2009

Silvio Muschter
Vice President
Engineering & Development

Bronschhofen, August 2009

12 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that Solid State Drives must comply with both Directives in order for them to be sold on the European market:

- **RoHS** – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2002/96/EC)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space. «In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty» (WEEE Directive 2002/96/EC)

When does the WEEE Directive take effect?

The Directive came into effect internationally on 13 August, 2005.

What is RoHS (2002/95/EC)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of 1 July, 2006, only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

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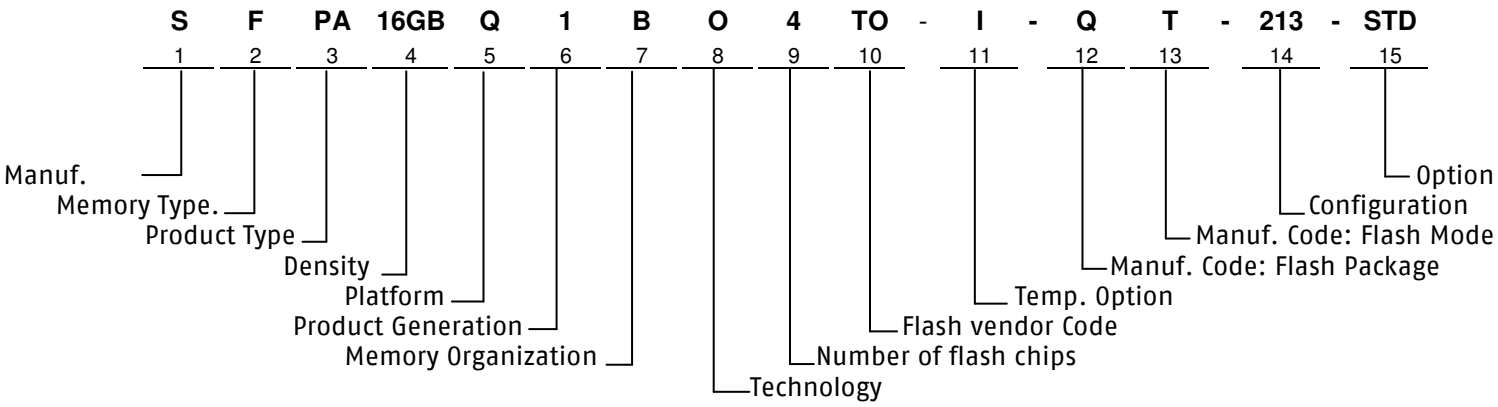
CH-9552 Bronschhofen
Tel: +41 71 913 03 03 – Fax: +41 71 913 03 15
E-mail: info@swissbit.com – Website: www.swissbit.com

13 Part Number Decoder



13.1 Manufacturer

Swissbit code	S

13.2 Memory Type

Flash	F

13.3 Product Type

Parallel ATA SSD	PA

13.4 Density

4 GByte	4096
8 GByte	8192
16 GByte	16GB
32 GByte	32GB

13.5 Platform

2.5'' SSD	Q

13.6 Product Generation

13.7 Memory Organization

x8	B

13.8 Technology

P-110 series		0

13.9 Number of Flash Chip

1 Flash	1
2 Flash	2
4 Flash	4
8 Flash	8

13.10 Flash Code

Samsung	SA
Intel	IT
Toshiba	T0

13.11 Temp. Option

Industrial Temp. Range -40°C – 85°C	I
Standard Temp. Range 0°C – 70°C	C

13.12 DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q

13.13 PIN Mode

Normal nCE & R/nB	0 or S
Dual nCE & Dual R/nB	1 or T

13.14 Drive configuration XYZ

X→ SSD Mode

Drive Mode	PIO	DMA support	X
Fix	yes	yes	2
Fix	yes	no	3

Y → Firmware Revision

FW Revision	Y
Standard	1

Z → max. transfer mode

Max PIO Mode / CIS	Z
PIO4 (if DMA support disabled)	1
UDMA4 (MDMA2, PIO4)	3

13.15 Option

Swissbit / Standard	STD

14 Swissbit SSD Marking specification

14.1 Top view

Industrial Drive

14.1.1 Label content:

- Swissbit logo
- Density
- Master/Slave Pin description
- CE logo
- FCC logo
- Pb-free logo
- WEEE logo
- Part number
- Assembly lot information
- Made in Germany
- Manufacturing Date

15 Revision History

Table 110: Document Revision History

Date	Revision	Revision Details
28-September-2010	1.00	Initial release