

QF1D512

Simple and versatile FIR engine (SavFIRe™)

APPLICATIONS

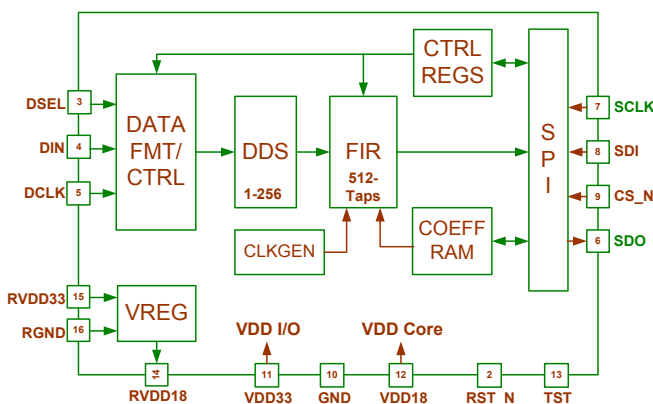
- Industrial Control
- Machine Monitoring
- Smart Sensors
- Medical Monitoring and Diagnostics
- Industrial Wireless Sensor Networks
- Homeland Security

DESCRIPTION

A single channel, programmable digital filter designed for near seamless insertion in the serial data path of a digital signal or used as an FIR coprocessor. The device can be programmed using the Quickfilter Pro™ Design Software which supports most FIR digital filter configurations. The FIR filter has 512 taps capable of generating “brick wall” filters such as a low pass filter with a 1 kHz cutoff frequency and a total transition band of only 25 Hz. The filter can operate over a broad range of ADC data rates - from 10sps up to 400kps and can support ADC’s with resolutions ranging from 12 to 24 bits.

ORDERING INFORMATION

Device	Package
QF1D512-QN-T	16-Pin QFN - Tape & Reel (Reel qty 1000)
QF1D512-QN-B	- Trays
QF1D512-DK	Development Kit



FEATURES

- Maximum 512-tap symmetric or 256-tap non-symmetric digital FIR filter with 12 – 24 bit data words and up to 32 bit coefficients
- Programmable Averaging and Down-sampler pre-FIR, including bypass mode
- Re-programmable in circuit
- Data Rate: Up to 400kps
- Data Interface: Supports SPI and synchronous serial modes up to 20 MHz, operates with a wide variety of ADC’s.
- SPI Configuration Interface support all 4 modes
- Multiple devices can be daisy chained, with programmable bypass mode.
- 3.3V Digital I/O, 5 Volt Tolerant with 3.3V & 1.8V Supplies, Internal regulator for single rail operation
- Low Power: < 1mW @ 1 Ksps, 10mW @ 200Ksps
- Industrial Temp -40C to +85C
- Package: 16-pin QFN (3 X 3 mm)

QUICKFILTER DEVELOPMENT KIT

(QF1D512-DK)

- Windows® Based Software for Rapid Filter Design and IC Configuration
- In-System Programmability (ISP) Through SPI Port
- Evaluation board for verification of device performance



TABLE OF CONTENTS

1	SPECIFICATIONS	4
1.1	Absolute Maximum Ratings	4
1.2	Package Assembly	4
1.3	Recommended Operating Conditions	4
1.4	Typical Performance Characteristics	4
1.5	Electrical Characteristics	5
1.6	Timing Requirements	5
1.6.1	GENERAL TIMING REQUIREMENTS	5
1.6.2	SPI CONFIGURATION TIMING REQUIREMENTS	6
1.6.3	DATA PATH TIMING REQUIREMENTS	7
2	PINOUT AND PIN DESCRIPTIONS	8
3	GENERAL DESCRIPTION	9
3.1	Data Format and Control	9
3.2	Averaging and Down-sampler	9
3.3	Finite Impulse Response filter (FIR)	9
3.4	Serial Interface - Serial Peripheral Interface (SPI)	9
3.5	Voltage Regulator	10
4	SOFTWARE	10
4.1	Device Configuration	10
4.2	Quickfilter Development Kit (QF1D512-DK)	10
5	CONFIGURATION INTERFACE	10
5.1	Native SPI Mode of Operation	10
5.2	Native SPI Configuration Mode Data Format	11
5.3	I2C Mode of Operation	12
5.4	I2C Configuration Mode Data Format	13
5.5	Sending Commands in Filter Mode	14
6	DATA INTERFACE	15
6.1	Modes of Operation	15
6.2	Data Passthrough	17
6.3	SDO Functionality	18
7	AVERAGING AND DOWNCONVERTER	19
7.1	Modes of Operation	19
8	FIR FILTER	19
8.1	Modes of Operation	19
8.2	FIR Latency	19
9	VOLTAGE REGULATOR	20
9.1	Mode of Operation	20

10 CONTROL REGISTERS	21
10.1 Overview	21
10.2 Configuration Registers	22
10.3 Coefficient Memory.....	30
11 OPERATING MODE CONFIGURATIONS.....	31
11.1 SPI FIR Coprocessor Mode.....	31
11.2 Inline Normal SPI Mode	31
11.3 Inline Continuous SPI Mode (CS_N tied to GND).....	32
11.4 Inline Synchronous Serial Mode (uP clock slave)	32
11.5 Inline SPI DAC	33
11.6 ADC Configuration Read / Write – QF1D512 Passthrough	33
11.7 QF1D512 Configuration Mode	34
12 PACKAGING INFORMATION	35
REGISTERS, TABLES, AND LISTS	36
Control Register Listing.....	36
List of Tables	37
List of Figures.....	37

1 SPECIFICATIONS

1.1 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Min	Max	Units
Storage Temperature	-60	125	°C
Supply Voltage, V_{DD18} to GND	-0.2V	2.2V	V
Supply Voltage, V_{DD33} with respect to GND	-0.2V	4.0V	V
VREG Voltage, V_{VREG33} with respect to GND	-0.2V	4.0V	V
Digital Input Voltage with respect to GND	-0.3	7	V
ESD Immunity (HBM, JESD22-A114-D Class 1C)		7.5	KV
ESD Immunity (HBM, AEC-Q100-002D)		6.75	KV



This integrated circuit can be damaged by ESD. Quickfilter Technologies recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

1.2 Package Assembly

The QF1D512 is offered in a “green” package (RoHS & no Sb/Br), assembled with enhanced environmentally compatible Pb-free and halide-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 260°C during printed circuit board assembly.

1.3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage 1.8	V_{DD18}	1.6	1.8	2.0	V
Supply Voltage 3.3	V_{DD33}	3.0	3.3	3.6	V
VREG Voltage 3.3	V_{VREG33}	3.0	3.3	3.6	V
Digital Input Voltage		0		5	V
Ambient Temperature	T_A	-40	25	85	°C

Note: Quickfilter guarantees the performance of this device over specified ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling.

1.4 Typical Performance Characteristics

Default Conditions: $T_A = 25\text{ C}$, $V_{DD18} = 1.8\text{V}$, $V_{DD33} = 3.3\text{V}$,

1.5 Electrical Characteristics

Symbol	Parameter (Condition)	Min	Typ	Max	Units	Note
Supply Current & Power Dissipation						
I _{DD18}	1.8V Supply Operating Current		- f _S = 50 kHz, 512 taps	1.3		mA
			- f _S = 299 kHz, 512 taps	6.6		mA
			- f _S = 400 KHz, 512 taps	11.6		mA
			- Standby	50		nA
I _{DD33}	3.3V Supply Operating Current		- f _S = 50 kHz	70		uA
			- f _S = 299 kHz	200		uA
			- f _S = 400 KHz	400		uA
			- Standby	20		uA
V _{OVREG}	Voltage Regulator Output Voltage, I _{max} =20mA	1.566	1.8V	2.034	V	
C _{OVREG}	Voltage Regulator External Output Capacitor	0.1	1		uF	
C _{OVREG} ESR	External Capacitor ESR		0.5	1	Ohm	
Digital Inputs (DIN, DSEL, DCLK, SCLK, SDI, CSN, RST_N)						
V _{IH}	High-level Input Voltage, V _{DD33} = 3.6V	2.8		5.5	V	
V _{IL}	Low-level Input Voltage, V _{DD33} = 3.0V	-0.3		0.8	V	
I _{IH} , I _{IL}	Input (leakage) current		+/- 1		uA	
C _{IN}	Input Capacitance		10		pF	
R _{PU}	Pull Up Resistance	40	75	190	KOhm	
R _{PD}	Pull Down Resistance	40	75	190	KOhm	
Digital Output (SDO)						
V _{OH}	High-level Output Voltage, DV _{DD33} = 3.0V, I _{OH} = -100uA	2.4			V	
V _{OL}	Low-level Output Voltage, DV _{DD33} = 3.0V, I _{OL} = 100uA			0.4	V	
C _O	Output Capacitance			10	pF	

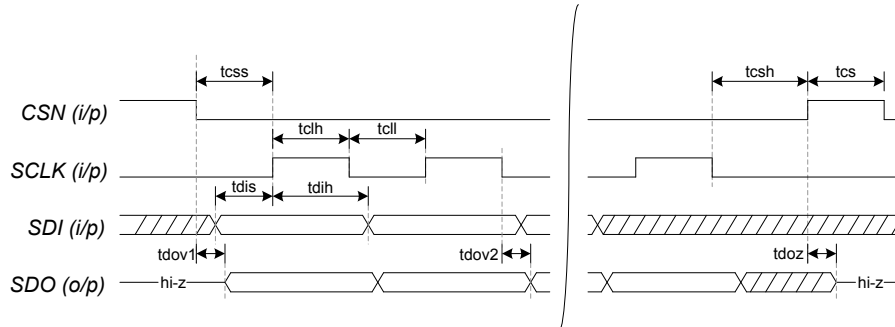
1.6 Timing Requirements

1.6.1 General Timing Requirements

Parameter	Min	Max	Units	Note
Sample Frequency* (f _S)		400	KHz	
Data Input Clock Frequency (DCLK)		20	MHz	
Serial Port Clock Frequency (SCLK) in all modes		20	MHz	
Setup time Chip select (CSN) low to SCLK rising edge	124		nS	
Setup time SDI before SCLK edge	24		nS	
Hold time SDI after SCLK edge	24		nS	
Setup time DSEL active to DCLK rising edge	24		nS	
Setup time DIN before DCLK edge	24		nS	
Hold time DIN after DCLK edge	25		nS	

1.6.2 SPI Configuration Timing Requirements

SPI Configuration Timing

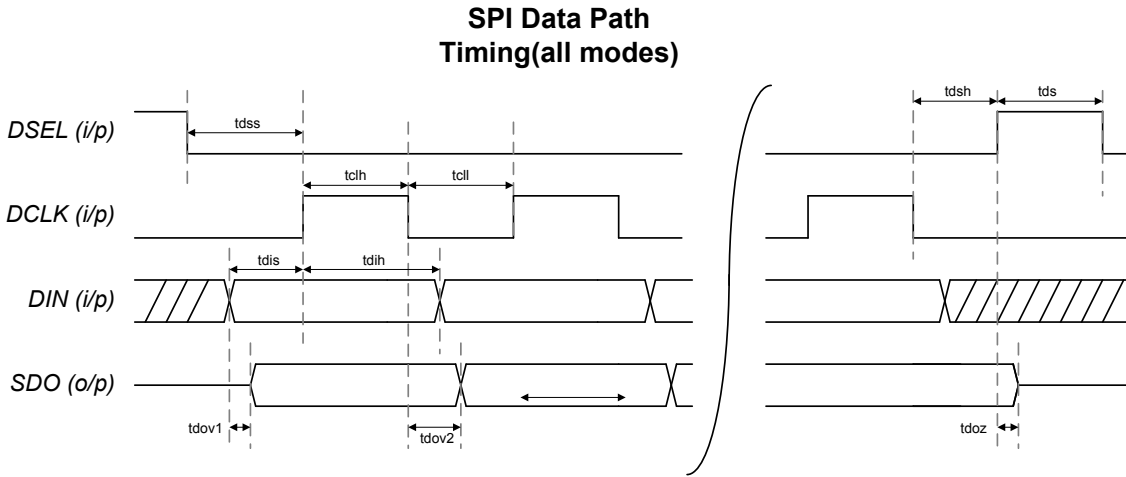


t_{cs} = CSN high time
 t_{css} = CSN falling to SCLK rising time
 t_{csh} = SCLK falling to CSN rising time
 t_{clh} = SCLK high time
 t_{cll} = SCLK low time
 t_{dis} = SDI setup time
 t_{dih} = SDI hold time
 t_{dov1} = CSN falling to SDO valid time
 t_{dov2} = SCLK falling to SDO valid time
 t_{doz} = CSN rising to SDO high-Z time

SPI Configuration Parameters

Parameter (SPI Input)	Min	Max	Units	Note
Sample Frequency* (f_s)		400	KHz	
Serial Port Clock Frequency (SCLK) in all modes		20	MHz	
CSN falling to SCLK rising time(t_{css})	24		nS	
SCLK falling to CSN rising time (t_{csh})	24		nS	
CSN high time (t_{cs})	50		nS	
SDI setup time (t_{dis})	12		nS	
SDI hold time (t_{dih})	24			
CSN falling to SDO valid time (t_{dov1})	12		nS	
SCLK falling to SDO valid time (t_{dov2})	12		nS	
CSN rising to SDO high-Z time (t_{doz})	12		nS	

1.6.3 Data Path Timing Requirements



t_{ds} = DSEL inactive time (Normal Mode)
 t_{dss} = DSEL active to 1st clock edge
 t_{dsh} = Last clock edge to DSEL inactive
 t_{clh} = Clock high time
 t_{ccl} = Clock low time
 t_{dis} = DIN setup time
 t_{dih} = DIN hold time
 t_{dov1} = DIN to SDO valid (pass thru data)
 t_{dov2} = DCLK to SDO valid (filtered data)
 t_{doz} = DSEL inactive to SDO tri-state (Normal Mode)

SPI Output Data Path Timing Parameters

Parameter(SPI Output)	Min	Max	Units	Note
Sample Frequency* (f_s)		400	KHz	
Data Clock (DCLK)		20	MHz	
Setup time DSEL low to DCLK rising edge	24		nS	
Hold time DSEL high	50		nS	
t_{dov1}	8		nS	
t_{dov2}	12		nS	
t_{doz}	12		nS	
Output Current(I_{load})		4	mA	
C_{load}		7	pF	

NOTE: For t_{dov1} and t_{dov2} , the output pin is set with I_{load} at 4mA and C_{load} at 7pf.

2 PINOUT and PIN DESCRIPTIONS

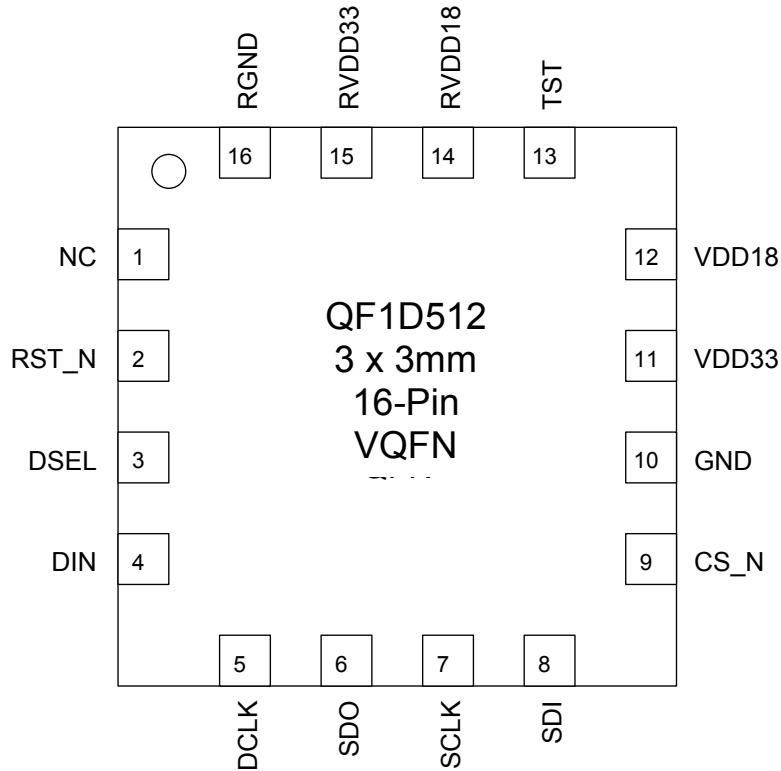
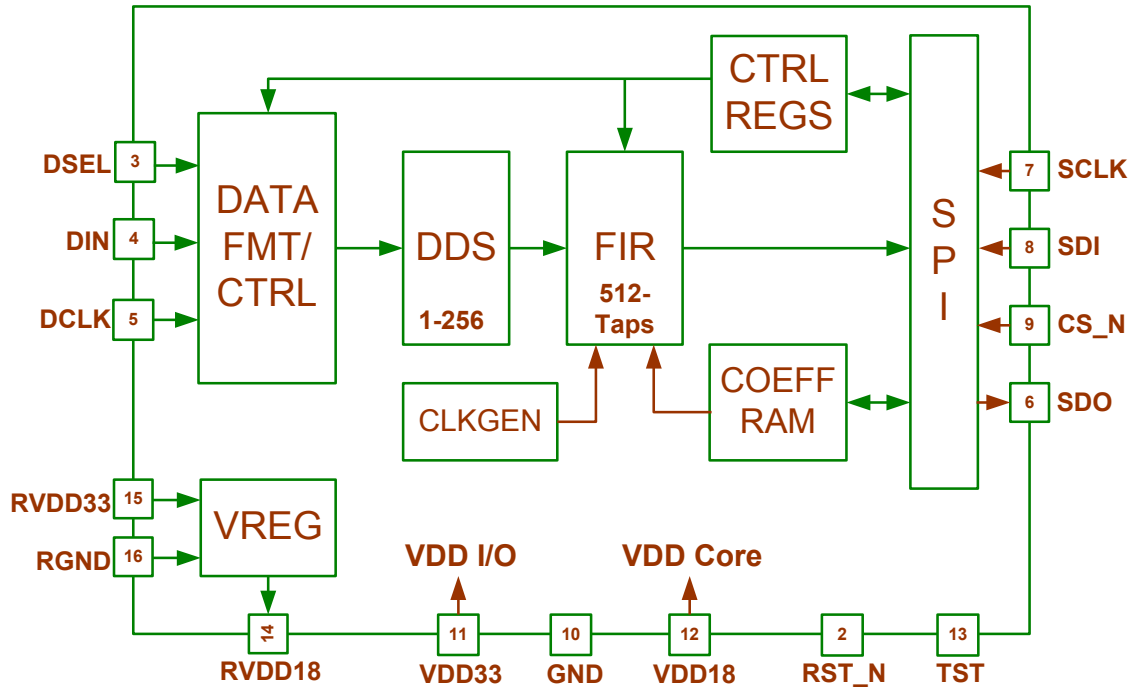


Figure 1: 16 Pin QFN Package Pin out

Table 1 Pin Descriptions

Pin	Signal Name	I/O	Type	Description
1	NC			No Connection
2	RST_N	I	Digital	Chip reset; active low; default internal pull-up
3	DSEL	I	Digital	SPI Mode: frames the data as a chip select; Synchronous Serial Mode: a frame pulse whose rising or falling edge identifies the 1 st bit of data; active high or low
4	DIN	I	Digital	Serial data input
5	DCLK	I	Digital	Data input clock used to capture DIN; active capture edge either high or low
6	SDO	O	Digital	Serial data output. Can be either config data or ADC/filter data depending on mode
7	SCLK	I	Digital	Serial input clock used for config data transfers; active capture edge either high or low
8	SDI	I	Digital	Serial data input used for config data
9	CS_N	I	Digital	Config interface chip select; active low; default internal pull-up
10	GND	N/A	Return	Digital power supply return pin
11	VDD33	N/A	Power	Digital I/O voltage; 3.3 +/- 10%
12	VDD18	N/A	Power	Digital Core voltage; 1.8 +/- 10%
13	TST	I	Digital	Production scan test mode enable; active high; default internal pull-down
14	RVDD18	N/A	Power	Internal voltage regulator 1.8v output; tie to VDD18 when in use; tie to GND to disable
15	RVDD33	N/A	Power	Internal voltage regulator 3.3v input; tie to GND to disable
16	RGND	N/A	Return	Internal voltage regulator return pin

3 GENERAL DESCRIPTION



2

Figure 3: Functional Block Diagram

3.1 Data Format and Control

The Data Format and Control block accepts the ADC serial data. It separates any header information and checks for data valid and then separates the data bits for processing. It also converts the data into the required format for the FIR filter.

3.2 Averaging and Down-sampler

The Averaging / Down-sampler block down-samples the incoming data by a factor of 1 to 256. It also can be configured to average the down sampled data.

3.3 Finite Impulse Response filter (FIR)

The FIR filter consists of up to 512 taps for a symmetric filter or 256 taps for an asymmetric filter.

3.4 Serial Interface - Serial Peripheral Interface (SPI)

The configuration and data serial interfaces are fully compatible with a standard SPI bus. Both the DCLK and SCLK are capable of running at up to 20 MHz, although they may be run at much lower speeds. The QF1D512 operates in a SLAVE mode.

The configuration interface consists of the SCLK, CS_N, SDI and SDO pins and is used to configure the control registers and program the coefficient memory space.

The data interface consists of the DCLK, DSEL, DIN, and SDO pins and allows for ADC data received on DIN to be filtered or passed through to SDO and on to the controlling device (uP, DSP, FPGA). DIN may also come from the controlling device (FIR coprocessor mode). If a header is used, it is passed unaltered along with the filtered data.

3.5 Voltage Regulator

The QF1D512 provides an internal voltage regulator to allow for operation from a single 3.3 V supply. The regulator is stand-alone and its use is optional.

4 SOFTWARE

4.1 Device Configuration

Before useful data can be output from the QF1D512 it must first be correctly configured. Configuration parameters include the following:

1. Data interface configuration: includes header use and size, and data size
2. Data mode of operation: SPI Normal, Continuous, or Synchronous Serial mode
3. Decimation and averaging configuration (if utilized)
4. FIR filter coefficients.

4.2 Quickfilter Development Kit (QF1D512-DK)

The Development Kit is a complete hardware and software combination which allows for rapid development of the QF1D512 configuration parameters for a specific application.

The Quickfilter Design Software tool allows all the necessary parameters to be generated in a quick and user-friendly manner. The user enters the desired characteristics (e.g. sampling rates, type of filter, cut-off frequencies etc.) for each channel and the software generates a configuration file for the device. The configuration file can be immediately downloaded into the QF1D512 on the development board, and the *actual hardware device performance* can be monitored - either in response to a PC-generated noise source or to a user-applied signal. Device configuration parameters can be further adjusted, if necessary, until the optimum system performance is reached.

Once satisfied with the performance the configuration file can be saved for future use, for example to program devices in bulk prior to volume board manufacturing.

5 CONFIGURATION INTERFACE

5.1 Native SPI Mode of Operation

The QF1D512 is designed to interface directly with the serial peripheral interface (SPI) of microcontrollers and Digital Signal Processors. The QF1D512 always operates in SPI slave mode using the **SDI**, **SDO**, **SCLK** and **CS_N** pins. **SDI** is the input serial data, and **SDO** is the output serial data (if **FILT_EN** = **DIN_PT** = 0*). **SCLK** is the input serial clock. Default is to capture on rising edge, but this can be changed to capture on falling edge by writing the **SCLK_POL** bit in the **DCONFIG** register (04h).

* There are two modes of bus operation for the QF1D512, "configure" mode, and "data" mode. The required mode is selected by writing the **FILT_EN** bit in the **CONTROL** register (03h). When *configuring* the device both **FILT_EN** and **DIN_PT** should be set to 0 (see Section 6.3).

"Configure" mode is used to set up or change options in the QF1D512. In this mode it is possible to read/write the control registers and the coefficient RAM.

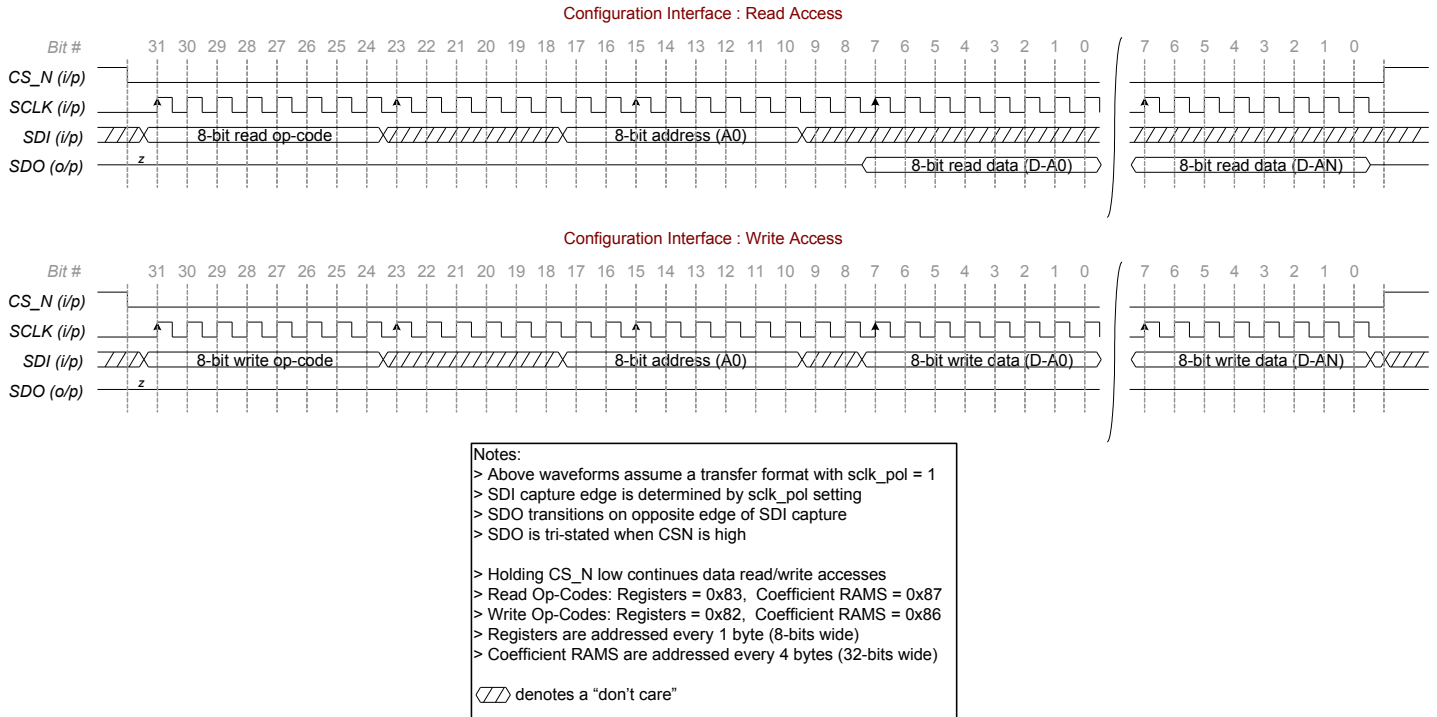
"Data" Mode is used to interface with an ADC or uP and run the FIR filter. When **FILT_EN** is set high, the function of the **SDO** pin changes from configuration data to filter data. (see DATA INTERFACE). The format of the **SDO** will match the format of the data coming into the **DIN** pin.

Note: The Control registers can be written to in either mode. However to write the coefficients or read the control registers the QF1D512 must be in "configure" mode.

5.2 Native SPI Configuration Mode Data Format

In order to address and read / write to the QF1D512, **CS_N** is asserted low to select the device. When the device is in “configure” mode but is not selected, data will not be accepted via the serial input pin (**SDI**) and the serial output pin (**SDO**) will remain in a high impedance state.

Figure 4: Configuration Data Timing



Note: There are 6 “don’t care” clock cycles between the end of the op code and the 8-bit address. The value of SDI during these clocks has no effect on the chip. There are also two “dead” clock cycles between the end of the address input and data output on the SDO pin.

The active edge of SCLK is programmable (**SCLK_POL** bit in the **DCONFIG** register) to suit the application system timing:

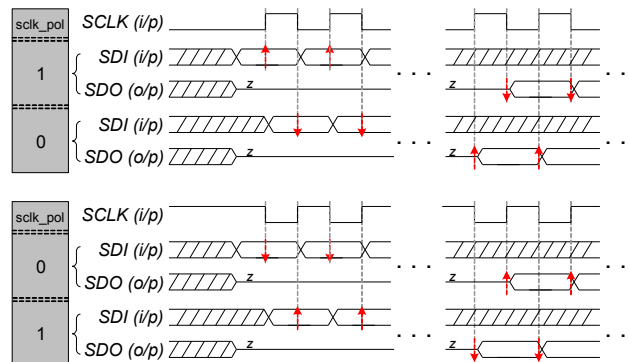


Figure 5: Configuration Interface Transfer Format

5.3 I2C Mode of Operation

While the QF1D512 is designed to interface directly with the serial peripheral interface (SPI) bus of microcontrollers and Digital Signal Processors, it is relatively straightforward to interface to and be controlled by an Inter-IC (I2C) master. Both interface protocols use a Master/Slave hierarchy and synchronous data transmission, with the SPI interface using two separate data lines (one input and one output) and the I2C interface using a single bi-directional data line.

The most significant difference in these two interface mechanisms lies in their addressing schemes. Each SPI device has its own chip select (CS) input. The SPI master selects any given SPI slave device by activating its chip select (for the QF1D512, pulling it low). At any given time, only one SPI slave will be selected, so any commands sent are responded to by that device. The I2C interface does not use chip selects. All I2C slave devices receive every command and the addressing scheme, imbedded in the software protocol, determines which slave is to respond to the command (see figure 5).

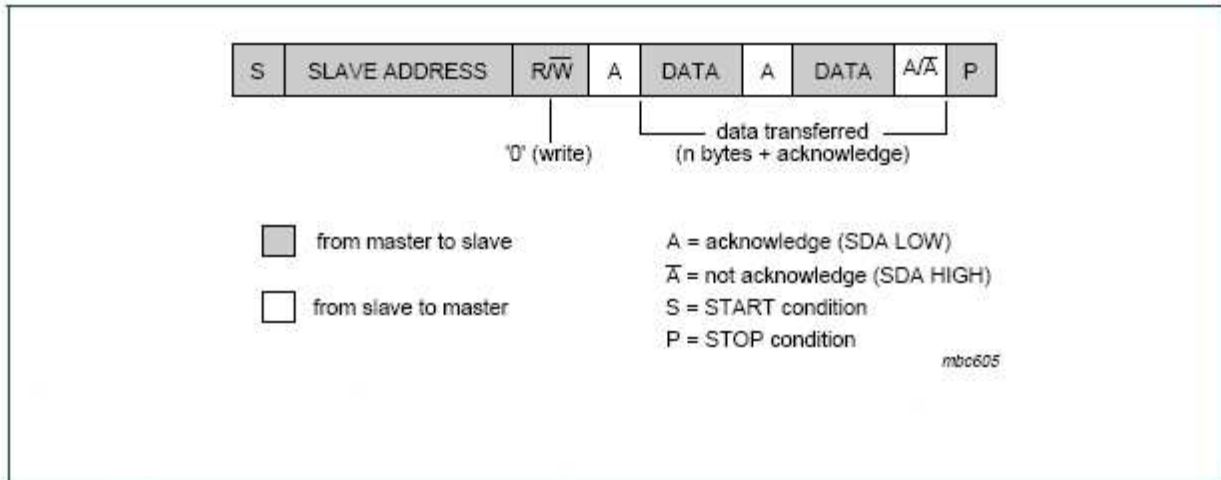


Figure 6: I2C Master/Slave Interaction

Each slave must detect its own address and respond only to those commands intended for it. For this reason, the I2C protocol includes arbitration and collision detection. While an SPI command is a single stream of bits from the master to the slave (and, for a READ command, a stream of bits back to the master), an I2C command is a succession of bit-string transfers and Acknowledge/Not-Acknowledge signals, interspersed throughout the command (see figure 6).

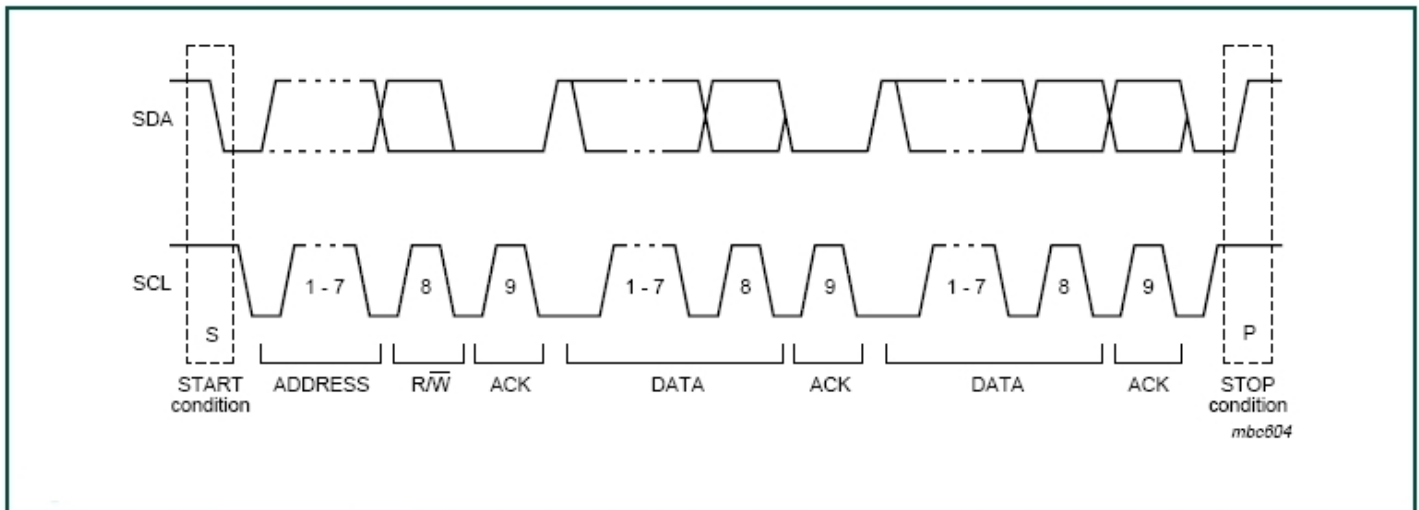


Figure 7: I2C Master/Slave Command/Response Timing

In interfacing the QF1D512 to an I2C bus, the presence of an ACK/NAK bit approximately every 8th location in the I2C data stream, must be properly handled with respect to both the I2C master and the QF1D512. This requires a response from the QF1D512 (or at least, a simulated response from the interface to the QF1D512). From the perspective of the QF1D512, the presence of the ACK/NAK bits interferes with the QF1D512's recognition of the address and data fields within the command and must be removed from the command stream.

Successfully interfacing the QF1D512 to an I2C bus requires the use of a bridge circuit (see figure 7). The bridge can be implemented entirely in hardware (e.g., logic gates in a PLD or PAL) or through a combination of hardware and software (e.g., a low-cost microcontroller with embedded code). In either case, this circuit must recognize and respond to both the start and stop conditions; reply automatically back to the I2C master with ACK's (signifying that all is well and ensuring that the master continues with the transmission); and, strip the ACK's from the stream of data sent on to the 1D (the data received by the 1D will look like a normal SPI command).

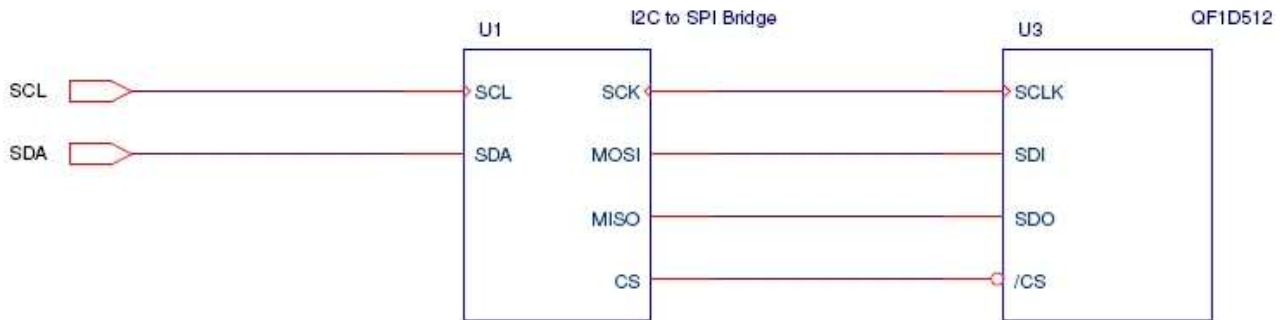


Figure 8: I2C to SPI Bridge Circuit

The I2C-to-SPI bridge will look to the I2C master like an I2C slave and to the QF1D512 like an SPI master. It will intercept the I2C commands, responding appropriately as applicable, and send on the equivalent SPI command to the 1D.

5.4 I2C Configuration Mode Data Format

The I2C bridge circuit must read and acknowledge the QF1D512's I2C address and strip this address from the SPI command sequence sent on to the QF1D512 (see figure 8). The first data byte must contain the command opcode (82h for Configuration WRITE, 83h for Configuration READ, 86h for Coefficient WRITE, or 87h for Coefficient READ) as it will be the first byte received by the QF1D512. The subsequent data byte(s) will contain the actual data to be written or the data being read.

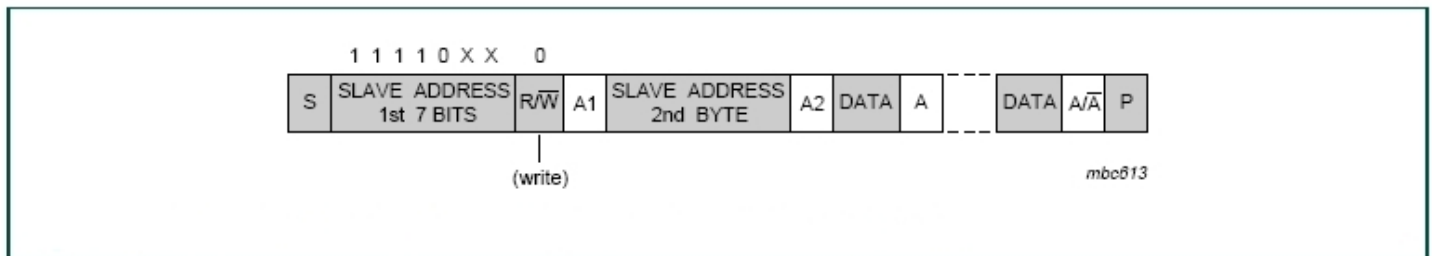


Figure 9: I2C Addressing Protocol

5.5 Sending Commands in Filter Mode

If the QF1D512 is in Data mode and it is required to reconfigure the device, it is first necessary to switch to Configure mode. This is done by writing to the FILT_EN bit using the configuration interface.

Note: While all of the configuration registers are accessible while the QF1D512 is in Data mode, the only register that should be accessed is the CONFIG register (address 0003h) and only the FILT_EN bit (bit 0) should be modified. Accesses to other registers might result in corrupted filter data or other unpredictable behavior.

In configurations in which the SDI and the DIN pins have been tied together, allowing for single SPI port data filtering, it is necessary to ensure that the incoming data format does not match either the configuration register access format (see Table 4 Configuration Register Access Format) or the FIR coefficient memory access format (see **Error! Reference source not found.**) as this may cause unintentional writes to configuration or coefficient memory. In other words, take care to ensure that the most significant byte of the data input does not match either of the WRITE opcodes.

6 DATA INTERFACE

6.1 Modes of Operation

The QF1D512 is designed to interface directly with a variety of ADC converters. The QF1D512 has four data interface modes:

1. SPI Normal Mode
The data is framed by the DSEL input signal
2. SPI Continuous Mode
Once DSEL is active data is output corresponding to clock bursts on the DCLK input
3. Synchronous Serial Mode
DSEL is used as a trigger to indicate the start of each new sample period. DCLK runs continuously, filtered data is output on the next n cycles of DCLK according to the programmed word length.
4. I2S Mode
A word select line (**WS** on the DSEL input) indicates which of two time-division multiplexed data channels is being transmitted. The channels are transmitted alternately on the data line (**SD** on the SDI input) and are synchronized by a clock line (**SCK** on the DCLK input).

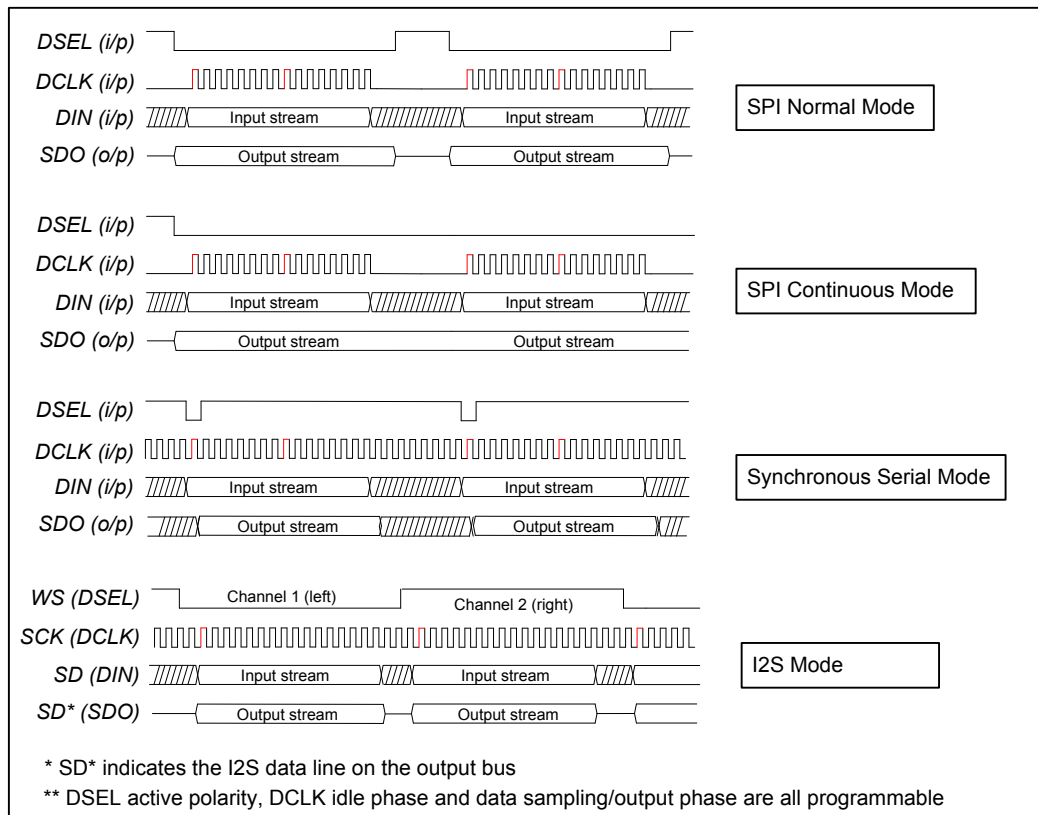


Figure 10: Interface Modes

Note: In both SPI Continuous Mode and SPI Normal Mode data should be presented to the part only when DSEL is active. In other words, the data clock, DCLK, should not clock unless DSEL is active. For more information on this requirement, see Quickfilter Application Note QFAN024 – Quickfilter in Multi-SPI Environment App Note.

MODE1	MODE0	Bus Mode
0	0	(Default) SPI Normal Mode
0	1	SPI Continuous Mode
1	X	Synchronous Serial Mode
1	X	I2S Mode

Figure 11: Data Format Selection

The data interface utilizes the **DIN** (**SD** for I2S), **SDO** (**SD*** for I2S), **DSEL** (**WS** for I2S) and **DCLK** (**SCK** for I2S) pins. **DIN** is the input serial data, and **SDO** is the output serial data (if **FILT_EN** = 1). **DCLK** is the input data clock and **DSEL** is the framing signal for the input data:

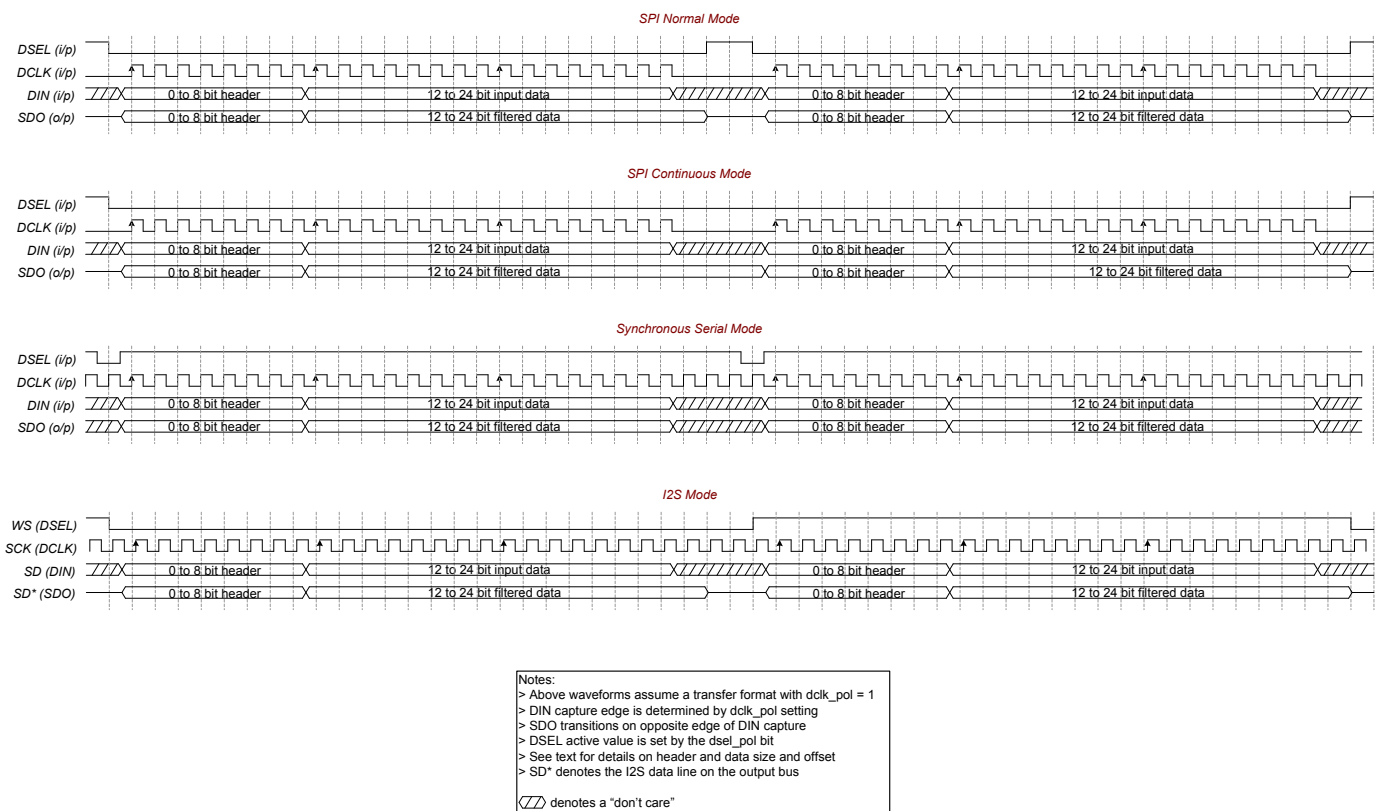


Figure 11: Data Interface Timing Diagram

Note: In SPI Continuous Mode the value of the SDO output (lsb) at the end of the data sample will be held constant until the header is output for the next data sample.

The QF1D512 supports both 2's complement and offset binary data formats. The data format is set by the **FORMAT** bit and the data mode is selected the **MODE0** and **MODE1** bits in the **DCONFIG** register (04h).

Default operation is to capture on the rising edge of **DCLK** (**SCK** for I2S), but this can be changed to capture on falling edge by writing the **DCLK_POL** bit in the **DCONFIG** register (04h). The active polarity of **DSEL** (**WS** for I2S) is also programmable via the **DCONFIG** register (**DSEL_POL** bit), which is especially useful for applications where the input pins are paired; e.g., **DIN** (**SD** for I2S) and **SDI**, **DCLK** (**SCK** for I2S) and **SCLK**, **CS_N** and **DSEL** (**WS** for I2S).

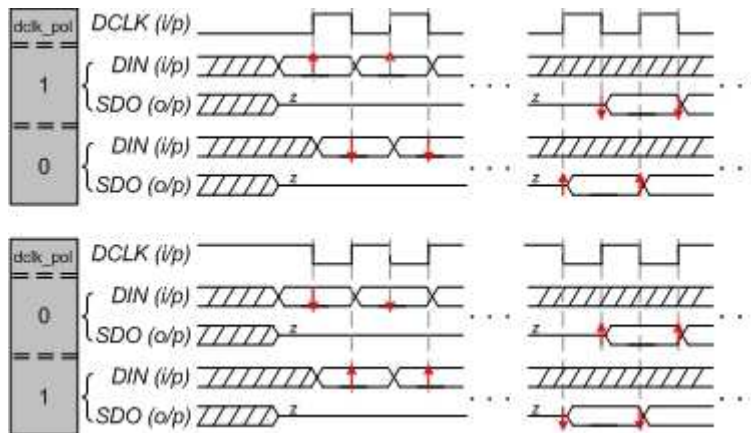


Figure 12: Data Interface Transfer Format

The QF1D512 supports data widths in the range of 12 and 24 bits, and headers of up to 8 bits.

The format of the input data stream is specified in the **HD_OFFSET** (address 09h), **HD_SIZE** (address 0Ah), **DATA_OFFSET** (address 000Dh), and the **DATA_SIZE** (address 000Eh) registers. These registers set the header offset, header size, data offset, and data size respectively of the individual data sample. This allows for a large number of different data formats. Additionally, if the sample data contains a data valid qualifier, this field can be masked by configuring the **HD_MASK**, address 0Bh and **HD_VALUE**, address 0Ch registers. The filtering of the sample will occur only if this value matches **HD_VALUE**, address 0Ch, otherwise the raw sample data is passed directly through to the **SDO** pin unfiltered.

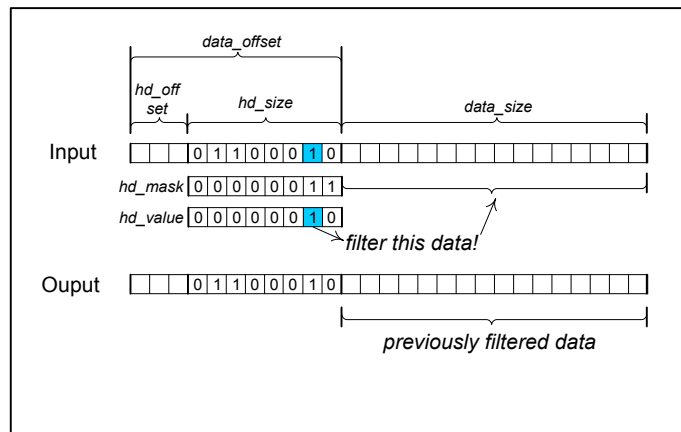


Figure 13: Data Header Masking Example

When configured for **FILTER** mode, **FILT_EN** bit set to '1' in the **CONTROL** register (03h), the output stream on the **SDO** pin will have the same format as the input stream coming in on the **DIN** pin. The header data is passed directly through to the **SDO** pin while the filtered data has a latency associated with it due to the properties of the FIR filter. If no filtering is being done (data valid qualifier in header does not match **HD_VALUE**) coincident header and data will be passed through for possible use down-stream of the QF1D512 device.

When averaging and / or down sampling is active, the data rate will be the same as the incoming data rate, but the number of valid samples will be reduced by the averaging / down sampling rate.

6.2 Data Passthrough

Sometimes it is required to pass-through the data present at **DIN** directly to the **SDO** output, for example when passing configuration data back from an ADC to the host controller. The data pass-through bit, **DIN_PT**, in the **CONTROL** register (03h), will force this to occur when it is set to 1. In this mode **SDO** follows **DIN** immediately, there is no clocking required. This control bit overrides all other settings for **SDO** functionality (see next section) and should be set to 0 for either configuration mode or data filtering.

6.3 SDO Functionality

The functionality of the **SDO** output pin, depending on the serial port mode selected, can be altered depending on the values of the control bits **DIN_PT** and **FILT_EN**, whether valid data to be filtered is present, and the levels on **CS_N** or **DSEL**. This functionality is illustrated in the following figures:

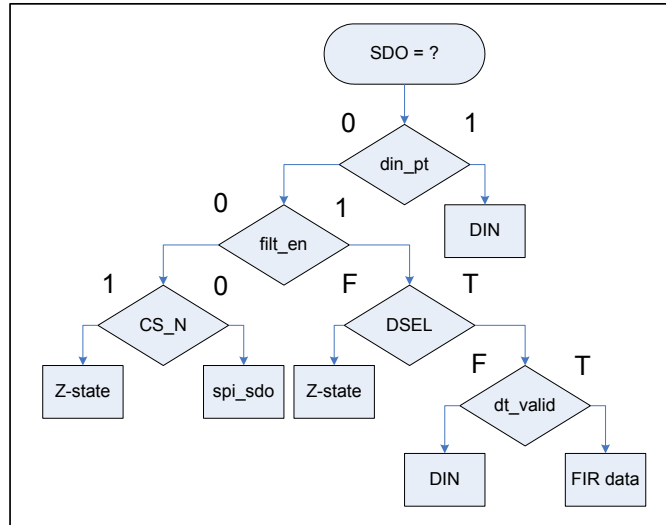


Figure 14: SDO Functionality – FIR Coprocessor and SPI Modes

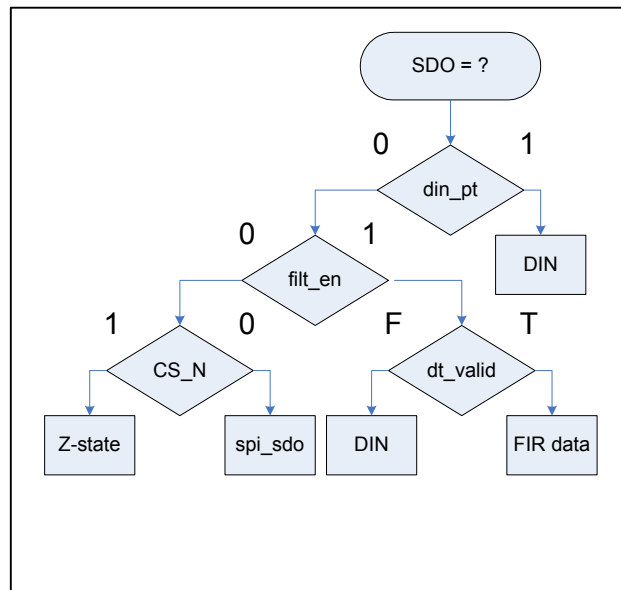


Figure 15: SDO Functionality – Sync Serial Mode

- Notes:
1. The value of **DSEL** is shown as either True or False, as the active level is user programmable.
 2. **dt_valid** is an internal control bit which is set true when the input data matches the programmed mask values for valid data.

7 AVERAGING and DOWNCONVERTER

7.1 Modes of Operation

The QF1D512 provides the capability to down-sample the incoming data samples. The divider ratio is any integer value and ranges from 1 (no down-sampling) to 256. The value is selected in the **DECIMATE** register (address 08h). In addition to down-sampling and “throwing away” the intermediate samples, an option is provided to average the samples and forward the averaged value to the downstream FIR filter. The averaging block effectively adds up N samples, where N is the down-sampling rate, then divides by a power of 2 by right shifting the result. Note that if averaging is enabled with a down-sampling rate that is not a power of 2, system gain will be affected. The averaging block always divides by the next highest power of 2 when a *non* power of 2 down-sampling rate is detected. Refer to the diagram below. This feature can be useful for noise reduction and possibly increasing bit resolution of the input data stream. To select filtering of the down sampled data, **DEC_AVG_EN**, bit 0 of the **FCONFIG** register (address 05h) is enabled.

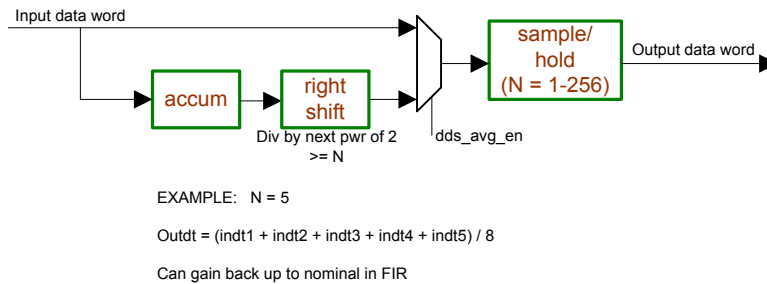


Figure 16: Averaging /Down-sampler Block Diagram

8 FIR FILTER

8.1 Modes of Operation

The QF1D512 filter can implement a symmetric 512-tap FIR filter or a 256-tap asymmetric FIR filter, which is used to define the precise filtering characteristics desired. The filter coefficients are 32 bits wide. The filtering provided by the software may be following types: low-pass, notched low-pass, high-pass, band-pass, dual band-pass, band-stop, and dual band-stop. Currently available filter algorithms include Parks-McClellan and Windowed Sync. User defined filters can also be implemented.

The QF1D512 can be loaded with up to 256 filter coefficients. To implement a non-folded (asymmetric) filter the **FIR_FOLD** bit in the **FCONFIG** register (05h) should be set to 0, allowing a filter of up to 256 taps. A folded (symmetric) filter of up to 512 taps can be implemented if **FIR_FOLD** is set to 1.

Note: For a folded filter, if the number of coefficients (N) is even, a filter of 2N taps will be realized. If N is odd, a filter of 2N-1 taps will result.

The Quickfilter software allows the user to enter the filter characteristics required and see the predicted performance in terms of frequency and impulse response. Once the desired performance has been attained, the configuration can be downloaded to the QF1D512, and the actual filter performance verified, by using the development kit. The development board can be fed with a white noise source (or other source as desired by the user) and the software can display an FFT of the QF1D512’s filter response.

8.2 FIR Latency

The delay introduced by the FIR filter is dependent on the number of taps of the filter and the data rate of the samples coming into the FIR filter. The delay is calculated by the following equation:

$$\text{FIR Delay} = (\# \text{ taps} - 1) / 2 * 1/f_s + 6/f_s$$

For data sampling at a 10 kHz rate, the latency will result in:

512 tap (maximum) filter:	Latency = 25.5ms
100 tap filter:	Latency = 4.95ms

Note: If using the Quickfilter Pro development software the latency of a particular filter is calculated and displayed in the Information bar on the "Filter" tab.

9 Voltage Regulator

9.1 Mode of Operation

The QF1D512 provides an internal linear voltage regulator to allow for operation from a single 3.3V supply. To use this feature, the input to the voltage regulator (pin **RVDD33**) is connected to the 3.3V supply. The output (pin **RVDD18**) is connected to the **VDD18** pin.

To disable this feature, tie **RVDD33** to Ground and leave the **RVDD18** pin unconnected (or connected to GND). When disabled the regulator consumes no power.

The regulator may be used to power additional 1.8V devices in the system. The output current drawn by the 1.8V circuitry of the QF1D512 plus the current drawn by any external devices must not exceed the maximum rating in Electrical Characteristics. It is important to provide adequate decoupling on the regulator output to eliminate droop due to switching of any connected loads.

10 CONTROL REGISTERS

10.1 Overview

The QF1D512 internal data is separated into configuration registers and coefficient memory.

Table 2 Register and Memory Format

Registers	Address Range	Data Size	Write OpCode	Read OpCode
Device Configuration	0x0000 – 0x0018	8 bit	0x82	0x83
FIR Coefficients	0x0000 – 0x00FF	32 bit	0x86	0x87

Table 3 Control Registers

Hex*	Register Name	Description
0000h	TEST_RW	Software Register, Test Reads and Writes
0001h	CHIP_ID	Chip ID Number
0002h	VERSION	Chip Version Number
0003h	CONTROL	Mode Control Register
0004h	DCONFIG	Data Format Control
0005h	FCONFIG	Filter Control and Status
0006h	NUM_TAPS	Number of Taps, lower bits
0007h	NUM_TAPS	Number of Taps, upper bits
0008h	DECIMATE	Down-sampling Rate
0009h	HD_OFFSET	Header Offset
000Ah	HD_SIZE	Header Length
000Bh	HD_MASK	Header Valid Mask
000Ch	HD_VALUE	Header Valid Value
000Dh	DATA_OFFSET	Data Offset
000Eh	DATA_SIZE	Data length
000Fh	TEST	Chip Test Register
0010h	IO_TST	TST Pin Configuration
0011h	IO_RST_N	RST_N Pin Configuration
0012h	IO_DCLK	DCLK Pin Configuration
0013h	IO_DSEL	DSEL Pin Configuration
0014h	IO_DIN	DIN Pin Configuration
0015h	IO_CS_N	CS_N Pin Configuration
0016h	IO_SCLK	SCLK Pin Configuration
0017h	IO_SDI	SDI Pin Configuration
0018h	IO_SDO	SDO Pin Configuration

10.2 Configuration Registers

Accessing the configuration registers uses an SPI access as shown below.

Table 4 Configuration Register Access Format

	OPCODE	ADDRESS	UNUSED	DATA
Number of bits	8 bits	14 bits	2 bits	8 bits per register [†]
Write Access	82h	0000h – 0018h	Don't care	00h – FFh
Read Access	83h	0000h – 0018h	Don't care	00h – FFh

Note: * Multiple registers can be written/read by extending the SPI access cycle.

Listed below are the detailed configuration register definitions.

Note: * denotes default values

→ 1 00h TEST_RW (User Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 00h	D7	D6	D5	D4	D3	D2	D1	D0

Description: Provided as a blank user byte for the programmer to read and write to as a test. This byte defaults to 0 at power up.

→ 2 01h CHIP_ID (Chip ID) - READ ONLY

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 01h	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

[ID7:ID0] = Identification number of the QF1D512, default = B0h.

Description: This read-only byte contains a number describing the identification of the QF1D512 device.

→ 3 02h VERSION (Version) - READ ONLY

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 02h	VER7	VER6	VER5	VER4	VER3	VER2	VER1	VER0

[VER7:VER0] = Version number of the QF1D512, default = 01h.

Description: This read-only byte contains a number describing the version of the QF1D512 device.

→ 4 03h CONTROL (Filter/Pass Through Control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 03h	X	X	X	X	X	X	DIN_PT	FILT_EN

[FILT_EN]

*0 = Configuration mode, SDO pin outputs the configuration register.

1 = Filter mode, SDO pin outputs the signal path data.

Description: Selects the data source of the SDO pin and enable the Signal processing blocks and data path.

[DIN_PT]

* 0 = Normal operation, SDO pin outputs the Configuration register or signal path data.
 1 = Data pass through, SDO pin outputs the data on the DIN pin
 Description: Puts the QF1D512 in Bypass mode.

→ **5 04h DCONFIG (Data Format Control)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 04h	X	X	MODE1	MODE0	FORMAT	DSEL_POL	DCLK_POL	SCLK_POL

[SCLK_POL]

0 = Input (SDI) Data is captured on the falling edge of SCLK.
 *1 = Input (SDI) Data is captured on the rising edge of SCLK.
 Description: Selects the clock edge of SCLK on which the data on the SDI is captured. SDO is output on the opposite edge.

[DCLK_POL]

0 = DIN is captured on the falling edge of DCLK.
 *1 = DIN is captured on the rising edge of DCLK.
 Description: Selects the clock edge of DCLK on which the data on the DIN pin is captured. SDO is output on the opposite edge (Filter mode).

[DSEL_POL]

*0 = DSEL is active low.
 1 = DSEL is active high.
 Description: Selects polarity of the DSEL pin.

[FORMAT]

*0 = Incoming data format is 2's complement.
 1 = Incoming data format is offset binary.
 Description: Selects the data format of the incoming data.

[MODE1:MODE0]

*00 = Input data mode is SPI Normal Mode.
 01 = Input data mode is SPI Continuous Mode.
 1X = Input data mode is Synchronous serial mode
 Description: Selects the data input mode.

→ **6 05h FCONFIG (Filter Control)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 05h	X	X	X	X	X	OVF_FLAG	FIR_FOLD	DEC_EN

[DEC_EN]

*0 = Averaging of down-sampled data is disabled.
 1 = Averaging of down-sampled data is enabled.
 Description: Selects the averaging of down-sampled data.

[FIR_FOLD]

0 = FIR Filter is not folded (asymmetric, 256 taps maximum).
 *1 = FIR Filter is folded (symmetric, 512 taps maximum).
 Description: Selects whether the FIR filter is symmetric (folded) or asymmetric.

[OVF_FLAG]

*0 = FIR filter has not overflowed.

1 = FIR filter has overflowed.

Description: Indicates that the FIR filter has overflowed. To clear, write a '0' to this bit.

→ **7** 06h NUM_TAPS (Number of FIR Filter Taps, Lower Bits)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 06h	NTAP7	NTAP6	NTAP5	NTAP4	NTAP3	NTAP2	NTAP1	NTAP0

→ **8** 07h NUM_TAPS (Number of FIR Filter Taps, Upper Bit)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 07h	X	X	X	X	X	X	X	NTAP8

[NTAP8: NTAP0] = Number of taps in the FIR filter, range from 0 to 511 (= 1 – 512 taps), default = 1FFh (512 Taps).

Description: Sets the number of taps in the FIR filter.

→ **9** 08h DECIMATE (Down-sampling Rate)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 08h	DEC7	DEC6	DEC5	DEC4	DEC3	DEC2	DEC1	DEC0

[DEC7: DEC0] = Down-sampling rate, range from 0 (no down-sampling) to 255 (= 256 down-sampling rate), default = 0h (no down sampling).

Description: Sets the down-sampling rate from 1 (no down-sampling) to 256.

→ **10** 09h HD_OFFSET (Offset of Header Field)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 09h	HDOFF7	HDOFF6	HDOFF5	HDOFF4	HDOFF3	HDOFF2	HDOFF1	HDOFF0

[HDOFF 7: HDOFF 0] = Header field offset in bits, range 0 to 255, default = 0h.

Description: Sets the offset in bits in the data word of the header.

→ **11** 0Ah HD_SIZE (Size of Header Field)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Ah	X	X	X	X	HDSIZ3	HDSIZ2	HDSIZ1	HDSIZ0

[HDSIZ3: HDSIZ0] = Header field size in bits, range 0 to 8, default = 0h.

Description: Sets the size of the header field.

→ **12 0Bh HD_MASK (Header Data Valid Mask)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Bh	HDMSK7	HDMSK6	HDMSK5	HDMSK4	HDMSK3	HDMSK2	HDMSK1	HDMSK0

[HDMSK 7: HDMSK 0] = Header data valid bits, default = 0h.

Description: Sets the bits of the header which are used to indicate the data valid condition of the sample.

→ **13 0Ch HD_VALUE (Header Data Valid Value)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Ch	HDDV7	HDDV6	HDDV5	HDDV4	HDDV3	HDDV2	HDDV1	HDDV0

[HDDV 7: HDDV 0] = Header data valid bit pattern, default = 0h.

Description: Sets the pattern in the header which indicates that the data is valid. This value has the mask defined in the **HD_MASK** register (0Bh) applied to it.

→ **14 0Dh DATA_OFFSET (Offset of Data Field)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Dh	DAOFF7	DAOFF6	DAOFF5	DAOFF4	DAOFF3	DAOFF2	DAOFF1	DAOFF0

[DAOFF 7: D DAOFF 0] = Data field offset in bits, range 0 to 255, default = 0h.

Description: Sets the offset to the data field in the incoming data.

→ **15 0Eh DATA_SIZE (Number of Bits in the Data Field)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Eh	X	X	X	DASIZ4	DASIZ3	DASIZ2	DASIZ1	DASIZ0

[DASIZ4: DASIZ0] = Data field size in bits, range 12 to 24 bits, default 10h (16 bits).

Description: Sets the number of bits in the data field. Only values 12 through 24 are valid. Unpredictable results may occur for values outside this range.

→ **16 0Fh TEST (Chip Test Register) – RESERVED Y**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Fh	X	X	X	X	X	X	X	X

Description: The register is reserved and should not be accessed. Unpredictable results may occur if accessed.

→ **17** 10h IO_TDT (**TST Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 10h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the TST pin.

[PD_EN]

0 = No pull down resistor on input.

*1 = 75K Ohm pull down resistor on input.

Description: Enables the pull down resistor on the TST pin.

[PU_EN]

*0 = No pull up resistor on input.

1 = 75K Ohm pull up resistor on input.

Description: Enables the pull down resistor on the TST pin.

→ **18** 11h IO_RST_N (**RST_N Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 11h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on RST_N pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull down resistor on input.

Description: Enables the pull down resistor on the RST_N pin.

[PU_EN]

0 = No pull up resistor on input.

*1 = 75K Ohm pull up resistor on input.

Description: Enables the pull down resistor on the RST_N pin.

→ **19** 12h IO_DCLK (**DCLK Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 12h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the DCLK pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull-down resistor on input.

Description: Enables the pull down resistor on the DCLK pin.

[PU_EN]

*0 = No pull up resistor on input.

1 = 75K Ohm pull-up resistor on input.

Description: Enables the pull down resistor on the DCLK pin.

→ **20** 13h IO_DSEL (**DSEL Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 13h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the DSEL pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull-down resistor on input.

Description: Enables the pull down resistor on the DSEL pin.

[PU_EN]

*0 = No pull up resistor on input.

1 = 75K Ohm pull-up resistor on input.

Description: Enables the pull down resistor on the DSEL pin.

→ **21** 14h IO_DIN (**DIN Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 14h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the DIN pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull-down resistor on input.

Description: Enables the pull down resistor on the DIN pin.

[PU_EN]

*0 = No pull up resistor on input.

1 = 75K Ohm pull-up resistor on input.

Description: Enables the pull down resistor on the DIN pin.

→ **22** 15h IO_CS_N (**CS_N Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 15h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the CS_N pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull-down resistor on input.

Description: Enables the pull down resistor on the CS_N pin.

[PU_EN]

0 = No pull up resistor on input.

*1 = 75K Ohm pull-up resistor on input.

Description: Enables the pull down resistor on the CS_N pin.

→ **23** 16h IO_SCLK (**SCLK Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 16h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the SCLK pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull-down resistor on input.

Description: Enables the pull down resistor on the SCLK pin.

[PU_EN]

*0 = No pull up resistor on input.

1 = 75K Ohm pull-up resistor on input.

Description: Enables the pull down resistor on the SCLK pin.

→ **24** 17h IO_SDI (**SDI Pin Configuration**)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 17h	X	X	X	X	X	PU_EN	PD_EN	SMT_EN

[SMT_EN]

0 = Normal input.

*1 = Schmitt trigger input.

Description: Enables the Schmitt trigger input on the SDI pin.

[PD_EN]

*0 = No pull down resistor on input.

1 = 75K Ohm pull-down resistor on input.

Description: Enables the pull down resistor on the SDI pin.

[PU_EN]

*0 = No pull up resistor on input.

1 = 75K Ohm pull-up resistor on input.

Description: Enables the pull down resistor on the SDI pin.

→ **25 18h IO_SDO (SDO Pin Configuration)**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	X	X	X	X	X	DR2MA	DR4MA	SLEW

[SLEW]

*0 = Slow slew rate.

1 = Fast slew rate.

Description: Selects the slew rate for the SDO pin. Fast slew rate is recommended for SCLK frequencies greater than TBD Hz.

[DR4MA] [DR2MA]

DR2MA	DR4MA	Output
0	0	2mA
1	0	4mA*
0	1	6mA
1	1	8mA

Description: Configures the output driver current for the SDO pin.

10.3 Coefficient Memory

Accessing the coefficient memory uses an SPI access as shown below.

Table 5 FIR Coefficient Memory Access Format

	OPCODE	ADDRESS	UNUSED	DATA
Number of bits	8 bits	14 bits	2 bits	32 bits per memory location*
Write Access	86h	0000h – 00FFh	Don't care	0000h – FFFFh
Read Access	87h	0000h – 00FFh	Don't care	0000h – FFFFh

Note: * Multiple memory locations can be written/read by extending the SPI access cycle.

0000h – 0400h COEF_RAM (FIR Filter Coefficient Memory)

	Bit 31 – Bit 0
Address 0000h – 00FFh	Data 31 – Data 0

Description: FIR filter coefficient memory.

11 Operating Mode Configurations

Note: Data paths in bold, Control paths in regular. Filter data in blue, configuration data in orange.

11.1 SPI FIR Coprocessor Mode

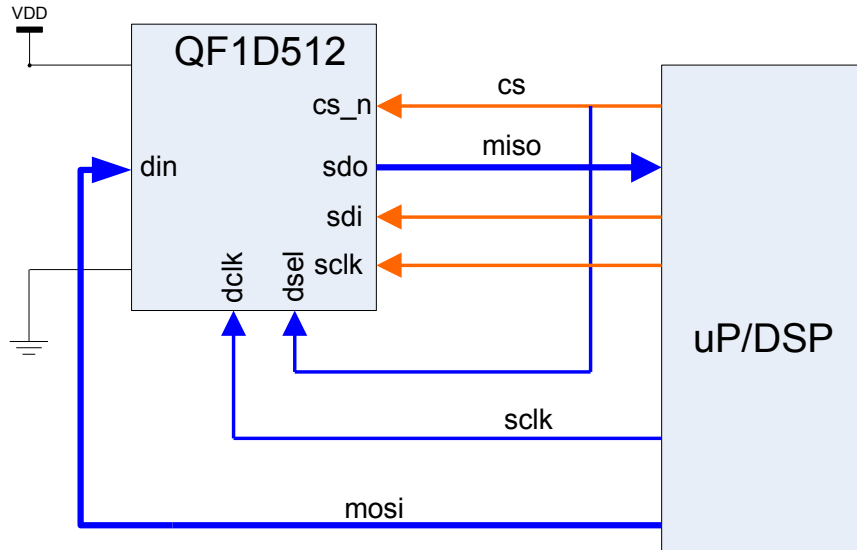


Figure 17: SPI FIR Coprocessor Mode

11.2 Inline Normal SPI Mode

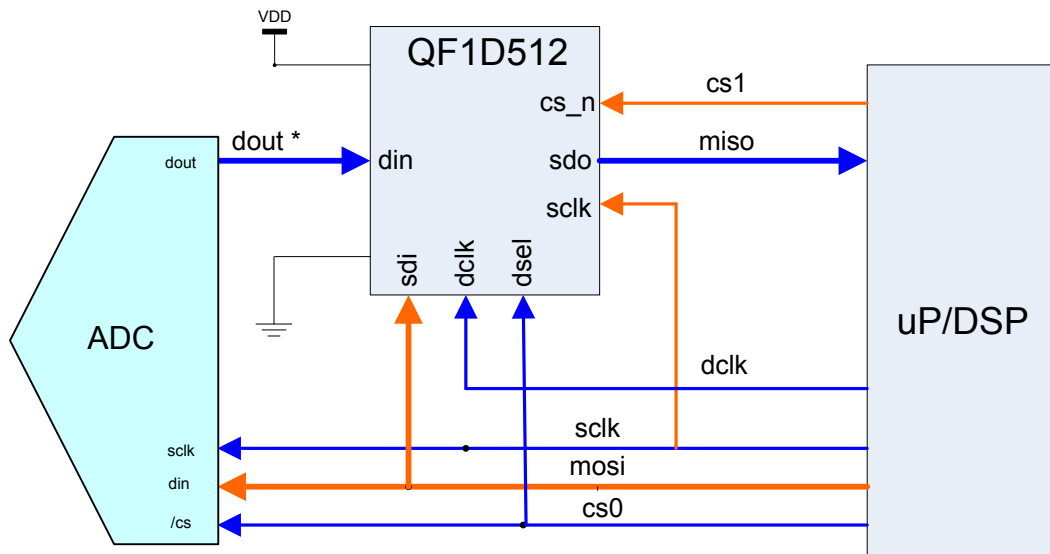


Figure 18: Inline Normal SPI Mode

11.3 Inline Continuous SPI Mode (CS_N tied to GND)

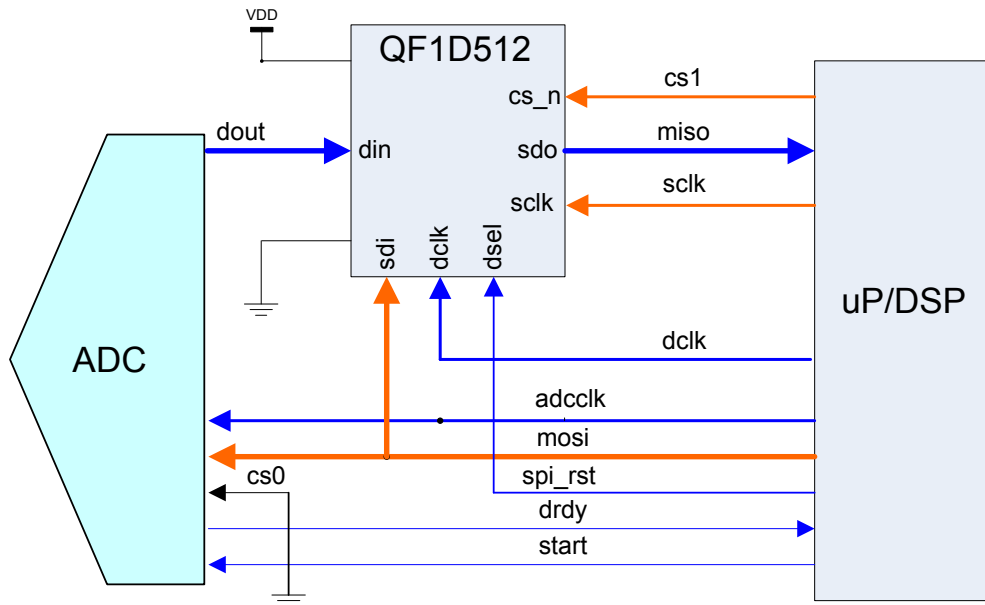


Figure 19: Inline Continuous SPI Mode

11.4 Inline Synchronous Serial Mode (uP clock slave)

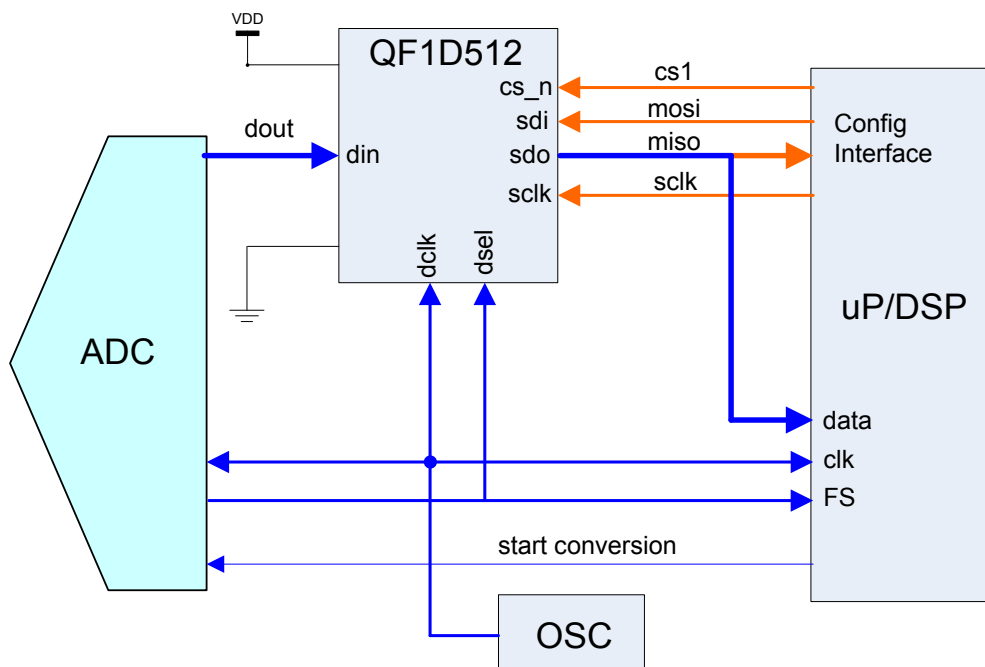


Figure 20: Inline Synchronous Serial Mode

11.5 Inline SPI DAC

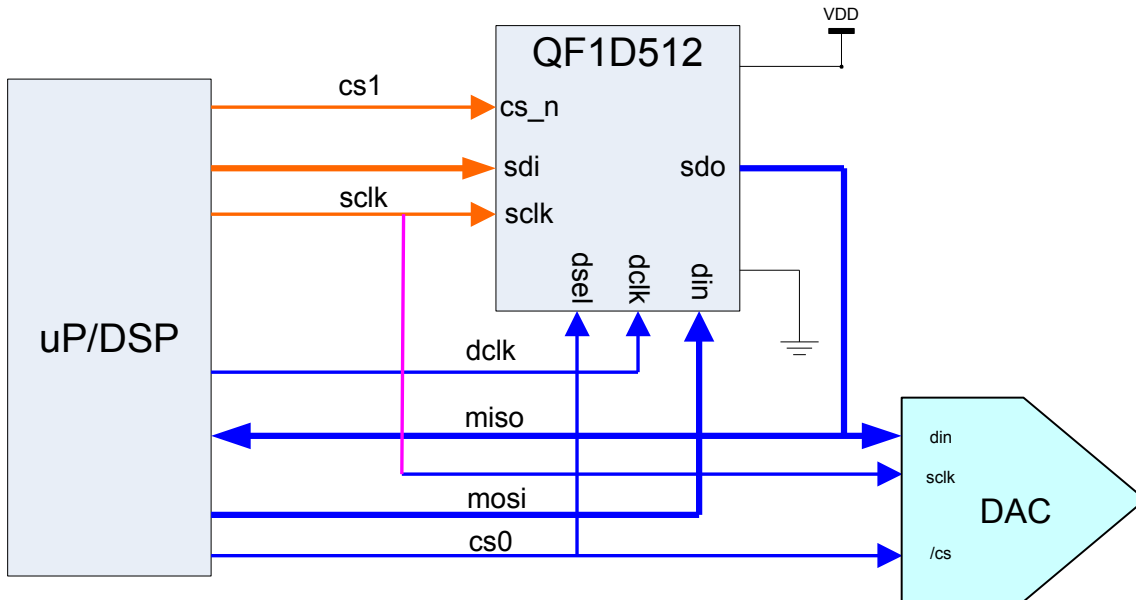


Figure 21: Inline SPI DAC

11.6 ADC Configuration Read / Write – QF1D512 Passthrough

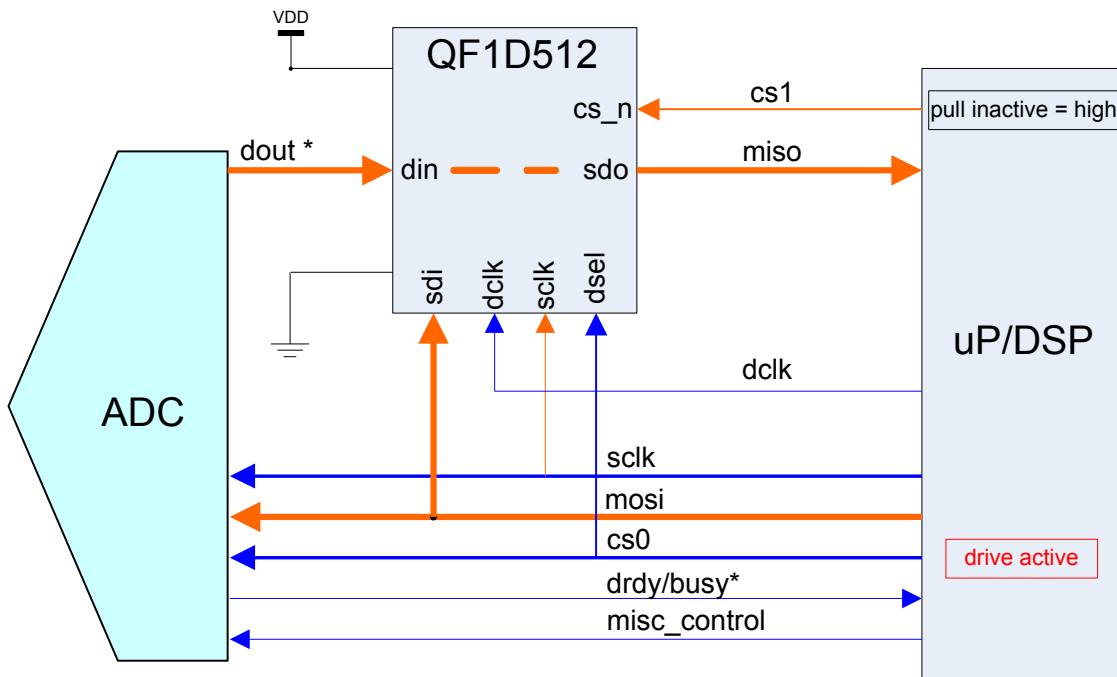


Figure 22: ADC Configuration Read / Write

11.7 QF1D512 Configuration Mode

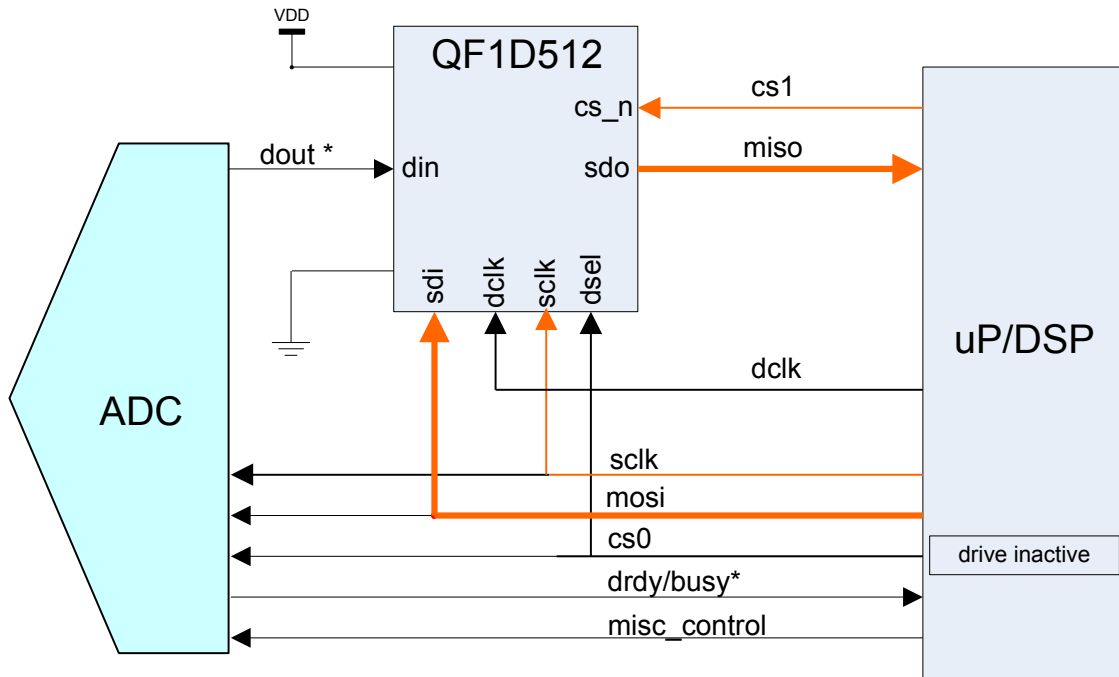


Figure 23: QF1D512 Configuration Read / Write

12 Packaging Information

3 x 3 x 0.9mm, VQFN 16, 0.8 mm Pull Back Lead (JEDEC)

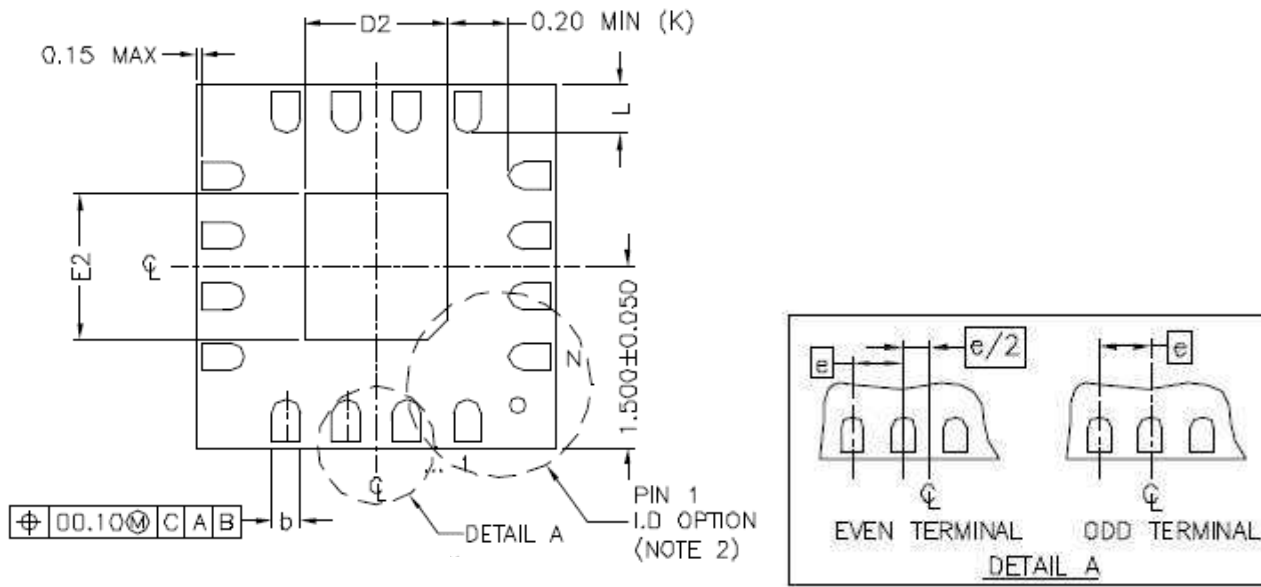


Figure 24: VQFN 16, Bottom View

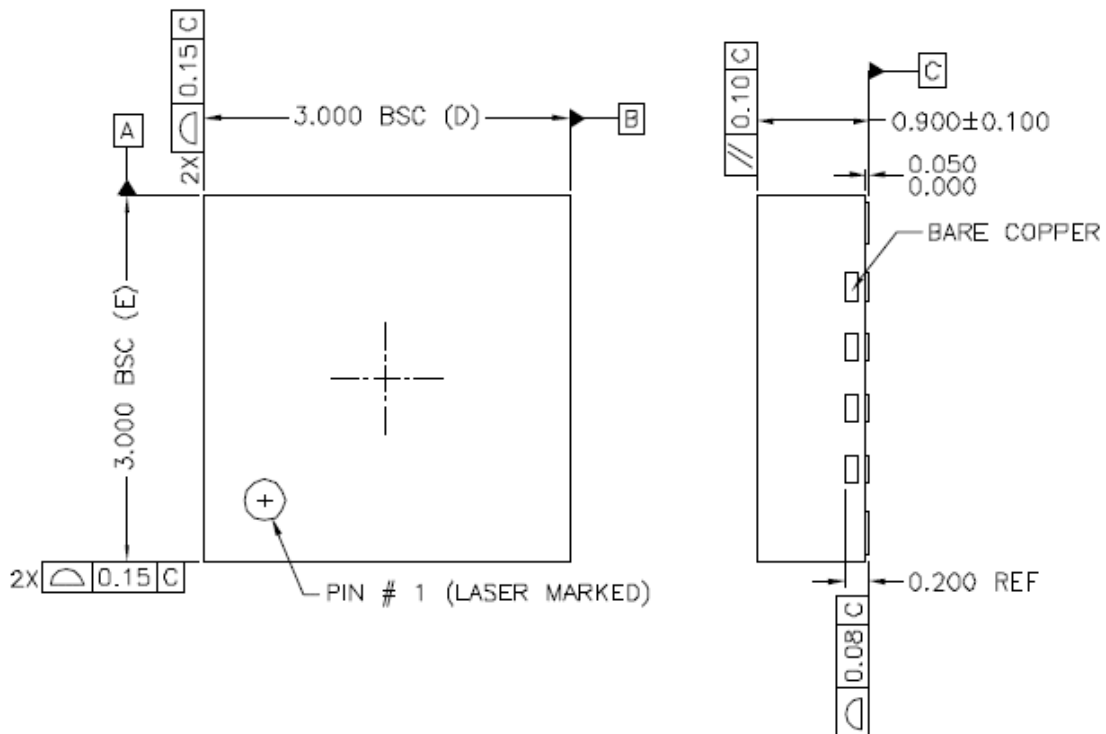


Figure 25: VQFN 16, Top/Side View

Table 6 VQFN 16, Dimensions

SYMBOL \ VARIATION	BB		
	MIN	NOM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
E2	1.60	1.70	1.80
D2	1.60	1.70	1.80
L	0.35	0.40	0.45
N	16 LD		
ND	4		
NE	4		
JEDEC VARIATION	VEED-4		
INTERNAL FEATURE	STANDARD		
LF P/N	PPF	16-016-003	
	AG SPOT	N/A	
	AG RING	A 16-016-091	
PKG CODE	VQ 016		

Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerance per ASME Y14.5M-1994
3. For PCB layout, it is recommended that no pad, solder paste, vias, or traces be placed under the part.

Registers, Tables, and Lists

Control Register Listing

00h TEST_RW (User Register)	22
01h CHIP_ID (Chip ID) - READ ONLY	22
02h VERSION (Version) - READ ONLY	22
03h CONTROL (Filter/Pass Through Control)	22
04h DCONFIG (Data Format Control)	23
05h FCONFIG (Filter Control).....	23
06h NUM_TAPS (Number of FIR Filter Taps, Lower Bits).....	24
07h NUM_TAPS (Number of FIR Filter Taps, Upper Bit)	24
08h DECIMATE (Down-sampling Rate).....	24
09h HD_OFFSET (Offset of Header Field)	24
0Ah HD_SIZE (Size of Header Field)	24
0Bh HD_MASK (Header Data Valid Mask).....	25
0Ch HD_VALUE (Header Data Valid Value)	25
0Dh DATA_OFFSET (Offset of Data Field)	25
0Eh DATA_SIZE (Number of Bits in the Data Field).....	25
0Fh TEST (Chip Test Register) – RESERVED Y	25
10h IO_TDT (TST Pin Configuration)	26
11h IO_RST_N (RST_N Pin Configuration).....	26
12h IO_DCLK (DCLK Pin Configuration).....	26

13h IO_DSEL (DSEL Pin Configuration)	27
14h IO_DIN (DIN Pin Configuration).....	27
15h IO_CS_N (CS_N Pin Configuration)	28
16h IO_SCLK (SCLK Pin Configuration)	28
17h IO_SDI (SDI Pin Configuration)	28
18h IO_SDO (SDO Pin Configuration).....	29

List of Tables

Table 1 Pin Descriptions	8
Table 2 Register and Memory Format	21
Table 3 Control Registers	21
Table 4 Configuration Register Access Format	22
Table 5 FIR Coefficient Memory Access Format	30
Table 6 VQFN 16, Dimensions	36

List of Figures

Figure 1: 16 Pin QFN Package Pin out.....	8
Figure 2: Functional Block Diagram	9
Figure 3: Configuration Data Timing	11
Figure 4: Configuration Interface Transfer Format.....	11
Figure 5: I2C Master/Slave Interaction	12
Figure 6: I2C Master/Slave Command/Response Timing.....	12
Figure 7: I2C to SPI Bridge Circuit.....	13
Figure 8: I2C Addressing Protocol	13
Figure 9: Interface Modes	15
Figure 10: Data Format Selection	16
Figure 11: Data Interface Timing Diagram	16
Figure 12: Data Interface Transfer Format	17
Figure 13: Data Header Masking Example	17
Figure 14: SDO Functionality – FIR Coprocessor and SPI Modes	18
Figure 15: SDO Functionality – Sync Serial Mode.....	18
Figure 16: Averaging /Down-sampler Block Diagram	19
Figure 17: SPI FIR Coprocessor Mode.....	31
Figure 18: Inline Normal SPI Mode	31
Figure 19: Inline Continuous SPI Mode	32
Figure 20: Inline Synchronous Serial Mode	32
Figure 21: Inline SPI DAC	33
Figure 22: ADC Configuration Read / Write	33
Figure 23: QF1D512 Configuration Read / Write	34
Figure 24: VQFN 16, Bottom View.....	35
Figure 25: VQFN 16, Top/Side View.....	35

The contents of this document are provided in connection with Quickfilter Technologies, Inc. products. Quickfilter makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel or otherwise, to any intellectual property rights is granted by this publication. Except as set forth in Quickfilter's Standard Terms and Conditions of Sale, Quickfilter assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

Quickfilter's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of Quickfilter's product could create a situation where personal injury, death, or severe property or environmental damage may occur. Quickfilter reserves the right to discontinue or make changes to its products at any time without notice.

© 2008 Quickfilter Technologies, Inc.
All rights reserved.

1024 S. Greenville Ave
Suite 130
Allen, TX 75002-3344

Telephone: (214) 547-0460
Fax: (214) 547-0481

For inquiries, please contact Quickfilter at the above address,

Or visit our website:
<http://www.quickfiltertech.com>

Quickfilter, the Quickfilter logo and "Programmable Signal Converter", and combinations thereof, are trademarks of Quickfilter Technologies, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.