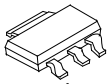
FS0203 **Preliminary** ***SCR***

SURFACE MOUNT SCR



SOT-223

■ DESCRIPTION

The UTC **FS0203** is a surface mount SCR, it uses UTC's advanced technology to provide customers with high gate sensitivity, etc.

■ FEATURES

* High gate sensitivity

■ ORDERING INFORMATION

Ordering Number		Package	Pin assignment			Packing
Lead Free Plating	Halogen Free		1	2	3	
FS0203L-x-AA3-R	FS0203G-x-AA3-R	SOT-223	K	A	G	Tape Reel

FS0203L-x-AA3-R (1)Packing Type (2)Package Type (3)V_{DRM}, V_{RRM} (4)Lead Free	(1) R: Tape Reel (2) AA3 : SOT-223 (3) 2: 200V, 4: 400V, 6: 600V, 8: 800V, 9:900V (4) L: Lead Free, G: Halogen Free

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■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive Peak Off State Voltage (R_{GK}=1kΩ)	FS0203-2	V_{DRM}, V_{RRM}	200	V
	FS0203-4		400	V
	FS0203-6		600	V
	FS0203-8		800	V
	FS0203-9		900	V
Average On-State Current (Note 1)	Half Cycle, θ=180 º T_{TAB}=95˚C	$I_{T(AV)}$	1.25	A
On-State Current (Note 1)	Half Cycle, θ=180 º T_{TAB}=95˚C	$I_{T(RMS)}$	0.8	A
Non-Repetitive On-State Current	Half Cycle, 60Hz, T_J=25ºC	I_{TSM}	25	A
	Half Cycle, 50Hz, T_J=25ºC		22.5	A
I^2t Value for Fusing	t_p=10ms, Half Cycle	I^2t	2.5	A^2s
Peak Reverse Gate Voltage	I_{GR}=10μA, T_J=25ºC	V_{GRM}	8	V
Peak Gate Current	20μs max.	I_{GM}	1.2	A
Peak Gate Power	20μs max.	P_{GM}	3	W
Average Gate Power Dissipation	20ms max.	$P_{G(AV)}$	0.2	W
Operating Junction Temperature		T_J	-40~+125	℃
Storage Junction Temperature		T_{STG}	-40~+150	℃
Soldering Temperature	10s max.	T_{SLD}	260	℃

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. With 5cm^2 copper (e=35μm) surface under tab.

■ THERMAL RESISTANCES

PARAMETER	SYMBOL	RATINGS	UNIT
Junction-Leads for DC	$θ_{JL}$	25	℃/W
Junction to Ambient	$θ_{JA}$	60	℃/W

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off-State Leakage Current	I_{DRM}/I_{RRM}	V_D=V_{DRM}, R_{GK}=1KΩ, T_J=125ºC			500	μA
		V_R=V_{RRM}, T_J=25ºC			5	μA
On-State Voltage	V_{TM}	at I_T=1.6A, t_p=380μs, T_J=25ºC			1.45	V
On-State Threshold Voltage	$V_{T(O)}$	T_J=125ºC			0.9	V
Dinamic Resistance	R_D	T_J=125ºC			150	mΩ
Gate Trigger Current	I_{GT}	V_D=12V_{DC}, R_L=140Ω, T_J=25ºC	20		200	μA
Gate Trigger Voltage	V_{GT}	V_D=12V_{DC}, R_L=140Ω, T_J=25ºC			0.8	V
Gate Non-Trigger Voltage	V_{GD}	V_D=V_{DRM}, R_L=3.3KΩ, R_{GK}=1KΩ, T_J=125℃	0.1			V
Holding Current	I_H	I_T=50mA, R_{GK}=1KΩ, T_J=25ºC			5	mA
Latching Current	I_L	I_G=1mA, R_{GK}=1KΩ, T_J=25ºC			6	mA
Critical Rate of Rise of Off-State Voltage	dv/dt	V_D=67%×V_{DRM}, R_{GK}=1KΩ, T_J=125℃	20			V/μs
Critical Rate of Current Rise	di/dt	I_G=2xI_{GT}, T_R≤100ns, F=60Hz, T_J=125℃	50			A/μs

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