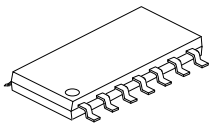
M1725 *CMOS IC*

16-BIT,96KHZ STEREO AUDIO D/A CONVERTER



SOP-14

■ DESCRIPTION

The UTC **M1725** is a complete stereo digital-to-analog output system including a 16-bit D/A conversion, a 5-level 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier in a small 14-pin package.

The UTC **M1725** can be operating with from a single 5V power supply and requires minimal support circuitry. These features are ideal for set-top boxes, DVD players and A/V receivers, etc.

■ FEATURES

* Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
* 16-Bit Conversion
* 95dB Dynamic Range
* Single +5V Power Supply
* 16kHz to 96kHz Multiple Sampling Frequencies
* 8X Oversampling Digital Filter
* 256 f_S /384 f_S System Clock
* Normal or I^2S Data Input Formats

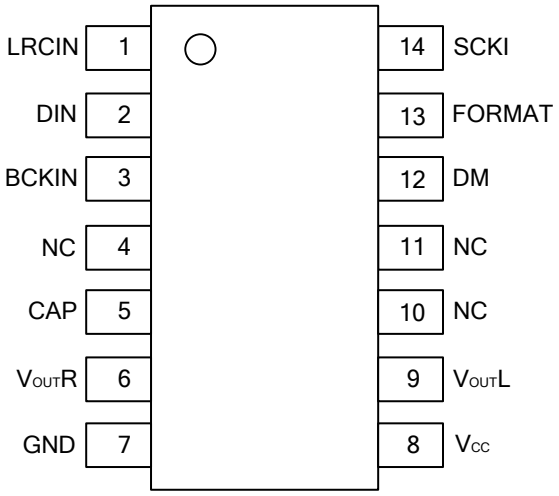
■ ORDERING INFORMATION

Ordering Number	Package	Packing
M1725G-S14-R	SOP-14	Tape Reel

M1725G-S14-T
- (1)Packing Type
- (2)Package Type
- (3)Halogen Free

(1) R: Tape Reel
(2) S14: SOP-14
(3) G: Halogen Free

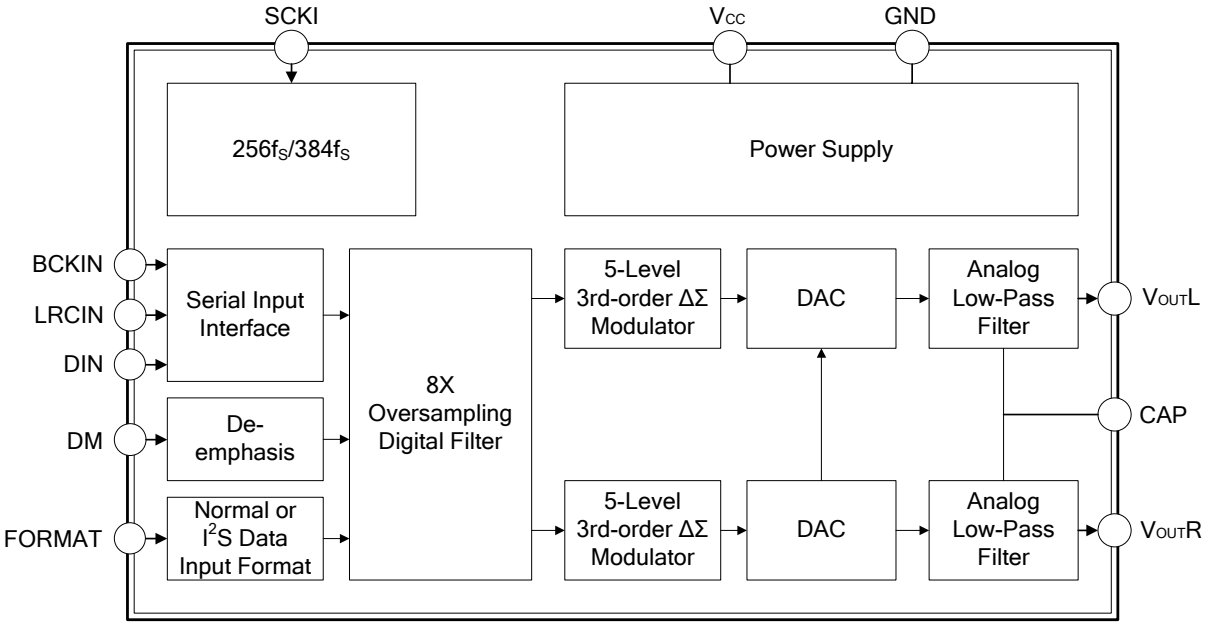
■ PIN CONFIGURATIONS



■ PIN DESCRIPTION

PIN NO	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	LRCIN	I	Left/Right Clock Input
2	DIN	I	Serial Audio Data Input
3	BCKIN	I	Bit Clock Input for Audio Data
4	NC	--	No Connection
5	CAP	I/O	Common Pin of Analog Output Amp
6	$V_{OUT}R$	O	Right-Channel Analog Output
7	GND	I/O	Ground
8	V_{CC}	I/O	Power Supply
9	$V_{OUT}L$	O	Left-Channel Analog Output
10	NC	--	No Connection
11	NC	--	No Connection
12	DM	I	De-emphasis Control High: De-emphasis OFF Low: De-emphasis ON(44.1kHz)
13	FORMAT	I	Audio Data Format Select High: I^2S Data Format Low: Standard Data Format
14	SCKI	I	System Clock Input (256 f_S or 384 f_S)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{CC}	+6.5	V
+ V_{CC} to+ V_{DD} Difference	V_D	±0.1	V
Input Logic Voltage	V_{LGC}	-0.3V to (V_{DD} +0.3V)	W
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_{OPR}	-25 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Junction Temperature	T_J	-25 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +100	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	70	°C/W

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC}=+5V, f_S=44.1kHz, CAP=10uF, 16-Bit Input Data, SCKI=384 f_S, unless otherwise specified)

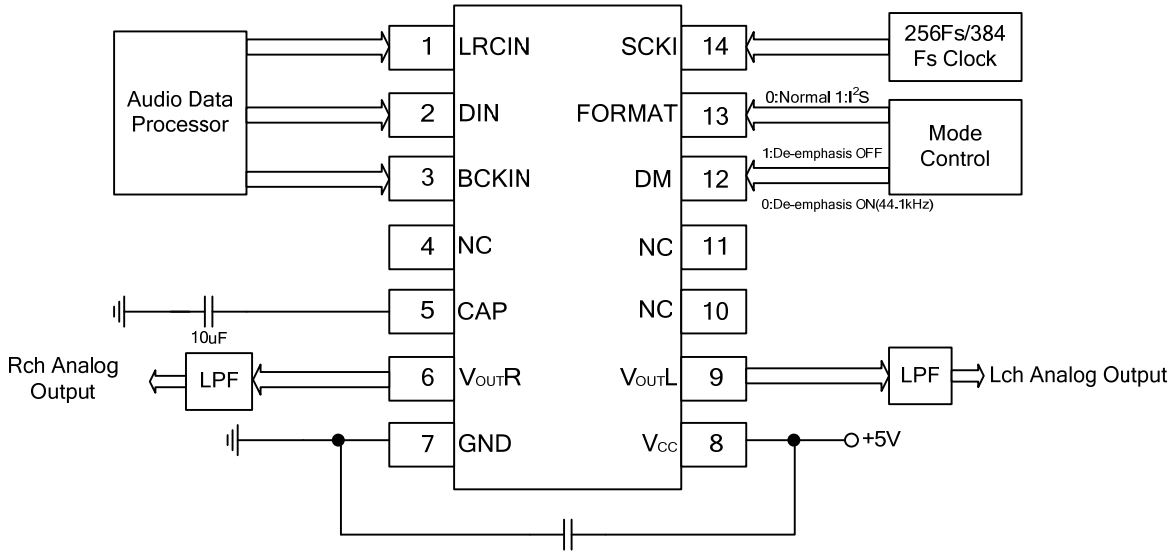
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA FORMAT						
Data Bit Length					16	Bits
Input sample Rate	f_S		16		96	kHz
Internal System Clock Frequency	SCKI			256/384		f_S
DIGITAL INPUT/OUTPUT						
Logic Level				TTL		
Input Logic Level (Note1)	V_{IH}		2			V
	V_{IL}				0.8	V
Input Logic Current (Note1)	I_{IN}				±0.8	uA
DYNAMIC PERFORMANCE (Note2)						
THD+N at FS (0dB)		f=991kHz		-83	-78	dB
THD+N at -60dB		f=991kHz		-32		dB
Dynamic Range	DR	f=991kHz,A-weighted	90	95		dB
Signal-to-Noise Ratio	SNR	f=991kHz,A-weighted	90	97		dB
Channel Separation	CS	f=991kHz	88	95		dB
DC ACCURACY						
Gain Arror				±1.0	±5.0	% of FSR
Gain Mis-match(Channel-to-Channel)				±1.0	±5.0	% of FSR
Bipolar Zero Error	BZE	V_{OUT}=Vcc/2 at BPZ		±20	±50	mV
ANALOG OUTPUT						
Output Voltage	V_O	Full Scale(0dB)		0.62*Vcc		V_{P-P}
Center Voltage	V_C			Vcc/2		V
Load Impedance	R_L	AC Load	10			kΩ

Note: 1. Pins 1, 2, 3, 12, 13: LRCIN, DIN, BCKIN, DM, FORMAT (Schmitt Trigger Input); Pin 14: SCKI.
2. Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

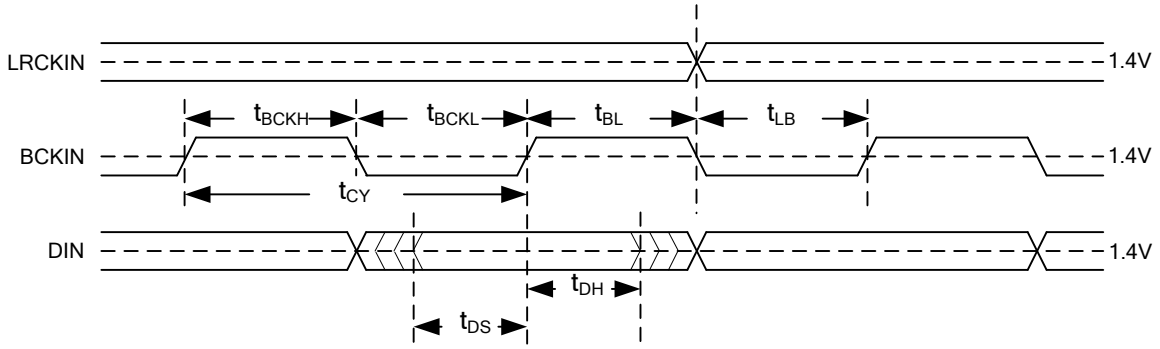
■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL FILTER PERFORMANCE						
Passband					0.445	f_S
Stopband			0.555			f_S
Passband Ripple					±0.17	dB
Stopband Attenuation			-35			dB
Delay Time	T_D			11.125/ f_S		Sec
INTERNAL ANALOG FILTER						
-3dB Bandwidth				100		kHz
Passband Response		f=20kHz		-0.16		dB
POWER SUPPLY REQUIREMENTS						
Voltage Range	V_{CC}		4.5	5	5.5	V
Supply Current	I_Q			13	18	mA
Power Dissipation	P_D			65	90	mW

■ TYPICAL APPLICATIONS CIRCUIT



■ TIMING DIAGRAMS



t_{CY}	BCKIN Pulse Cycle Time	⩾100ns
t_{BCKH}	BCKIN Pulse Width High	⩾50ns
t_{BCKL}	BCKIN Pulse Width Low	⩾50ns
t_{BL}	BCKIN Rising Edge to LRCIN Edge	⩾30ns
t_{LB}	LRCIN Edge to BCKIN Rising Edge	⩾30ns
t_{DS}	DIN Set Up Time	⩾30ns
t_{DH}	DIN Hold Time	⩾30ns

Figure 1.Audio Data Input Timing

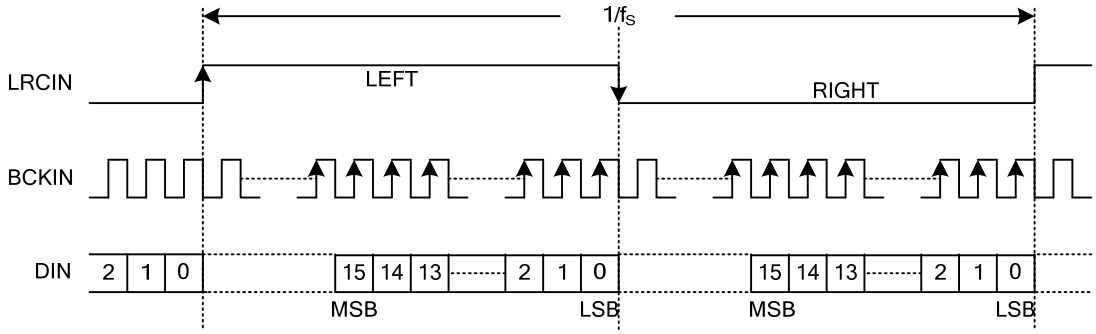


Figure 2.Normal Data Input Timing

■ TIMING DIAGRAMS (Cont.)

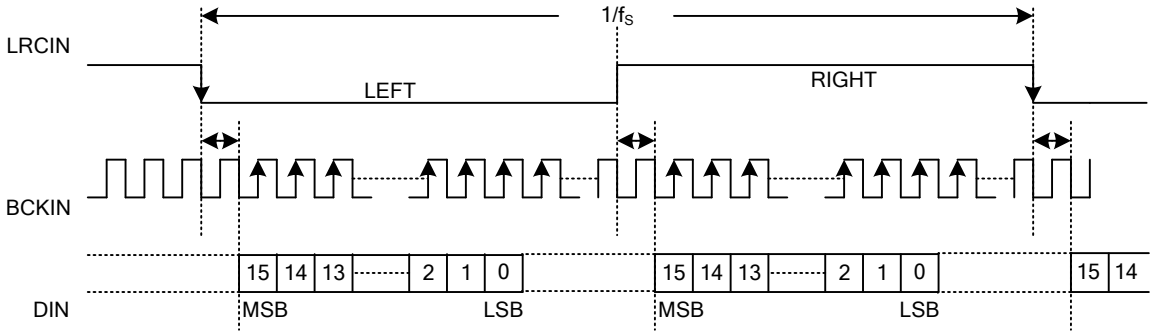
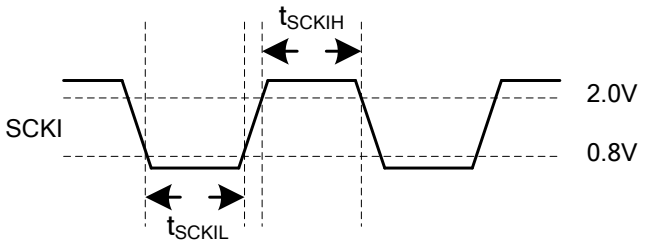


Figure 3. I²S Data Input Timing



t_{SCKIH}	System Clock Pulse Width High	⩾13ns
t_{SCKIL}	System Clock Pulse Width Low	⩾13ns

Figure 4. System Clock Timing

■ FUNCTIONAL DESCRIPTION

SYSTEM CLOCK

The system clock (SCKI) must be either 256 f_S or 384 f_S, where f_S is the audio sampling frequency (LRCIN),typically 32kHz, 44.1kHz or 48kHz. The system clock is used to operate the digital filter and the noise shaper. Timing conditions for SCKI are shown in **Figure4**.

M1725 includes a system clock detection circuit which auto-matically detects the frequency, either 256 f_S or 384 f_S. The system clock should be synchronized with LRCIN,but **M1725** can compensate for phase differences. If the phase difference between LRCIN and system clock is greater than ±6 bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state (VCC/2) during the synchronization function. The typical system clock frequency inputs vs sampling rate for the **M1725** is shown below.

SAMPLING RATE(LRCIN)(kHz)	SYSTEM CLOCK FREQUENCY(MHz)	
	256 f_S	384 f_S
32	8.192	12.288
44.1	11.2896	16.934
48	12.288	18.432

INPUT DATA FORMAT

M1725 can accept input data in either normal (MSB-first, right-justified) or I^2S format by applying LOW or HIGH voltage level on FORMAT-pin.

FORMAT	INPUT DATA FORMAT SELECTED
Low	Normal Format (MSB-first, right-justified)
High	I2S Format (Philips serial data protocol)

DE-EMPHASIS CONTROL

DM-pin enables **M1725**'s de-emphasis function. De-emphasis operates only at 44.1kHz.

DM	DE-EMPHASIS FUNCTION SELECTED
Low	De-emphasis ON (44.1kHz)
High	De-emphasis OFF

RESET

M1725 includes an internal power-on reset circuit. The power-on reset initializes and has an initialization period equal to 1024 system clock periods after V_{CC}>2.2V. During the initialization period, the DAC outputs are invalid, and the analog outputs are forced to VCC/2.