UT138E

TRIAC

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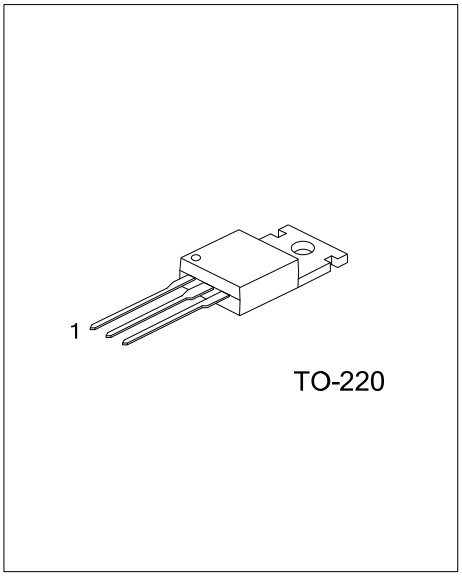
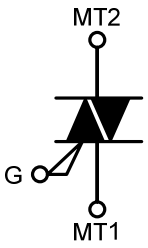


TO-220

■ DESCRIPTION

Glass passivated , sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT138EL-x-TA3-T	UT138EG-x-TA3-T	TO-220	MT1	MT2	G	Tube

UT138EL-x-TA3-T (1)Packing Type (2)Package Type (3)Voltage (4)Lead Free	(1) T: Tube (2) TA3: TO-220 (3) 5: 500V, 6: 600V, 8: 800V (4) L: Lead Free, G: Halogen Free

■ ABSOLUTE MAXIMUM RATING (T_J=25°C)

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive Peak Off State Voltag	UT138E-5	V_{DRM}	500	V
	UT138E-6		600	V
	UT138E-8		800	V
RMS On-state Current (Full sine wave, T_{MB}≤99°C)		$I_{T(RMS)}$	12	A
Non-Repetitive Peak. On-State Current	t=20mS	I_{TSM}	95	A
(Full sine wave, T_J=25°C prior to surge)	t=16.7mS		105	A
I^2t For Fusing (t=10ms)		I^2t	45	A^2s
Repetitive Rate of Rise of On-state Current After Triggering (I_{TM}=20A, I_G=0.2A, dI_G/dt=0.2A/μs)	T2+ G+	dI_T/dt	50	A/μs
	T2+ G-		50	A/μs
	T2- G-		50	A/μs
	T2- G+		10	A/μs
Peak Gate Voltage		V_{GM}	5	V
Peak Gate Current		I_{GM}	2	A
Peak Gate Power		P_{GM}	5	W
Average Gate Power (Over any 20ms period)		$P_{G(AV)}$	0.5	W
Operating Junction Temperature		T_J	125	°C
Storage Temperature		T_{STG}	-40~150	°C

Notes: Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

■ THERMAL RESISTANCES

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to Mounting Base	Full cycle	$θ_{JC}$			1.5	K/W
	Half cycle				2.0	
Thermal Resistance, Junciton to Ambient In free air		$θ_{JA}$		60		K/W

■ STATIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gate Trigger Current	I_{GT}	V_D=12V, I_T=0.1A	T2+ G+		2.5	10	mA
			T2+ G-		4.0	10	
			T2- G-		5.0	10	
			T2- G+		11	25	
Latching Current	I_L	V_D=12V, I_{GT} =0.1A	T2+ G+		3.2	30	mA
			T2+ G-		16	40	
			T2- G-		4.0	30	
			T2- G+		5.5	40	
Holding Current	I_H	V_D=12V, I_{GT}=0.1A			4.0	30	mA
On-State Voltage	V_T	I_T=15A			1.4	1.65	V
Gate Trigger Voltage	V_{GT}	V_D=12V, I_T=0.1A			0.7	1.5	V
		V_D=400V, I_T=0.1A, T_J=125°C		0.25	0.4		V
Off-state Leakage Current	I_D	V_D=$V_{DRM(max)}$, T_J=125°C			0.1	0.5	mA

■ DYNAMIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate Of Rise Of Off-State Voltage	dV_D/dt	V_{DM}=67% $V_{DRM(max)}$, T_J=125°C Exponential waveform, Gate open circuit		50		V/μs
Gate Controlled Turn-on Time	t_{gt}	I_{TM}=16A, V_D=$V_{DRM(max)}$, I_G=0.1A dI_G/dt=5A/μs		2		μs

■ TYPICAL CHARACTERISTICS

Figure 1. Maximum On-State Dissipation. P_{tot} vs RMS On-state Current, $I_{T(RMS)}$, Where α=Conduction Angle.

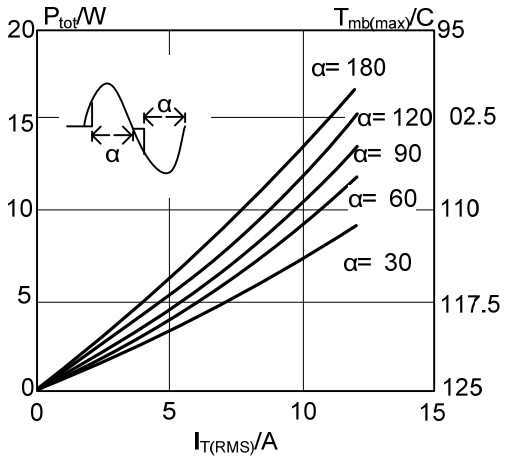


Figure 2. Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM}, vs Pulse Width t_p, for Sinusoidal Currents, t_p≦20ms.

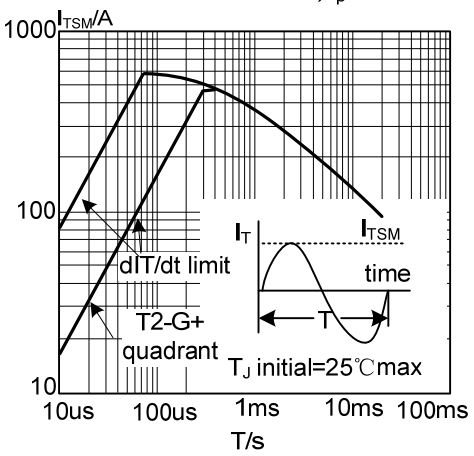


Figure 3 .Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM}, vs Number of Cycles, for Sinusoidal Currents, f=50Hz.

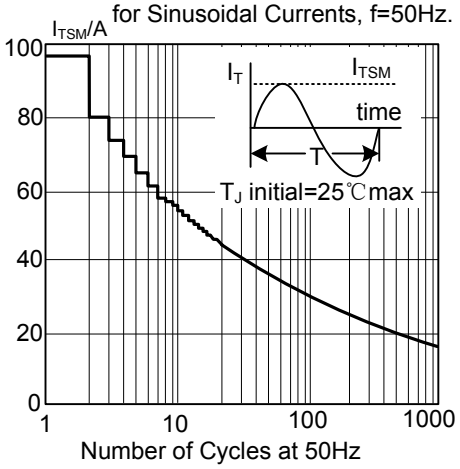


Figure 4. Maximum Permissible RMS Current $I_{T(RMS)}$ vs Mounting Base Temperature T_{mb}

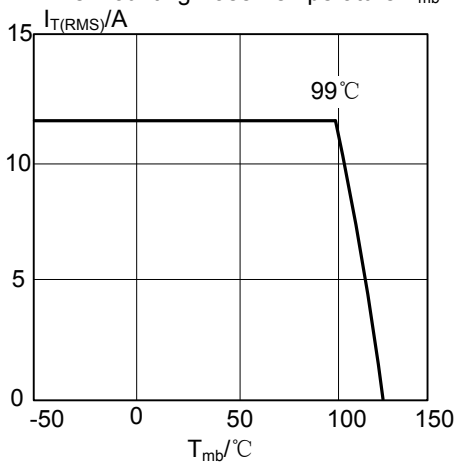


Figure 5. Maximum Permissible Repetitive RMS On-State Current $I_{T(RMS)}$, vs Surge Duration, for Sinusoidal Currents,f =50Hz, T_{mb}≦99℃

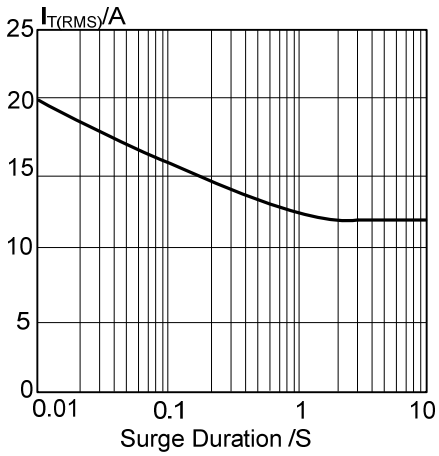
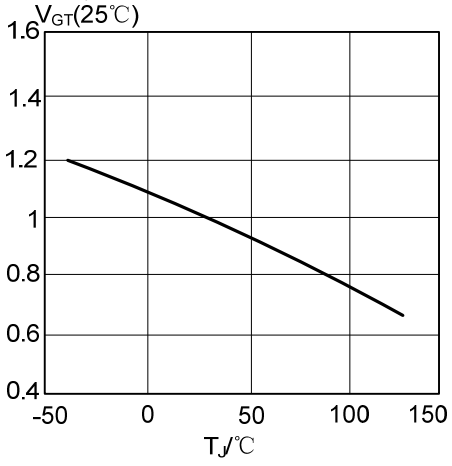


Figure 6. Normalised Gate Trigger Voltage $V_{GT}(T_J)/V_{GT}(25℃)$, vs Junction Temperature T_J



■ TYPICAL CHARACTERISTICS(Cont.)

Figure 7. Normalised Gate Trigger Current $I_{GT}(T_J)/I_{GT}(25°C)$, vs Junction Temperature T_J.

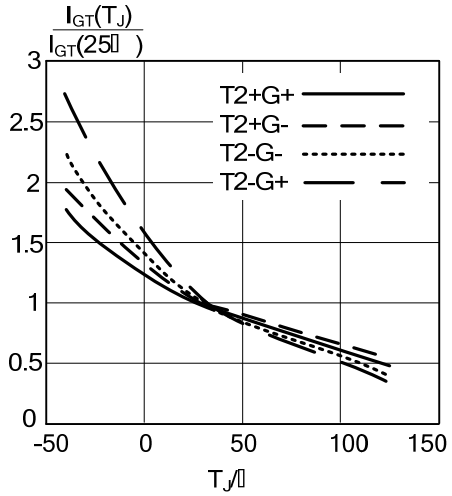


Figure 8. Normalised Latching Current $I_L(T_J)/I_L(25°C)$, vs Junction Temperature T_J

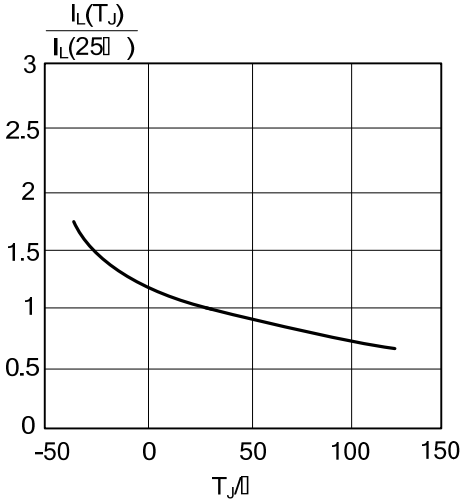


Figure 9. Normalised Holding Current $I_H(T_J)/I_H(25°C)$, vs Junction Temperature T_J

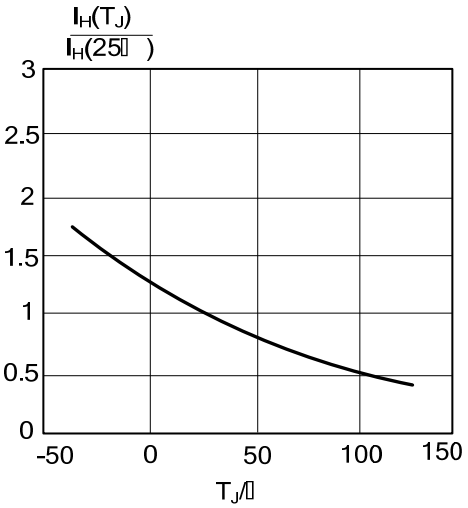


Figure 10. Typical and Maximum On-state Characteristic

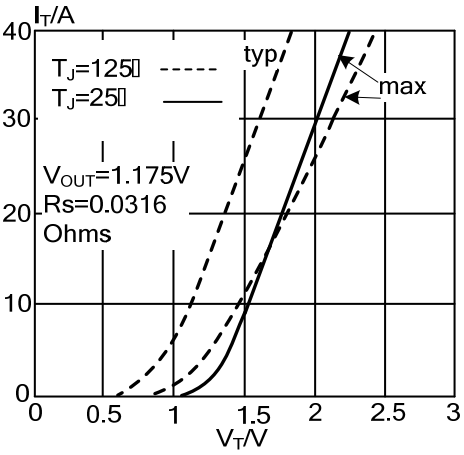


Figure 11. Transient Thermal Impedance $Z_{th\ j\text{-}mb}$, vs Pulse Width t_p

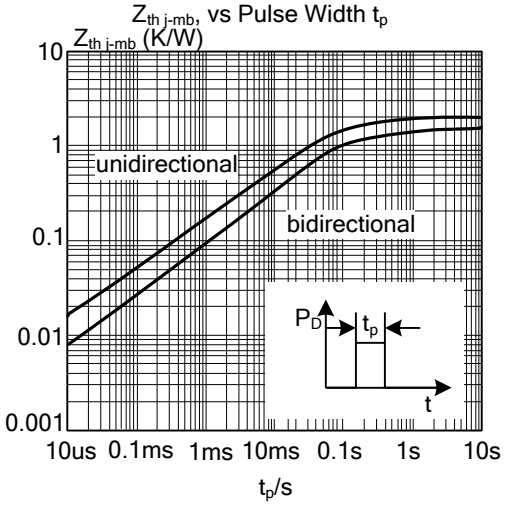


Figure 12. Typical Critical Rate of Rise of Off-State Voltage, dV_D/dt Versus Junction Temperature T_J