



U74HC14

CMOS IC

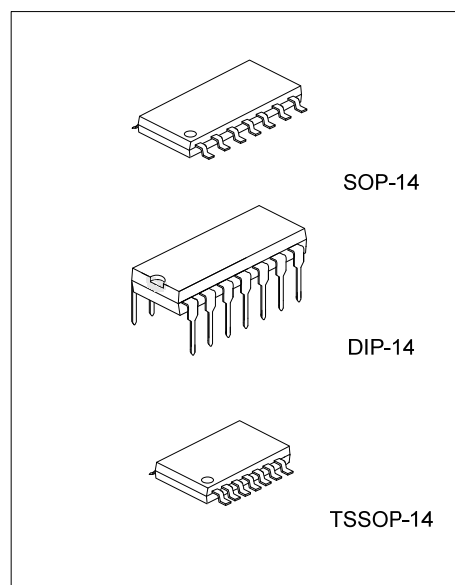
HIGH-SPEED CMOS LOGIC HEX INVERTING SCHMITT TRIGGER

■ DESCRIPTION

The UTC **U74HC14** each contain six inverting Schmitt triggers in one package. Each of them perform the Boolean function $Y=\overline{A}$.

■ FEATURES

- * Widely range of input rise and fall time
- * high noise immunity
- * Fan-out parameters(over temperature range)
up to 10 LSTTL Loads
- * Low power consumption
- * Wide range operation 2V ~ 6V



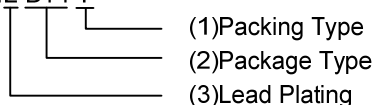
Lead-free: U74HC14L

Halogen-free: U74HC14G

■ ORDERING INFORMATION

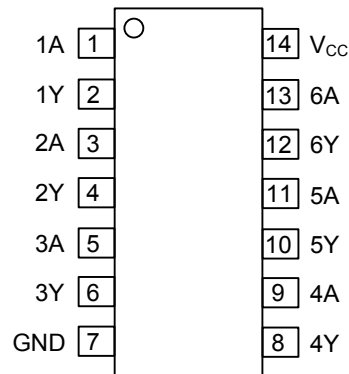
Ordering Number			Package	Packing
Normal	Lead Free Plating	Halogen Free		
U74HC14-D14-T	U74HC14L-D14-T	U74HC14G-D14-T	DIP-14	Tube
U74HC14-S14-R	U74HC14L-S14-R	U74HC14G-S14-R	SOP-14	Tape Reel
U74HC14-P14-R	U74HC14L-P14-R	U74HC14G-P14-R	TSSOP-14	Tape Reel

U74HC14L-D14-T

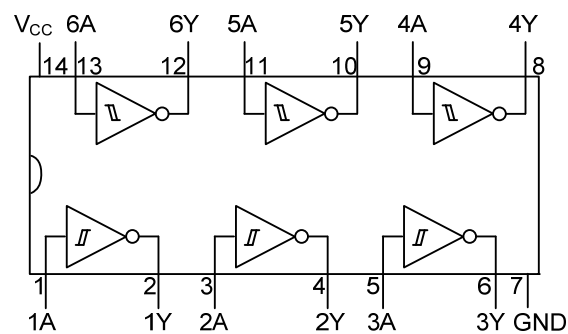


- (1) R: Tape Reel, T: Tube
(2) D14: DIP-14, S14: SOP-14, P14: TSSOP-14
(3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

■ PIN CONFIGURATION



■ FUNCTIONAL DIAGRAM



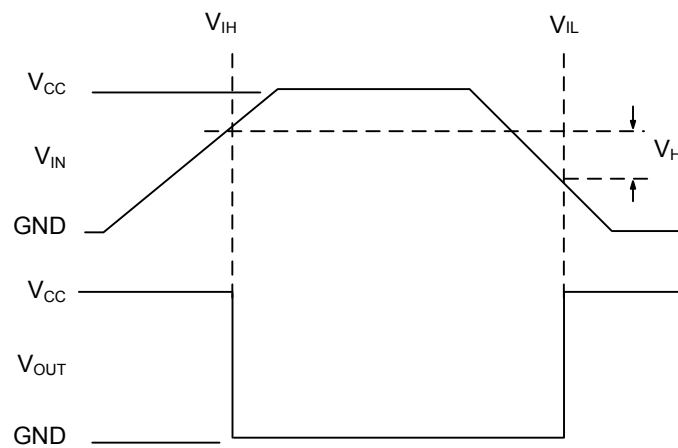
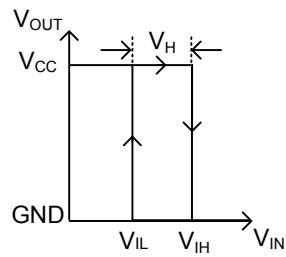
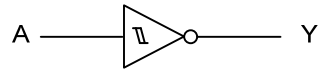
■ TRUTH TABLE

INPUT(A)	OUTPUT(Y)
L	H
H	L

H=High level

L=Low Level

■ LOGIC DIAGRAM



Hysteresis Definition, Characteristic, And Test Setup

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5V ~ 7V	V
Input Clamp Current	For $V_{IN} < 0$ or $V_{IN} > V_{CC}$	I_{IK}	± 20	mA
Output Clamp Current	For $V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	I_{OK}	± 20	mA
Continuous Output Current	For $V_{OUT} = 0$ to V_{CC}	I_{OUT}	± 25	mA
V_{CC} or Ground Current		I_{CC}	± 50	mA
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance Junction Ambient	DIP-14	θ_{JA}	80	°C/W
	SOP-14		76	°C/W
	TSSOP-14		113	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Range HC Types	V_{CC}		2	5	6	V
Input or Output Voltage	V_{IN}, V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		85	°C

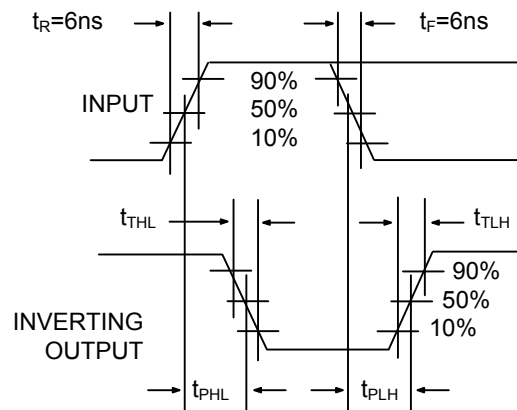
■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Switch Points	V_{IH}	$V_{CC}=2V$	0.7	1.2	1.5	
		$V_{CC}=4.5V$	1.55	2.5	3.15	
		$V_{CC}=6V$	2.1	3.3	4.2	
	V_{IL}	$V_{CC}=2V$	0.3	0.6	1	V
		$V_{CC}=4.5V$	0.9	1.6	2.45	V
		$V_{CC}=6V$	1.2	2	3.2	V
	V_{TH}	$V_{CC}=2V$	0.2	0.6	1.2	V
		$V_{CC}=4.5V$	0.4	0.9	2.1	V
		$V_{CC}=6V$	0.5	1.3	2.5	V
High Level Output Voltage CMOS Loads	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=2V$, $I_{OH}=-0.02mA$	1.9			V
		$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=4.5V$, $I_{OH}=-0.02mA$	4.4			V
		$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=6V$, $I_{OH}=-0.02mA$	5.9			V
High Level Output Voltage TTL Loads	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=4.5V$, $I_{OH}=-4mA$	3.98			V
		$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=6V$, $I_{OH}=-5.2mA$	5.48			V
Low Level Output Voltage CMOS Loads	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=2V$, $I_{OL}=0.02mA$			0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=4.5V$, $I_{OL}=0.02mA$			0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=6V$, $I_{OL}=0.02mA$			0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=4.5V$, $I_{OL}=4mA$			0.26	V
		$V_{IN}=V_{IH}$ or V_{IL} , $V_{CC}=6V$, $I_{OL}=5.2mA$			0.26	V
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ and GND, $V_{CC}=6V$			± 0.1	μA
Quiescent Device Current	I_Q	$V_{IN}=V_{CC}$ or GND, $V_{CC}=6V$, $I_{OUT}=0$			2	μA

■ SWITCHING SPECIFICATIONS ($T_A = 25^\circ\text{C}$, Input $t_R, t_F = 6ns$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay, A to Y	t_{PLH}, t_{PHL}	$V_{CC}=2V, C_L=50pF$		55	125	ns
		$V_{CC}=4.5V, C_L=50pF$		12	25	ns
		$V_{CC}=6V, C_L=50pF$		11	21	ns
Output Transition Times	t_{TLH}, t_{THL}	$V_{CC}=2V, C_L=50pF$		38	75	ns
		$V_{CC}=4.5V, C_L=50pF$		8	15	ns
		$V_{CC}=6V, C_L=50pF$		6	13	ns
Input Capacitance	C_{IN}			3	10	pF
Power Dissipation Capacitance	C_{PD}	No load		20		pF

■ TEST CIRCUIT AND WAVEFORMS



Transition Times And Propagation
Delay Times, Combination Logic

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