



U74CBT3126

Preliminary

CMOS IC

QUADRUPLE FET BUS SWITCH

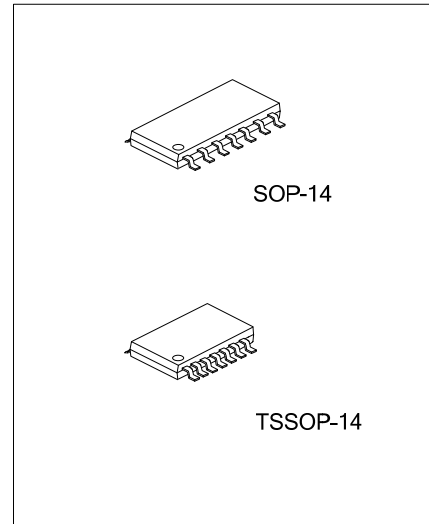
DESCRIPTION

The **U74CBT3126** is a quadruple line bus switch. It is composed of four 1-bit line switches with independent separate output-enable (OE) inputs. When OE is low, the switch is disabled.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor and the minimum value of the resistor is determined by the current-sourcing capability of the driver.

FEATURES

- * 5 Ω switch connection between two ports
- * Max t_{pd} of 0.25 ns at 5V
- * Low power consumption, $I_{CC} = 3 \mu A$ (Max.) at 5.5V
- * TTL compatible input levels

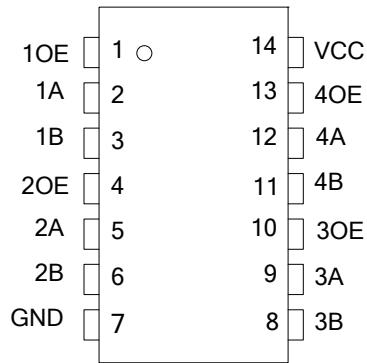


ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CBT3126L-P14-R	U74CBT3126G-P14-R	TSSOP-14	Tape Reel
U74CBT3126L-S14-R	U74CBT3126G-S14-R	SOP-14	Tape Reel

<p>U74CBT3126G-P14-R</p> <p>(1) Packing Type (2) Package Type (3) Halogen Free</p>	<p>(1) R: Tape Reel (2) P14: TSSOP-14, S14: SOP-14 (3) G: Halogen Free, L: Lead Free</p>
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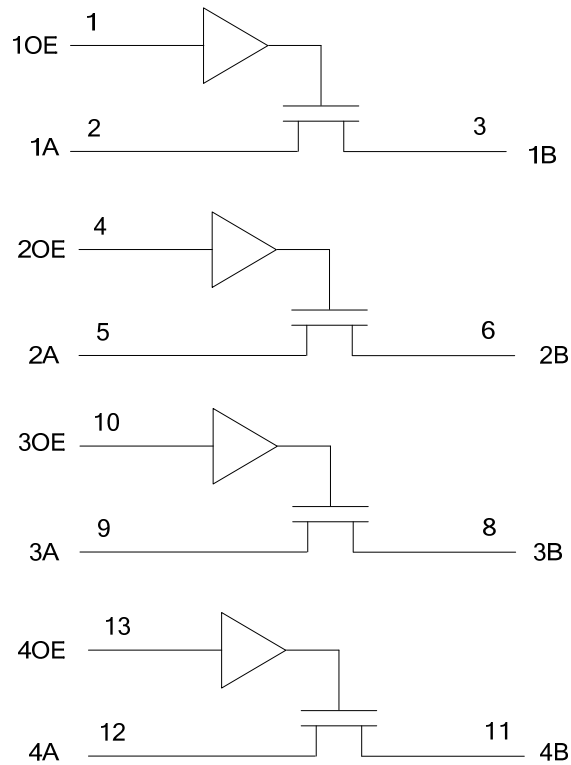
■ PIN CONFIGURATION



■ FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
L	Z
H	A=B

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{CC}	-0.5~7	V
Input Voltage	V _{IN}	-0.5~7	V
Supply Voltage	V _{CC}	4 ~ 5.5	V
Control Input Voltage	High	V _{IH}	2
	Low	V _{IL}	0.8
Input Clamp Current	I _{IK}	-50	mA
Continuous Channel Current	I _{CH}	128	mA
Power Dissipation T _{OPR} = -40°C to +125°C	SOP-14	P _D	600
	TSSOP-14		500
Operating Temperature	T _{OPR}	-40 ~ +85	°C
Storage Temperature	T _{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junctions to Ambient	SOP-14	θ _{JA}	139
	TSSOP-14		170

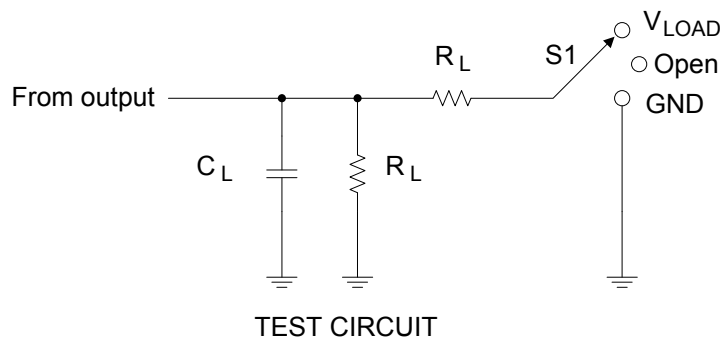
■ ELECTRICAL CHARACTERISTICS (T_A =25°C , V_{CC} = 5 V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input Diode Voltage	V _{IK}	V _{CC} = 4.5V, I _I = -18mA			-1.2	V
Input Leakage Current (OE inputs)	I _{I(LEAK)}	V _{CC} = 5.5V, V _{IN} = 5.5V or GND			±1	µA
Quiescent Supply Current	I _{CC}	V _{CC} = 5.5V, V _{IN} = 5.5V or GND, I _{OUT} = 0			3	µA
Additional quiescent Supply Current	Δ I _{CC}	V _{CC} = 5.5V, One input at 3.4V, Other inputs at V _{CC} or GND			2.5	mA
Input Capacitance (OE)	C _{IN}	V _{IN} = 3V or GND		3		pF
I/O Capacitance (OFF)	C _{IO}	V _{OUT} = 3V or GND, OE = GND		4		pF
Resistor between two ports	r _{on}	V _{CC} = 4V, V _{IN} = 2.4V, I _{IN} = 15mA, TYP at V _{CC} = 4V		16	22	Ω
		V _{CC} = 4.5V, V _{IN} = 0V, I _{IN} = 64mA		5	7	
		V _{CC} = 4.5V, V _{IN} = 0V, I _{IN} = 30mA		5	7	
		V _{CC} = 4.5V, V _{IN} = 2.4V, I _{IN} = 15mA		10	15	

■ SWITCHING CHARACTERISTICS (T_A =25°C)

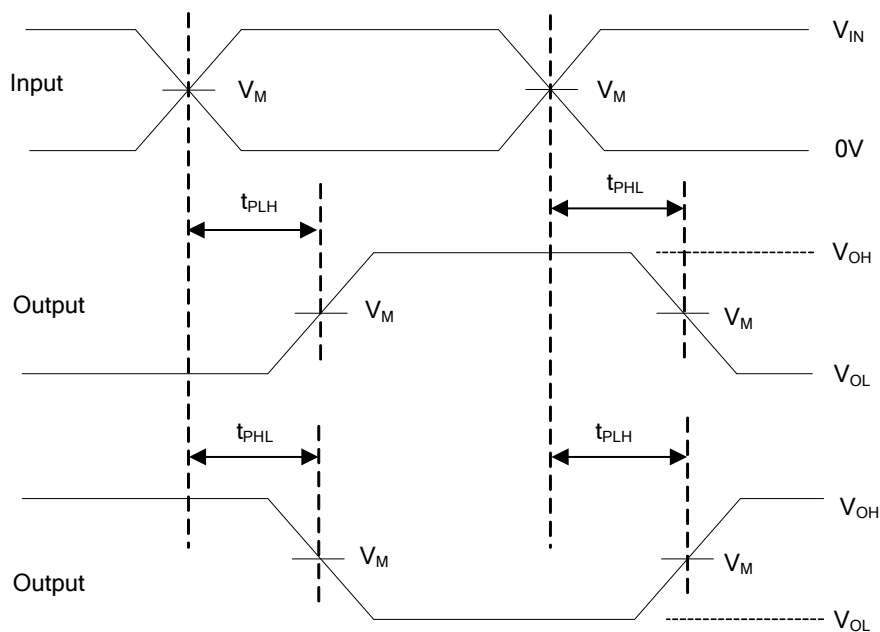
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Propagation delay from input A (or B) to output B (or A)	t _{PLH} /t _{PHL} (t _{pd})	V _{CC} =4V, C _L =50pF, R _L =500Ω		0.35	ns
		V _{CC} =5±0.5V, C _L =50pF, R _L =500Ω		0.25	
Propagation delay from input OE to output A or B	t _{PZL} /t _{PZH} (t _{en})	V _{CC} =4V, C _L =50pF, R _L =500Ω		5.4	ns
		V _{CC} =5±0.5V, C _L =50pF, R _L =500Ω	1.6	5.1	
Propagation delay from input OE to output A or B	t _{PLZ} /t _{PHZ} (t _{dis})	V _{CC} =4V, C _L =50pF, R _L =500Ω		5	ns
		V _{CC} =5±0.5V, C _L =50pF, R _L =500Ω	1	4.5	

■ TEST CIRCUIT AND WAVEFORMS



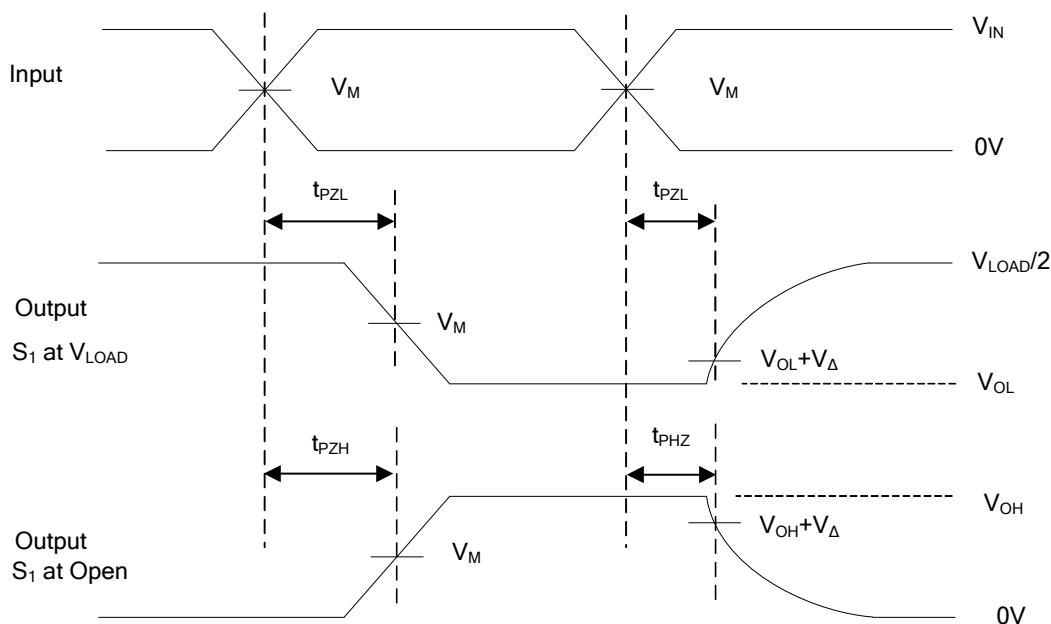
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	Open

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_{IN}	t_r, t_f					
4V	V_{CC}	$\leq 2.5ns$	1.5V	7V	50pF	500 Ω	0.3V
5V \pm 0.5V	V_{CC}	$\leq 2.5ns$	1.5V	7V	50pF	500 Ω	0.3V



Voltage waveforms Propagation delay times

■ TEST CIRCUIT AND WAVEFORMS(Cont.)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- Notes: 1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR \leq 10MHz, $Z_O = 50\Omega$.

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