

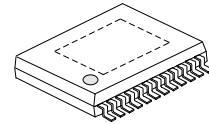
**PA3202**

CMOS IC

**2-W STEREO AUDIO POWER
AMPLIFIER WITH MUTE****■ DESCRIPTION**

The UTC **PA3202** is a monolithic integrated circuit that stereo bridged audio power amplifiers capable of producing 2 W into 3Ω with a 5V supply voltage or 800mW into 3Ω with a 3.3V supply voltage. The UTC **PA3202** simplifies design and frees up board space for other features. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in UTC **PA3202**, that reduce clicks and pops noise during power up or shutdown mode operation.

A MUX control terminal (HP/LINE) allows selection between the two sets of stereo input signals. To simplify the audio system design, UTC **PA3202** combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal.



HTSSOP-24

■ FEATURES

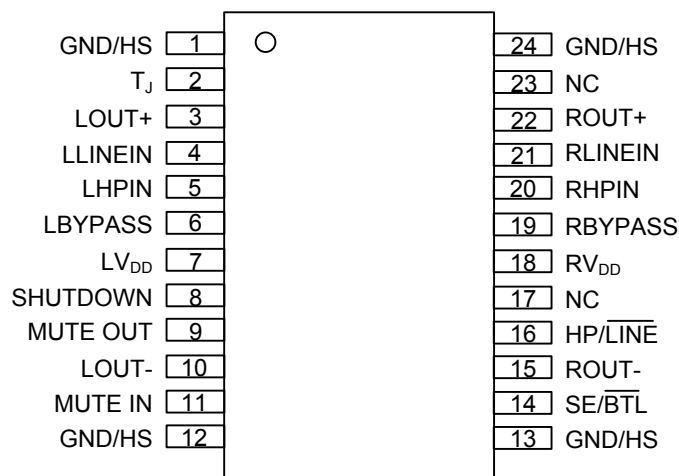
- * Improves depop circuitry to eliminate turn-on and turn-off transients in output
- * Output power:
 - 2W(typ.)@5V into 3Ω with 0.2% THD+N max (1kHz)
 - 800mW(typ.)@3.3V into 3Ω with 0.2% THD+N max (1kHz)
- * Fully specified for use with 3-Ω Loads
- * Stereo switchable bridged/single-ended power amplifiers
- * Input MUX select terminal
- * Thermal-shutdown protection
- * Shutdown mode available

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA3202L-N24-R	PA3202G-N24-R	HTSSOP-24	Tape Reel
PA3202L-N24-T	PA3202G-N24-T	HTSSOP-24	Tube

	(1)Packing Type	(1) R: Tape Reel, T: Tube
	(2)Package Type	(2) N24: HTSSOP-24
	(3)Lead Plating	(3) G:Halogen Free, L: Lead Free

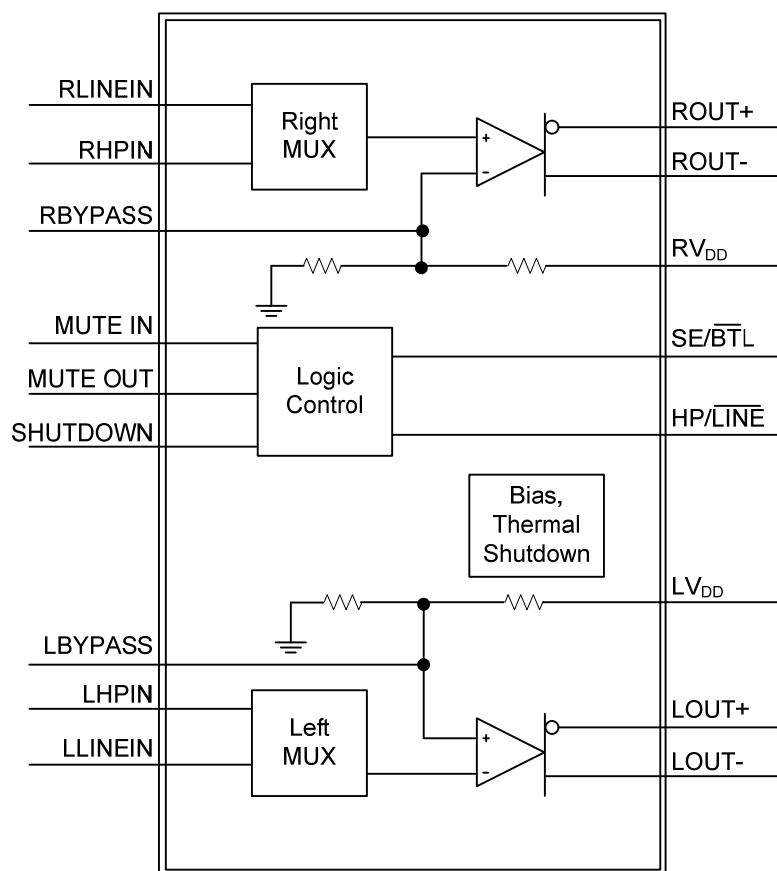
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO	PIN NAME	I/O	DESCRIPTION
1, 12, 13, 24	GND/HS		Power ground; directly connected to thermal pad.
6	LBYPASS		Tap to left channel internal mid-supply voltage divider bias
17, 23	NC		No connection
19	RBYPASS		Tap to right channel internal mid-supply voltage divider bias
4	LLINE IN	I	Left channel line input; selected when HP/LINE is held low
5	LHP IN	I	Left channel headphone input; selected when HP/LINE is held high
7	LVDD	I	Left channel power supply and for primary bias circuits
8	SHUTDOWN	I	Places entire IC in shutdown mode when held high, $I_{DD} = 5\mu A$
9	MUTE OUT	I	Follows MUTE IN, provides buffered output
11	MUTE IN	I	Mute all amplifiers input; high active to mute amplify, low active to normal operation
14	SE/BTL	I	SE & BTL mode selection; active high for SE mode, active low for BTL mode
16	HP/LINE	I	MUX control input, active high to select headphone input, active low to select line input
18	RVDD	I	Right channel power supply
20	RHPIN	I	Right channel headphone input, selected when HP/LINE is held high
21	RLINEIN	I	Right channel line input, selected when HP/LINE is held low
2	TJ	O	Sources current proportional to the junction temperature. Left floating for normal operation.
3	LOUT+	O	Left channel + output in BTL & SE mode
10	LOUT-	O	Left channel – output in BTL mode & high-impedance in SE mode
22	ROUT+	O	Right channel + output in BTL & SE mode
15	ROUT-	O	Right channel – output in BTL mode & high impedance in SE mode

■ BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATINGS** (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD} \sim +0.3$	V
Continuous Total Power Dissipation	P_D	Internally limited	
Junction Temperature	T_J	+150	°C
Operating Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL		MIN	NOM	MAX	UNIT
Supply Voltage	V_{DD}		3	5	5.5	V
Operating Temperature	T_{OPR}	$V_{DD} = 5\text{ V}$, 250 mW/ch average power, 4-Ω stereo BTL drive, with proper PCB design	-40		85	°C
		$V_{DD} = 5\text{ V}$, 2 W/ch average power, 3-Ω stereo BTL drive, with proper PCB design	-40		85	
Common Mode Input Voltage	V_{ICM}	$V_{DD}=5\text{V}$	1.25		4.5	V
		$V_{DD}=3.3\text{V}$	1.25		2.7	

■ **DC ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Supply Current	I_{DD}	$V_{DD}=5\text{V}$	Stereo BTL	19	30	mA
			Stereo SE	9	18	
			Mono BTL	9	18	
			Mono SE	3	10	
		$V_{DD}=3.3\text{V}$	Stereo BTL	13	20	mA
			Stereo SE	5	10	
			Mono BTL	5	10	
			Mono SE	3	6	
Output Offset Voltage (Measured Differentially)	$V_{O(OFF)}$	$V_{DD} = 5\text{ V}$, Gain = 2, See Note 1		5	25	mV
Supply Current in Mute Mode	$I_{DD(MUTE)}$	$V_{DD}=5\text{V}$		1		mA
I_{DD} in Shutdown	$I_{DD(SD)}$	$V_{DD}=5\text{V}$		5	19	μA

Note 1. At $3\text{ V} < V_{DD} < 5\text{ V}$ the dc output voltage is approximately $V_{DD}/2$.

■ AC OPERATING CHARACTERISTICS

$V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 3\Omega$

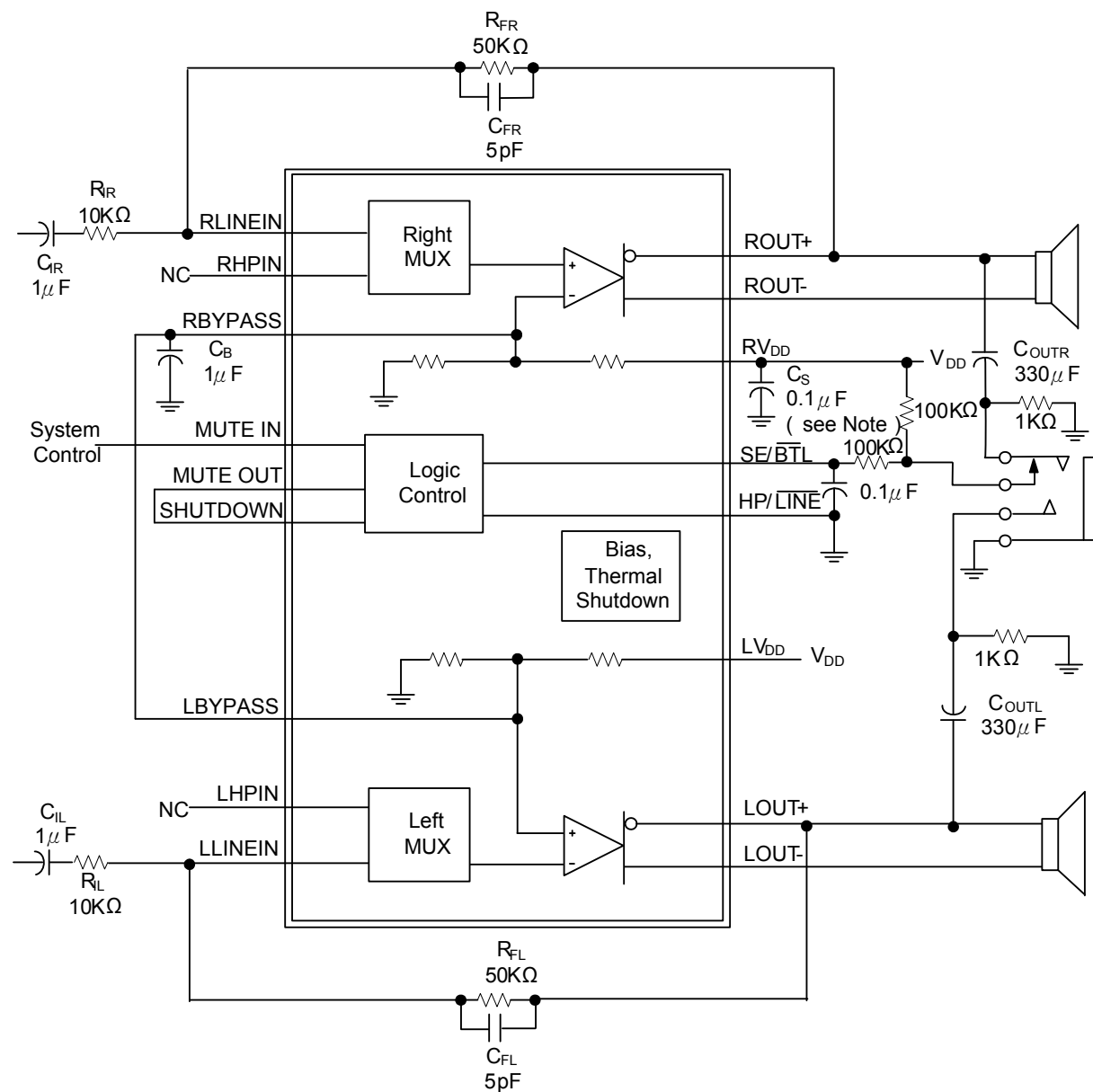
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power (Each Channel) See Note 2	P_{OUT}	THD =0.2% BTL		2		W
		THD =1% BTL		2.2		
Total Harmonic Distortion Plus Noise	TDH+N	$P_{OUT} = 2\text{ W}$, $f = 20 \sim 20\text{ kHz}$		200		m%
		$V_{IN} = 1\text{ V}$, $R_L = 10\text{ K}\Omega$, $A_V = 1\text{ V/V}$		100		m%
Maximum Output Power Bandwidth	B_W	$A_V = 10\text{ V/V}$, THD < 1 %,		>20		KHz
Phase Margin		$R_L = 4\Omega$, Open Loop,		85°		
Supply Ripple Rejection Ratio	RR	$f = 1\text{ kHz}$		80		dB
		$f = 20 \sim 20\text{ kHz}$,		60		
Mute Attenuation				85		dB
Channel-to-Channel Output Separation		$f = 1\text{ kHz}$		85		dB
Line/HP Input Separation				100		dB
BTL Attenuation in SE Mode				100		dB
Input Impedance	Z_{IN}			2		M Ω
Signal-to-Noise Ratio		$P_{OUT} = 500\text{ mW}$, BTL		95		dB
Output Noise Voltage	eN			21		$\mu\text{V}_{(RMS)}$

$V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 3\Omega$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power (Each Channel) See Note 2	P_{OUT}	THD =0.2% BTL		800		mW
		THD =1% BTL		900		
Total Harmonic Distortion Plus Noise	TDH+N	$P_{OUT} = 800\text{ mW}$, $f = 20 \sim 20\text{ kHz}$		350		m%
		$V_{IN} = 1\text{ V}$, $R_L = 10\text{ K}\Omega$, $A_V = 1\text{ V/V}$		200		m%
Maximum Output Power Bandwidth	B_W	$A_V = 10\text{ V/V}$, THD < 1 %,		>20		KHz
Phase Margin		$R_L = 4\Omega$, Open Loop		85°		
Supply Ripple Rejection Ratio	RR	$f = 1\text{ kHz}$		70		dB
		$f = 20 \sim 20\text{ kHz}$,		55		
Mute Attenuation				85		dB
Channel-to-Channel Output Separation		$f = 1\text{ kHz}$		85		dB
Line/HP Input Separation				100		dB
BTL Attenuation in SE Mode				100		dB
Input Impedance	Z_{IN}			2		M Ω
Signal-to-Noise Ratio		$P_{OUT} = 500\text{ mW}$, BTL		95		dB
Output Noise Voltage	eN			21		$\mu\text{V}_{(RMS)}$

Note 2. Output power is measured at the output terminals of the IC at 1 kHz.

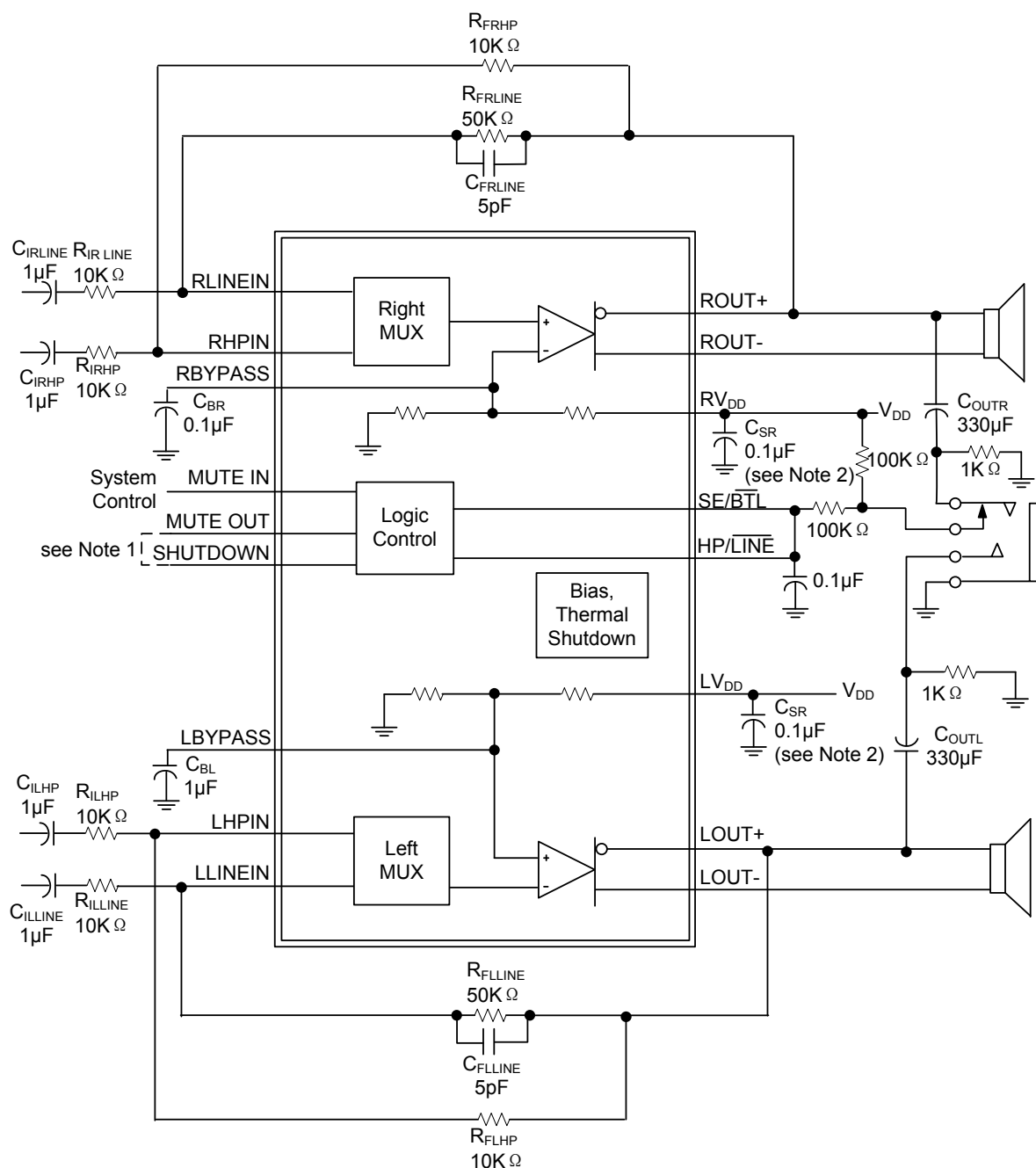
■ TYPICAL APPLICATION CIRCUIT



Note: 0.1 μ F ceramic capacitor should be placed as close as possible to the IC. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 10 μ F or greater should be placed near the audio power amplifier.

PA3202 Minimum Configuration Application Circuit

■ TYPICAL APPLICATION CIRCUIT

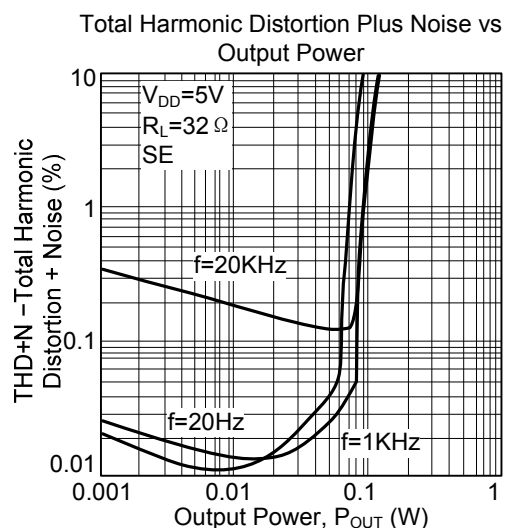
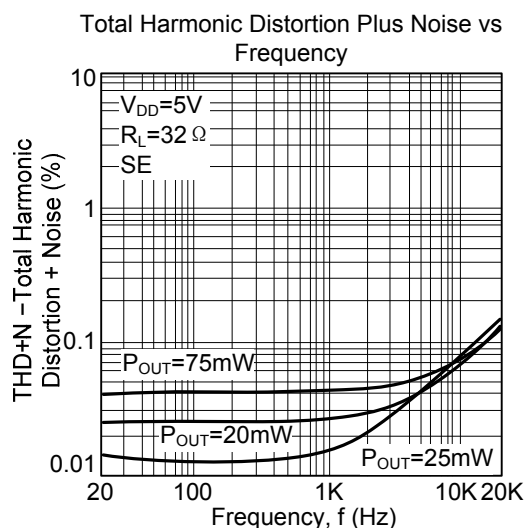
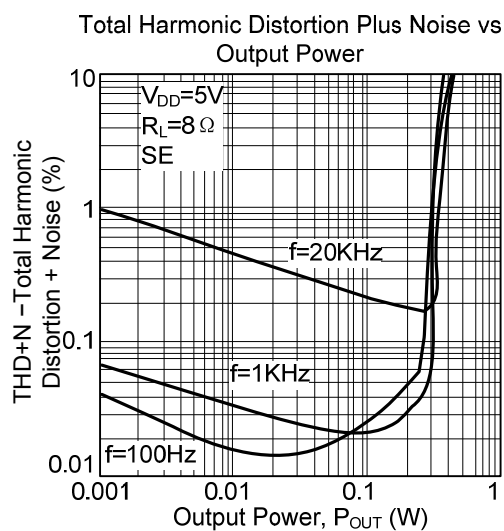
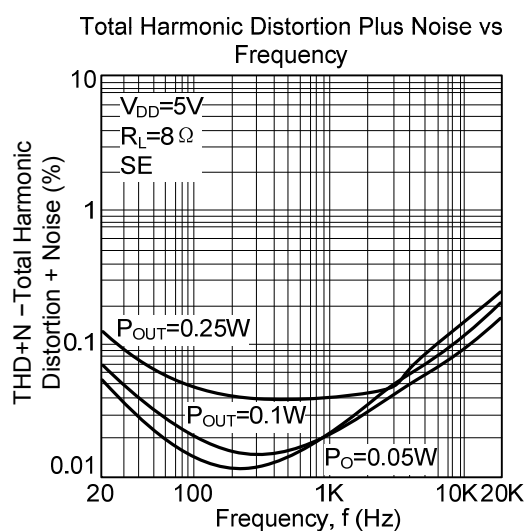
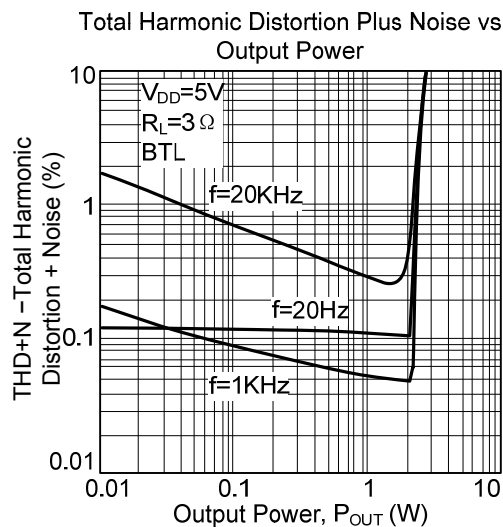
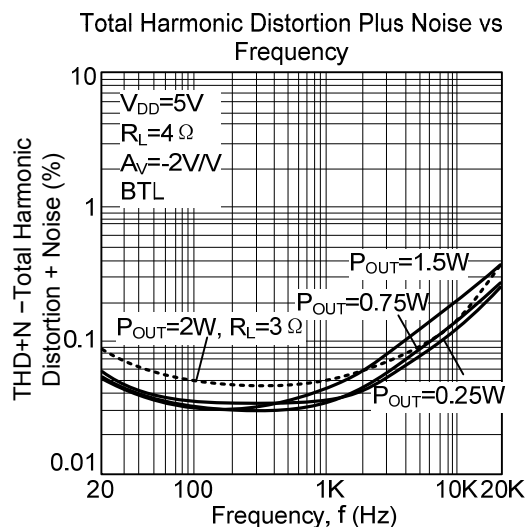


Note:1. This connection is for ultra-low current in shutdown mode.

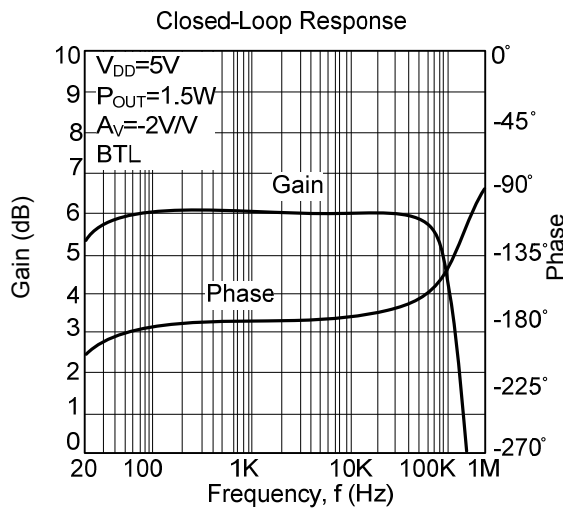
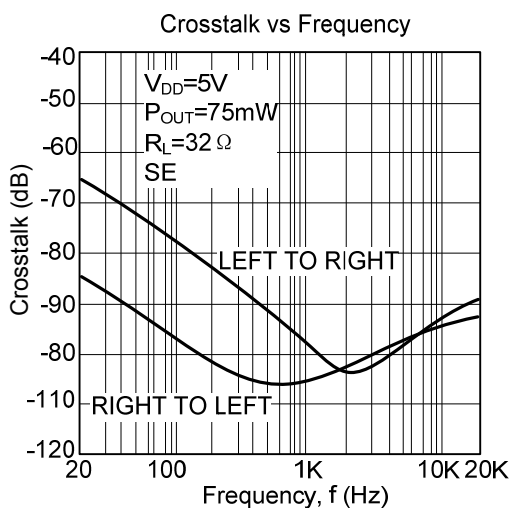
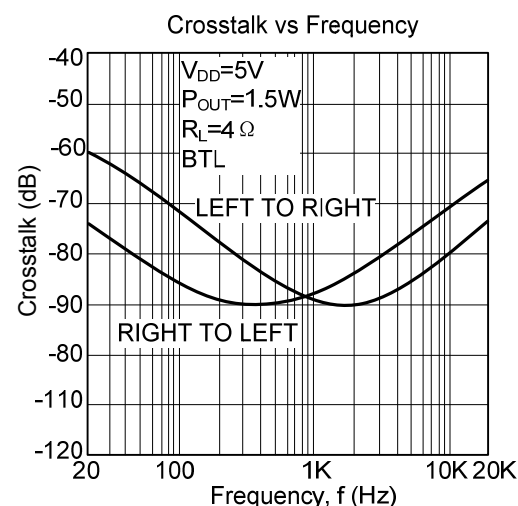
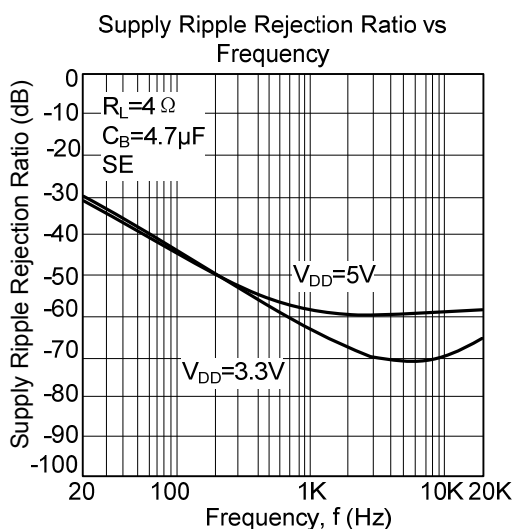
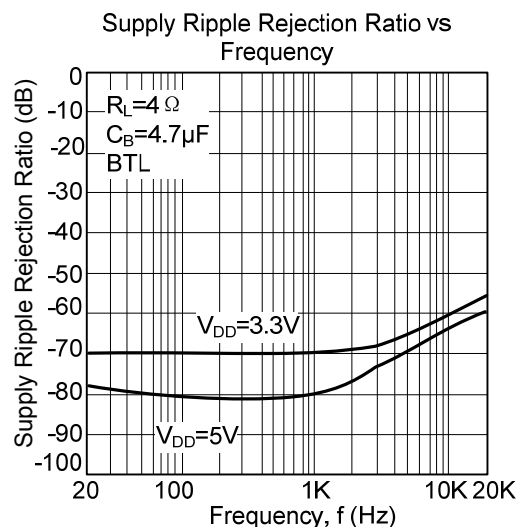
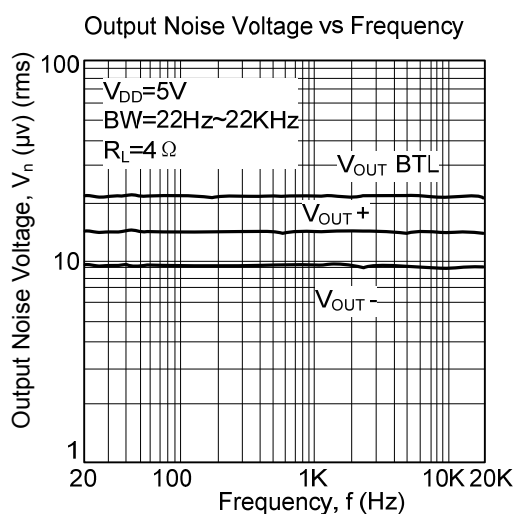
2. A 0.1 μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater should be placed near the audio power amplifier.

PA3202 Full Configuration Application Circuit

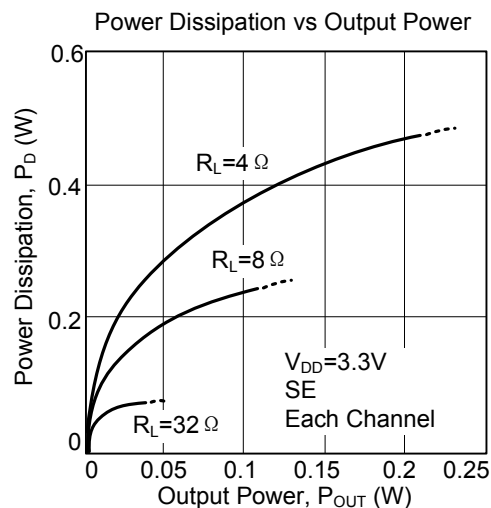
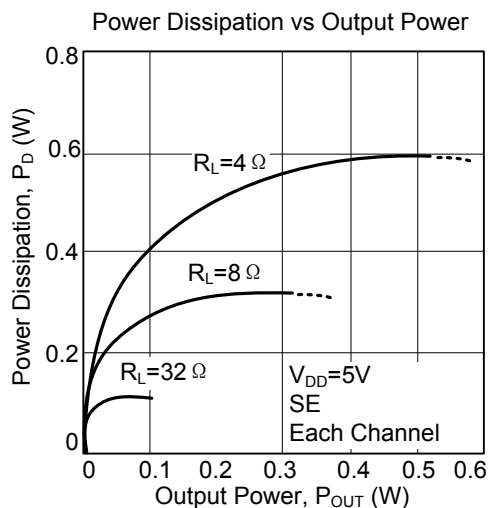
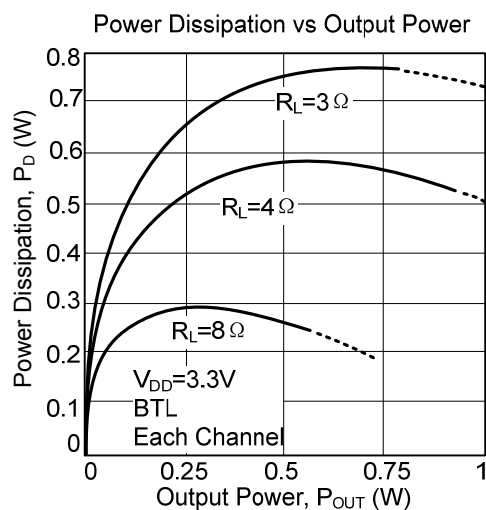
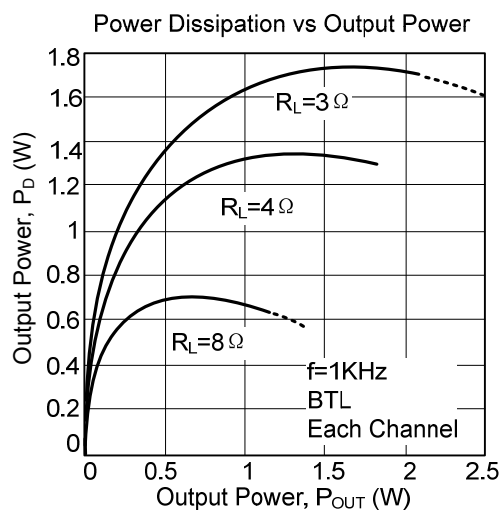
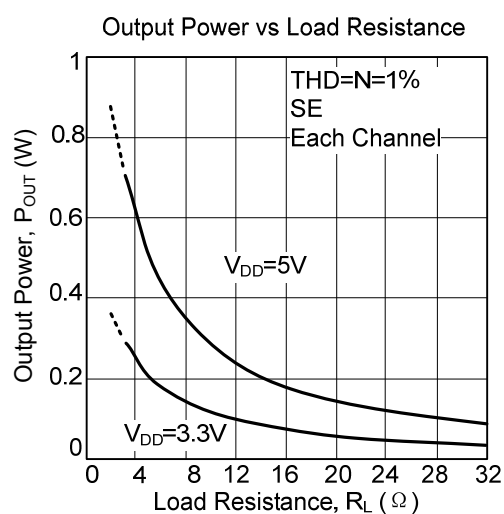
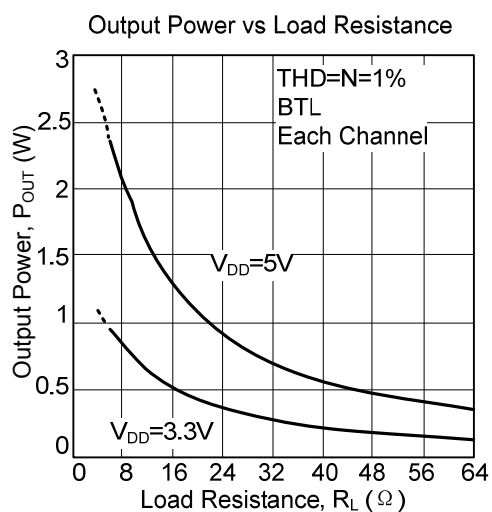
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(Cont.)



TYPICAL CHARACTERISTICS(Cont.)



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