

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

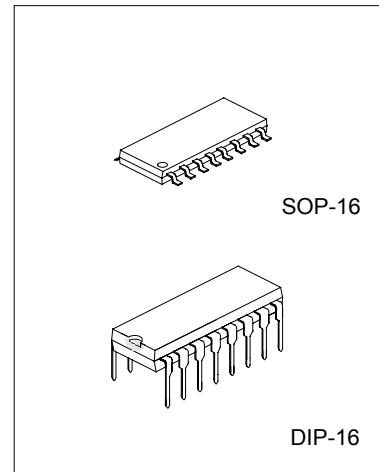
DESCRIPTION

The UTC MC14511 BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

FEATURES

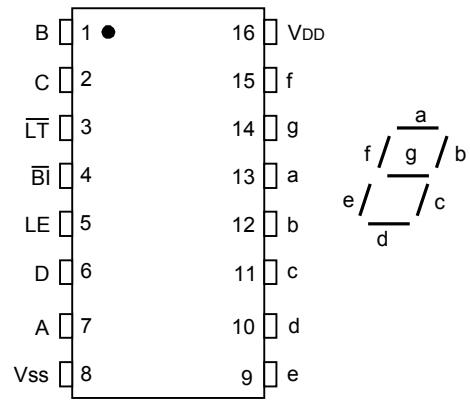
- * Low Logic Circuit Power Dissipation
- * High-Current Sourcing Outputs (Up to 25 mA)
- * Latch Storage of Code
- * Blanking Input
- * Lamp Test Provision
- * Readout Blanking on all Illegal Input Combinations
- * Lamp Intensity Modulation Capability
- * Time Share (Multiplexing) Facility
- * Supply Voltage Range = 3.0 V ~ 18 V
- * Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- * Chip Complexity: 216 FETs or 54 Equivalent Gates
- * Triple Diode Protection on all Inputs



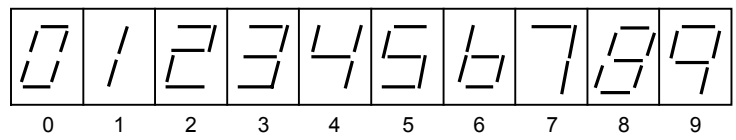
UTC MC14511

CMOS IC

PIN CONFIGURATION



DISPLAY



TRUTH TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X	*							*

X=Don't Care

*Depends upon the BCD code previously applied when LE=0

UTC

UNISONIC TECHNOLOGIES CO., LTD.

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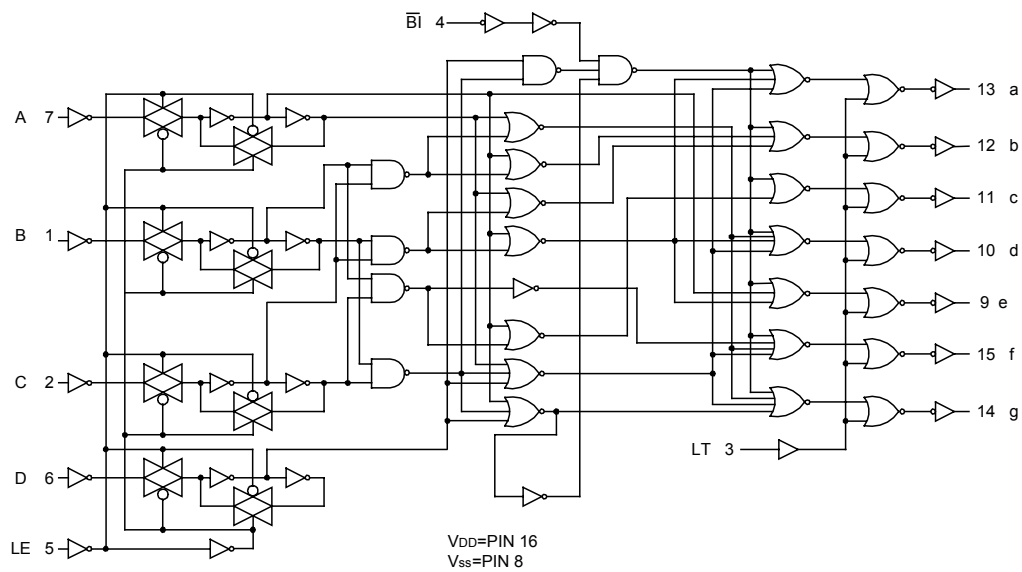
This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range:

$$V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$$

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to Vss) (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage Range	V _{DD}	-0.5 ~ +18.0	V
Input Voltage Range, All Inputs	V _{in}	-0.5 ~ V _{DD} +0.5	V
DC Current Drain per Input Pin	I	10	mA
Power Dissipation, per Package (Note 2)	P _D	500	mW
Maximum Output Drive Current (Source) per Output	I _{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output (Note 3)	P _{OHmax}	50	mW
Operating Temperature Range	T _a	-55 ~ +125	°C
Storage Temperature Range	T _{stg}	-65 ~ +150	°C

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C ~ 125°C

Note 3: P_{OHmax} = I_{OH} (V_{DD} - V_{OH})

ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vss)

PARAMETER	SYMBOL	V _{DD} V _{dC}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	V _{OL}	5.0	"0" Level		0	0.05	V
		10	V _{in} =V _{DD} or 0		0	0.05	
		15			0	0.05	
	V _{OH}	5.0	"1" Level	4.1	4.57		V
		10	V _{in} =0 or V _{DD}	9.1	9.58		
		15		14.1	14.59		
Input Voltage #	V _{IL}	5.0	"0" Level		2.25	1.5	V
		10	V _o =3.8 or 0.5 V		4.50	3.0	
		15	V _o =8.8 or 1.0 V		6.75	4.0	
	V _{IH}	5.0	"1" Level		2.75		V
		10	V _o =0.5 or 3.8 V	3.5	7.0		
		15	V _o =1.0 or 8.8 V	11	5.50		
Output Drive Voltage	V _{OH}	5.0	I _{OH} =0mA Source	4.1	4.57		V
			I _{OH} =5.0mA		4.24		
			I _{OH} =10mA	3.9	4.12		
			I _{OH} =15mA		3.94		
			I _{OH} =20mA	3.4	3.70		
	V _{OH}	10	I _{OH} =25mA		3.54		V
			I _{OH} =0mA Source	9.1	9.58		
			I _{OH} =5.0mA		9.26		
			I _{OH} =10mA	9.0	9.17		
			I _{OH} =15mA		9.04		
			I _{OH} =20mA	8.6	8.90		
			I _{OH} =25mA		8.70		

PARAMETER	SYMBOL	V _{DD} V _{dc}	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Drive Voltage	V _{OH}	15	I _{OH} =0mA Source	14.1	14.59		V
			I _{OH} =5.0mA		14.27		
			I _{OH} =10mA	14	14.18		
			I _{OH} =15mA		14.07		
			I _{OH} =20mA	13.6	13.95		
			I _{OH} =25mA		13.70		
Output Drive Current	I _{OL}	5.0	V _{OL} =0.4V Sink	0.51	0.88		mA
		10	V _{OL} =0.5V	1.3	2.25		
		15	V _{OL} =1.5V	3.4	8.8		
Input Current	I _{in}	15			±0.00001	±0.1	μA
Input Capacitance	C _{in}				5.0	7.5	pF
Quiescent Current	I _{DD}	5.0	(Per Package) V _{in} =0 or		0.005	5.0	μA
		10	V _{DD} ,		0.010	10	
		15	I _{out} =0 μA		0.015	20	
Total Supply Current (Notes 5 & 6)	I _T	5.0	(Dynamic plus Quiescent,	I _T =(1.9 μA/kHz) f+I _{DD} I _T =(3.8 μA/kHz) f+I _{DD} I _T =(5.7 μA/kHz) f+I _{DD}			μA
		10	Per Package)				
		15	(C _L =50pF on all outputs, all buffers switching)				

Note 4: Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 V min @ V_{DD} = 5.0 V

2.0 V min @ V_{DD} = 10 V

2.5 V min @ V_{DD} = 15 V

Note 5: The formulas given are for the typical characteristics only at 25°C.

Note 6: To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

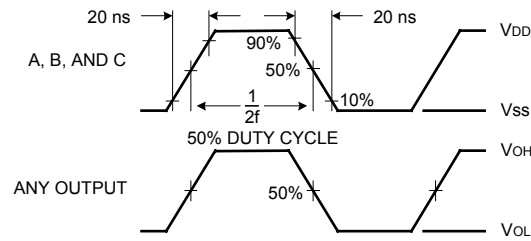
Where: I_T is in μA (per package), C_L in pF, V_{DD} in V_{dc}, and f in kHz is input frequency.

SWITCHING CHARACTERISTICS (Note 7) (CL=50pF, Ta=25°C)

PARAMETER	SYMBOL	VDD Vdc	TEST CONDITIONS	Min	TYP	MAX	UNIT
Output Rise Time	t _{TLH}	5.0 10 15	t _{TLH} =(0.40 ns/pF) CL+20 ns t _{TLH} =(0.25 ns/pF) CL+17.5 ns t _{TLH} =(0.20 ns/pF) CL+15 ns		40 30 25	80 60 50	ns
Output Fall Time	t _{THL}	5.0 10 15	t _{THL} =(1.5 ns/pF) CL+50 ns t _{THL} =(0.75 ns/pF) CL+37.5 ns t _{THL} =(0.55 ns/pF) CL+37.5 ns		125 75 65	250 150 130	ns
Data Propagation Delay Time	t _{PLH}	5.0 10 15	t _{PLH} =(0.40 ns/pF) CL+620 ns t _{PLH} =(0.25 ns/pF) CL+237.5 ns t _{PLH} =(0.20 ns/pF) CL+165 ns		640 250 175	1280 500 350	ns
	t _{PHL}	5.0 10 15	t _{PHL} =(1.3 ns/pF) CL+655 ns t _{PHL} =(0.60 ns/pF) CL+260 ns t _{PHL} =(0.35 ns/pF) CL+182.5 ns		720 290 200	1440 580 400	
Blank Propagation Delay Time	t _{PLH}	5.0 10 15	t _{PLH} =(0.30 ns/pF) CL+585 ns t _{PLH} =(0.25 ns/pF) CL+187.5 ns t _{PLH} =(0.15 ns/pF) CL+142.5 ns		600 200 150	750 300 220	ns
	t _{PHL}	5.0 10 15	t _{PHL} =(0.85 ns/pF) CL+442.5 ns t _{PHL} =(0.45 ns/pF) CL+177.5 ns t _{PHL} =(0.35 ns/pF) CL+142.5 ns		485 200 160	970 400 320	
Lamp Test Propagation Delay Time	t _{PLH}	5.0 10 15	t _{PLH} =(0.45 ns/pF) CL+290.5 ns t _{PLH} =(0.25 ns/pF) CL+112.5 ns t _{PLH} =(0.20 ns/pF) CL+80 ns		313 125 90	625 250 180	ns
	t _{PHL}	5.0 10 15	t _{PHL} =(1.3 ns/pF) CL+248 ns t _{PHL} =(0.45 ns/pF) CL+102.5 ns t _{PHL} =(0.35 ns/pF) CL+72.5 ns		313 125 90	625 250 180	
Setup Time	t _{su}	5.0 10 15		100 40 30			ns
Hold Time	t _h	5.0 10 15		60 40 30			ns
Latch Enable Pulse Width	t _{WL}	5.0 10 15		520 220 130	260 110 65		ns

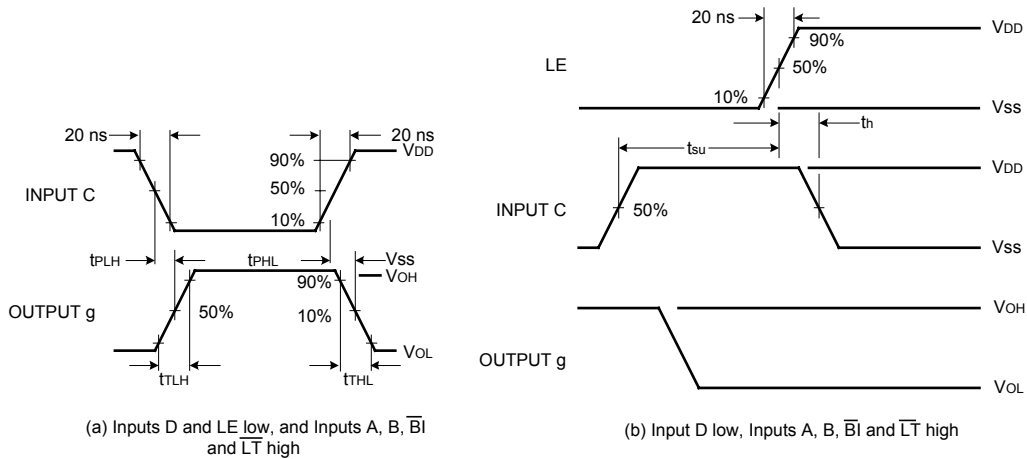
Note 7: The formulas given are for the typical characteristics only.

SWITCHING TIME WAVEFORMS



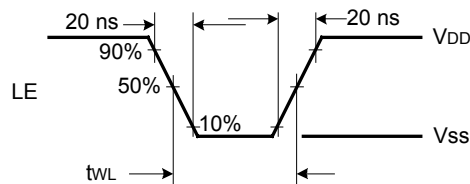
Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective CL loads.

Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high

(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high

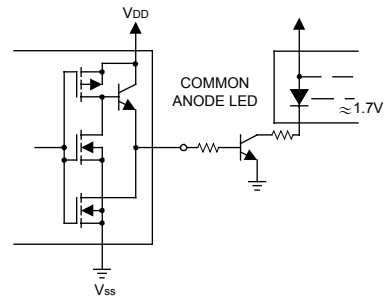
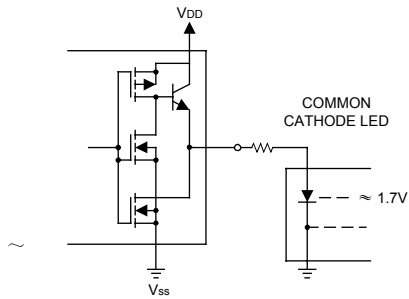


(c) Data DCBA strobed into latches.

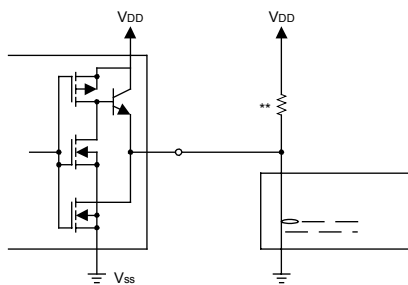
Figure 2. Dynamic Signal Waveforms

CONNECTIONS TO VARIOUS DISPLAY READOUTS

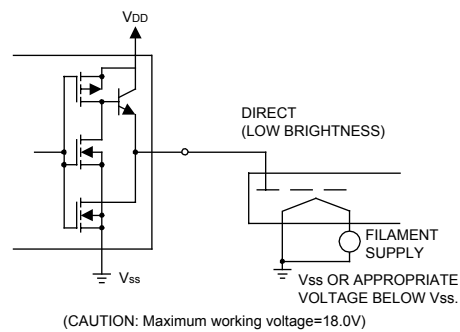
LIGHT EMITTING DIODE (LED) READOUT



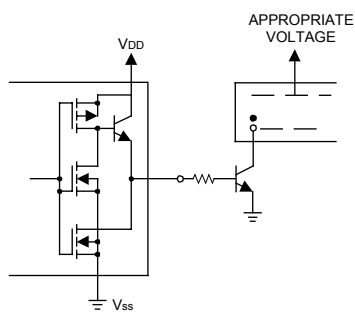
INCANDESCENT READOUT



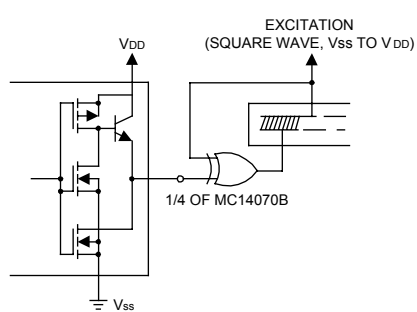
FLUORESCENT READOUT



GAS DISCHARGE READOUT



LIQUID CRYSTAL(LCD) READOUT



** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LCD's not recommended for life of LCD readouts.

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