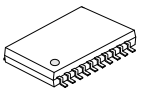
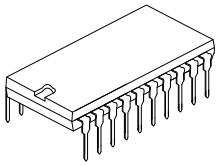
75323 *LINEAR INTEGRATED CIRCUIT*

MULTIPLE RS-232 DRIVERS AND RECEIVERS



SOP-20



DIP-20

■ DESCRIPTION

The UTC **75323** provides a rugged, low-cost effectiveness performance due to the circuits consisting of bipolar ones, incorporating five drivers and three receivers. It is characterized with less required external components, board spaces and an easy interface between UART and serial-port connector for a single chip. Working at temperatures from 0℃ to 70℃ is one of its features.

■ FEATURES

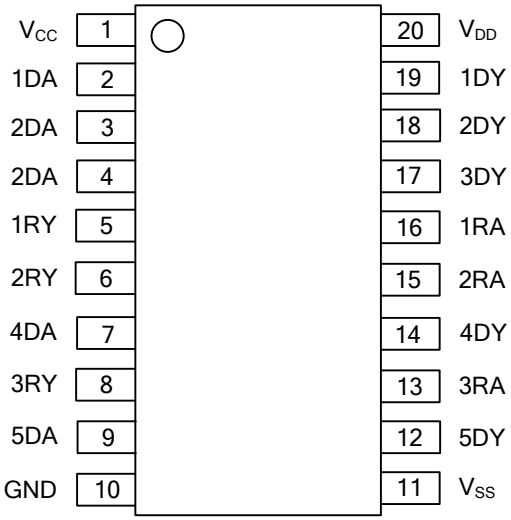
* Single chip with easy interface between UART and serial-port connector
* Data rates : 20 kb/s.
* Complement to the UTC **75232**.

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
75323L-S20-R	75323G-S20-R	SOP-20	Tape Reel
75323L-S20-T	75323G-S20-T	SOP-20	Tube
75323L-D20-T	75323G-D20-T	DIP-20	Tube

75323L-S20-R (1) Packing Type (2) Package Type (3) Lead Free	(1) R: Tape Reel, T: Tube (2) S20: SOP-8, D20: DIP-20 (3) G: Halogen Free, L: Lead Free

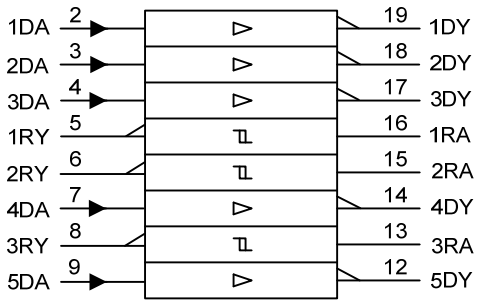
■ PIN CONFIGURATION



■ PIN DESCRIPTION

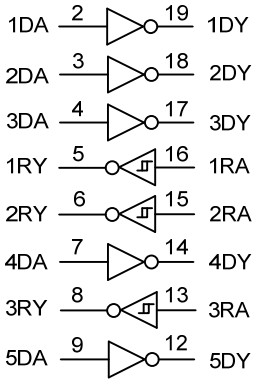
PIN NO.	PIN NAME	DESCRIPTION
1	V_{CC}	Supply Voltage of receiver
2	1DA	Input of driver 1
3	2DA	Input of driver 2
4	3DA	Input of driver 3
5	1RY	Output of receiver 1
6	2RY	Output of receiver 2
7	4DA	Input of driver 4
8	3RY	Output of receiver 3
9	5DA	Input of driver 5
10	GND	Ground
11	V_{SS}	Negative Supply Voltage of driver
12	5DY	Output of driver 5
13	3RA	Input of receiver 3
14	4DY	Output of driver 4
15	2RA	Input of receiver 2
16	1RA	Input of receiver 1
17	3DY	Output of driver 3
18	2DY	Output of driver 2
19	1DY	Output of driver 1
20	V_{DD}	Positive Supply Voltage of driver

■ LOGIC SYMBOL



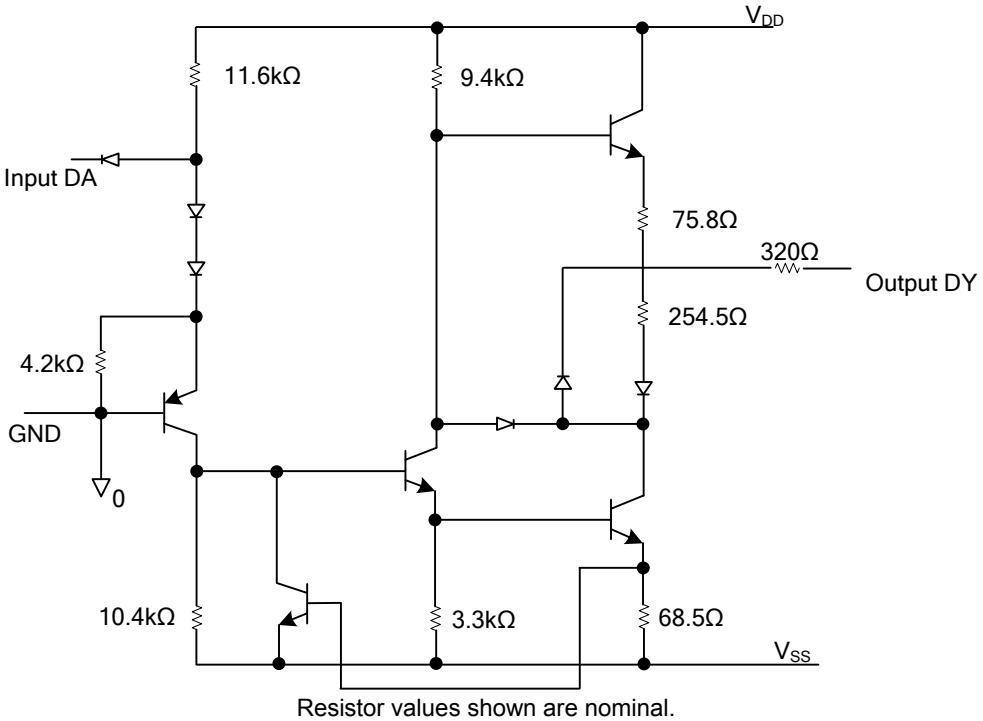
Note: This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

■ LOGIC DIAGRAM (POSITIVE LOGIC)



■ BLOCK DIAGRAM

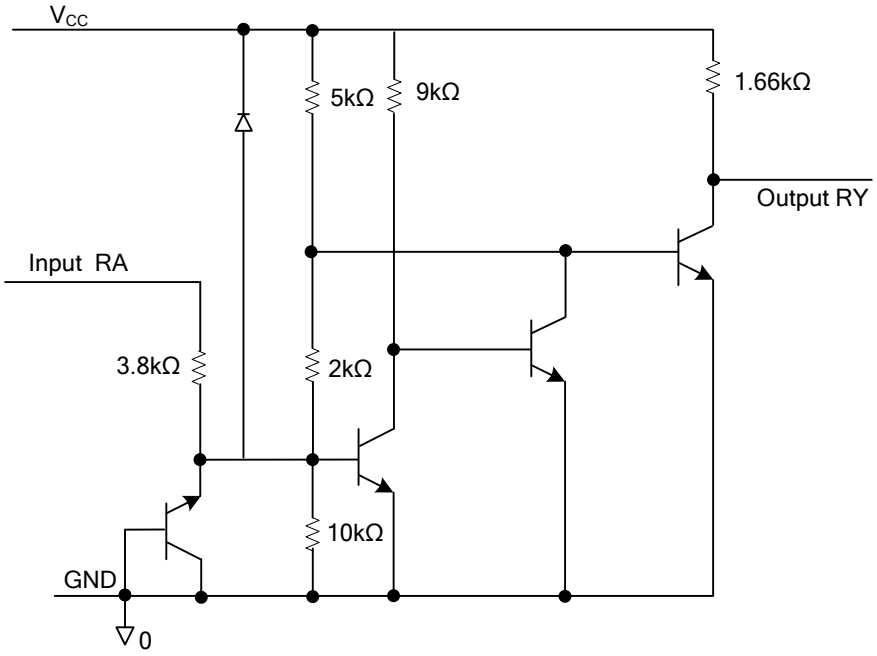
The circuit for each driver



Resistor values shown are nominal.

■ BLOCK DIAGRAM(Cont.)

The circuit for each receiver



Resistor values shown are nominal

■ ABSOLUTE MAXIMUM RATING (T_A=25℃, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage (Note 2)		V_{CC}	10	V
Supply Voltage (Note 2)		V_{DD}	15	V
Supply Voltage (Note 2)		V_{SS}	-15	V
Input Voltage	Driver	V_I	-15 ~ 7	V
	Receiver		-30 ~ 30	
Output Voltage (Driver)		Vo	-15 ~ 15	V
Low-level Output Current (Receiver)		I_{OL}	20	mA
Storage temperature		T_{STG}	-65 ~ 150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. All voltages are with respect to the network ground terminal.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-20	θ_{JA}	97	°C/W
	DIP-20		67	

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}	7.5	9	13.5	V
		V_{SS}	-7.5	-9	-13.5	
		V_{CC}	4.5	5	5.5	
High-Level Input Voltage	Driver	V_{IH}	1.9			V
Low-Level Input Voltage	Driver	V_{IL}			0.8	V
High-Level Output Current	Driver	I_{OH}			-6	mA
	Receiver				-0.5	
High-Level Output Current	Driver	I_{OL}			6	mA
	Receiver				16	
Operating Free-Air Temperature		T_A	0		70	℃

■ SUPPLY CURRENTS OVER OPERATING FREE-AIR TEMPERATURE RANGE

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Supply Current From V_{DD}	I_{DD}	All inputs at 1.9V, No load	V_{DD}=9V, V_{SS}=-9V		25	mA
			V_{DD}=12V, V_{SS}=-12V		32	
		All inputs at 0.8V, No load	V_{DD}=9V, V_{SS}=-9V		7.5	mA
			V_{DD}=12V, V_{SS}=-12V		9.5	
Supply Current From V_{SS}	I_{SS}	All inputs at 1.9V, No load	V_{DD}=9V, V_{SS}=-9V		-25	mA
			V_{DD}=12V, V_{SS}=-12V		-32	
		All inputs at 0.8V, No load	V_{DD}=9V, V_{SS}=-9V		-5.3	mA
			V_{DD}=12V, V_{SS}=-12V		-5.3	
Supply Current From V_{CC}	I_{CC}	V_{CC}=5V, All inputs at 5V, No load			20	mA

■ ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE (V_{DD}=9V, V_{SS}=-9V, V_{CC}=5V , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{IL}=0.8V, R_L=3kΩ (Fig. 1)	6	7.5		V
Low-Level Output Voltage(see Note 1)	V_{OL}	V_{IH}=1.9V, R_L=3kΩ (Fig. 1)		-7.5	-6	V
High-Level Input Current	I_{IH}	V_I=5V (Fig. 2)			10	μA
Low-Level Input Current	I_{IL}	V_I=0 (Fig. 2)			-1.6	mA
High-Level Short-Circuit Output Current	$I_{OS(H)}$	V_{IL}=0.8V,Vo=0 (Fig. 1, Note 2)	-4.5	-9	-19.5	mA
Low-Level Short-Circuit Output Current	$I_{OS(L)}$	V_{IH}=2V, Vo=0 (Fig. 1)	4.5	9	19	mA
Output Resistance (Note 3)	r_O	V_{CC}=V_{DD}=V_{SS}=0, Vo=-2V ~ 2V	300			Ω

Note: 1. The algebraic convention, where the more positive(less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e. g.,if-10V is maximum, the typical value is a more negative voltage.
2. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
3. Test conditions are those specified by TIA/EIA-232-F and as listed above.

■ SWITCHING CHARACTERISTICS (T_A=25℃, V_{DD}=12V, V_{SS}=-12V, V_{CC}=5V±10%)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time, Low- to High-Level Output	t_{PLH}	R_L=3kΩ ~ 7kΩ, C_L=15pF (Fig. 3)		315	500	ns
Propagation Delay Time, High-to Low-Level Output	t_{PHL}			75	175	
t_{TLH} Transition Time, Low-to High-Level Output	t_{TLH}	R_L=3kΩ~7kΩ, C_L=15pF(Fig. 3)		60	100	ns
		R_L=3kΩ ~ 7kΩ, C_L=2500pF (Fig. 3, Note 1)		1.7	2.5	μs
Transition Time, High-to Low-Level Output	t_{THL}	R_L=3kΩ~7kΩ, C_L=15pF(Fig. 3)		40	75	ns
		R_L=3kΩ ~ 7kΩ, C_L=2500pF (Fig. 3, Note 2)		1.5	2.5	μs

Note: 1. Measured between-3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.
2. Measured between 3-V and -3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low

■ ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V_{IT}+	Fig.5	T_A=25℃	1.75	1.9	2.3	V
			T_A=0℃ ~ 70℃	1.55		2.3	
Negative-Going Input Threshold Voltage	V_{IT}-	Fig. 5		0.75	0.97	1.25	
Input Hysteresis Voltage(V_{IT}+ - V_{IT}-)	V_{HYS}			0.5			
High-Level Output Voltage	V_{OH}	I_{OH}=-0.5mA	V_{IH}=0.75V	2.6	4	5	V
			Inputs open	2.6			
Low-Level Output Voltage	V_{OL}	I_{OL}=10mA, V_I=3V			0.2	0.45	V
High-Level Input Current	I_{IH}	V_I=25V		3.6		8.3	mA
		V_I=3V		0.43			mA
Low-Level Input Current	I_{IL}	V_I=-25V		-3.6		-8.3	mA
		V_I=-3V		-0.43			mA
Short-Circuit Output Current	I_{OS}	Fig. 4			-3.4	-12	mA

Note: All typical values are at T_A=25℃, V_{CC}=5V, V_{DD}=9V, V_{SS}=-9V

■ SWITCHING CHARACTERISTICS (T_A=25℃, V_{CC}=5V, V_{DD}=12V, V_{SS}= -12V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time, Low-to High-Level Output	t_{PLH}	C_L=50pF, R_L=5kΩ Fig. 6		107	500	ns
Propagation Delay Time, High- to Low-Level Output	t_{PHL}			42	150	ns
Transition Time, Low-to High-Level Output	t_{TLH}			175	525	ns
Transition time, High- to Low-Level Output	t_{THL}			16	60	ns

■ PARAMETER MEASUREMENT INFORMATION

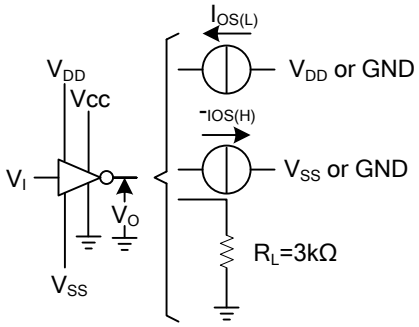


Fig. 1 Driver Test Circuit for V_{OH}, V_{OL}, I_{OS}(H), I_{OS}(L)

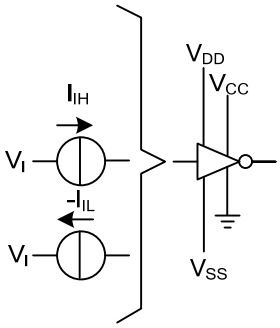


Fig. 2 Driver Test Circuit for I_{IH} and I_{IL}

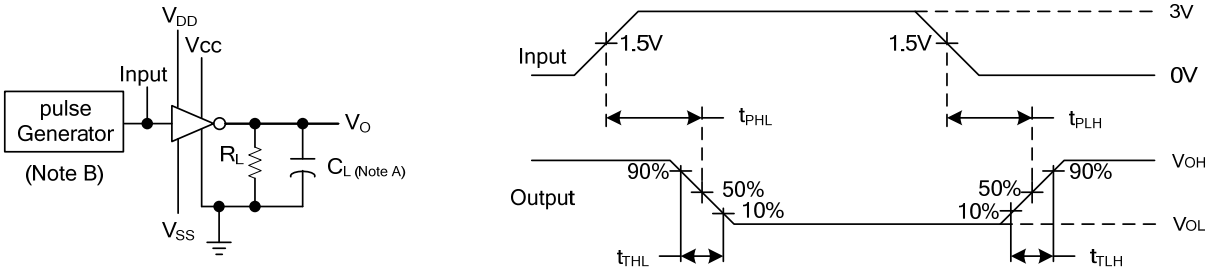


Fig.3 Driver Test Circuit and Voltage Waveforms

Notes: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics(t_W=25μs,P_{RR}=20kHz,Z_O=50Ω,t_R=t_F<50ns)

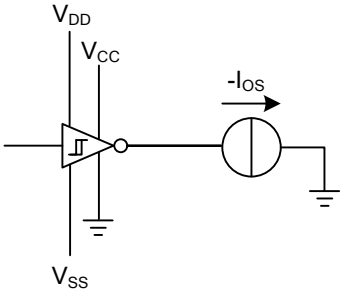


Fig.4 Receiver Test Circuit for Ios

■ PARAMETER MEASUREMENT INFORMATION(Cont.)

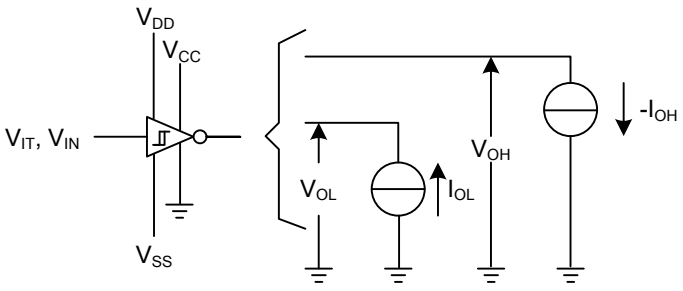


Fig. 5 Receiver Test Circuit for V_{IT} ,V_{OH}, and V_{OL}

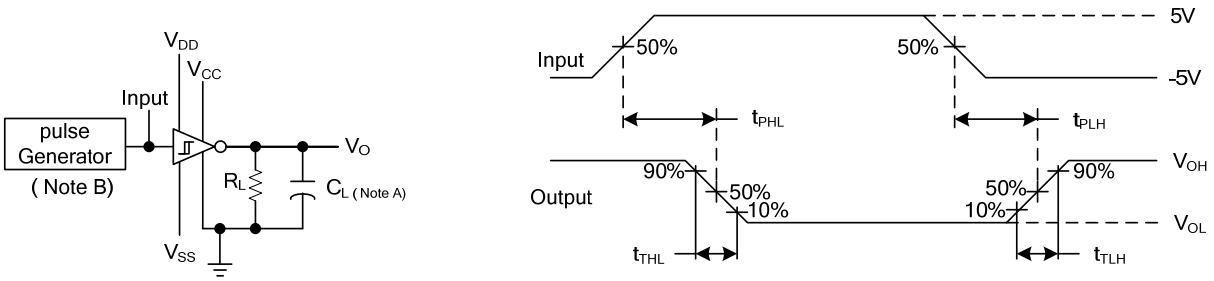


Fig. 6 Receive Propagation and Transition Times

Notes: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics(t_W=25μs,P_{RR}=20kHz,Z_O=50Ω,t_R=t_F<50ns)

■ APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the UTC **75323** in the fault condition in which the device output are shorted to V_{DD} or V_{SS}, and the Power supplies are at low and provide low-impedance paths to ground (see Figure7)

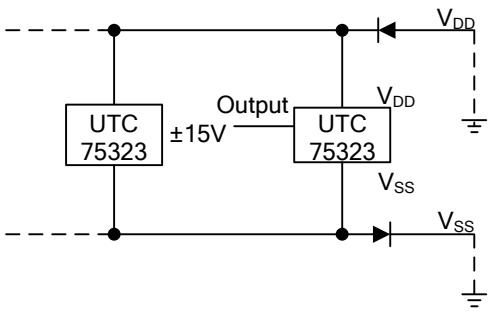


Fig. 7 Power-Supply Protection to Meet Power-Off Fault Condition of TIA/EIA-232-F

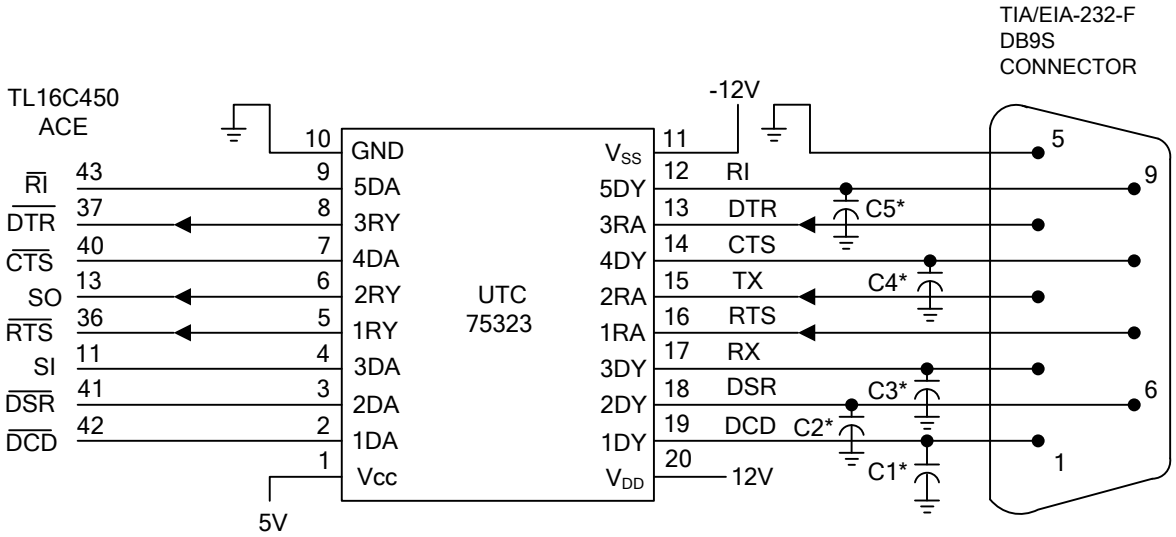


Fig. 8 Typical Connection

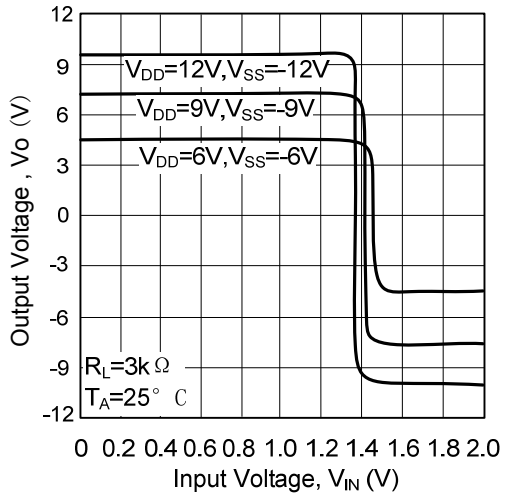
*See Figure Slew Rate vs. Load Capacitance to select the correct values for the loading capacitors (C1, C2, C3, C4 and C5), which may be required to meet the RS-232 maximum slew-rate requirement of 30V/us. The value of the loading capacitors resrequired depends upon the line length and desired slew rate, but is typically 330pF.

Note C: To use the receivers only, V_{DD} and Vss both must be powered or tied to ground.

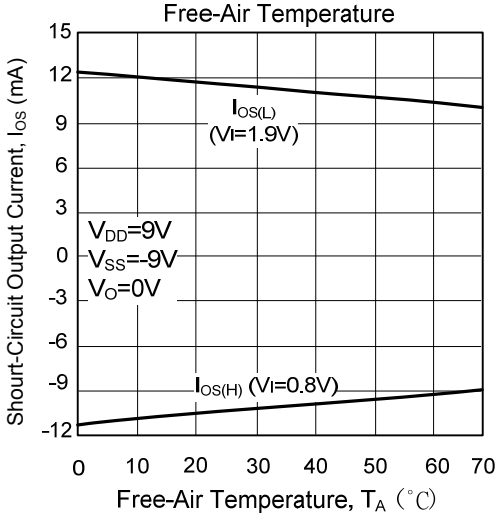
■ TYPICAL CHARACTERISTICS

DRIVER SECTION

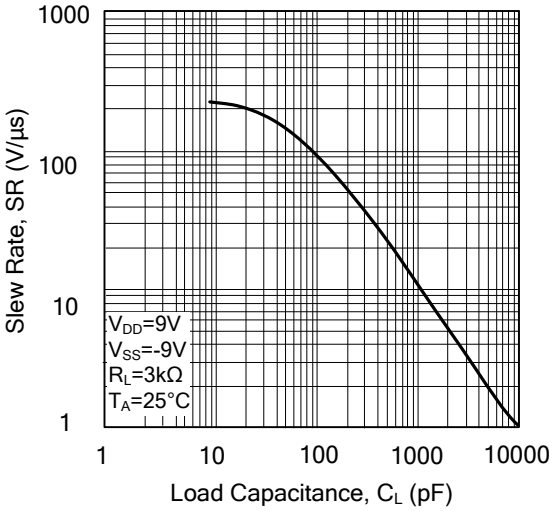
Voltage-Transfer Characteristic



Short-Circuit Output Current vs. Free-Air Temperature



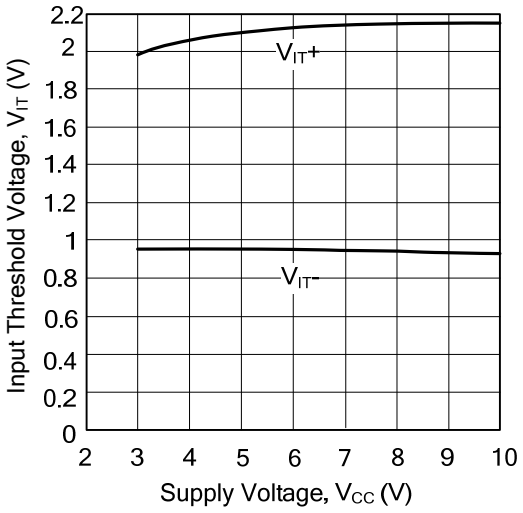
Slew Rate vs. Load Capacitance



■ TYPICAL CHARACTERISTICS(Cont.)

RECEIVER SECTION

Input Threshold Voltage vs. Supply Voltage



Input Threshold Voltage vs. Free-Air Temperature