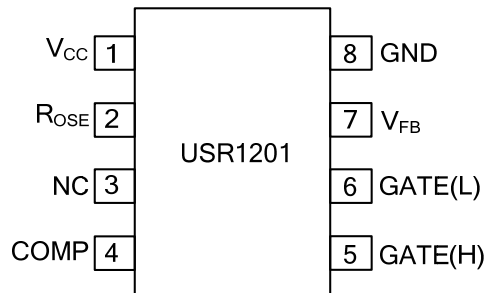


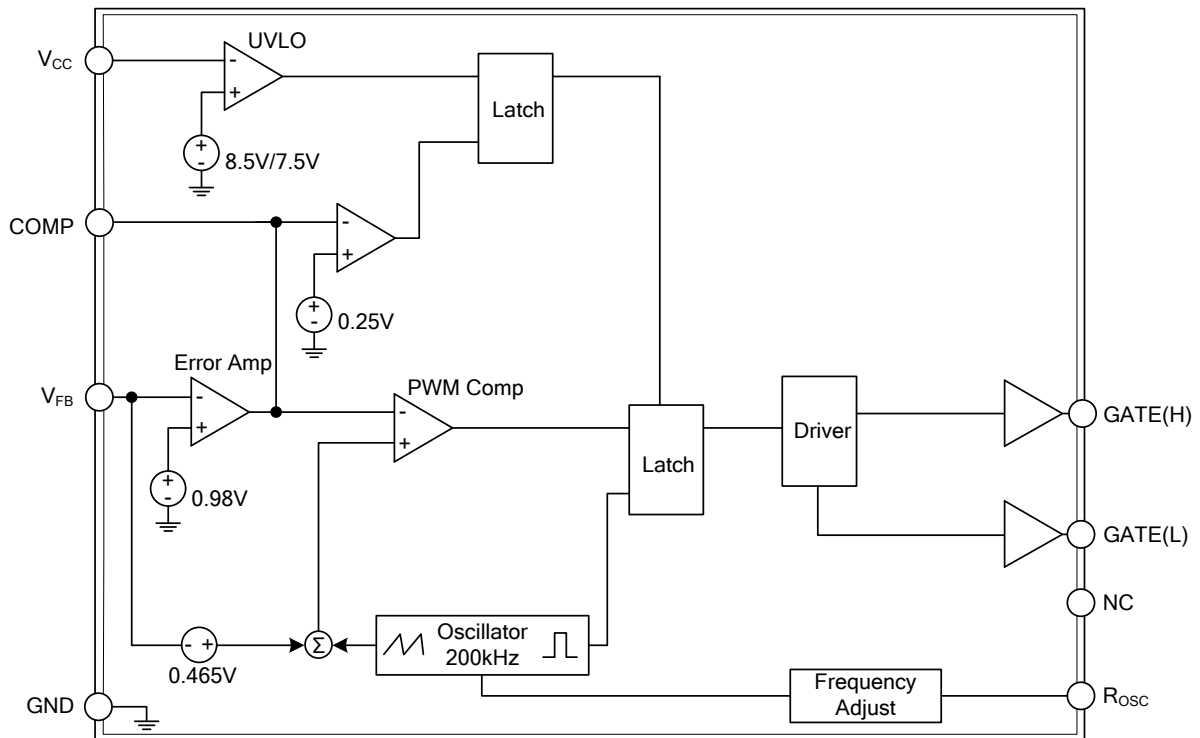
■ **PIN CONFIGURATION**



■ **PIN DESCRIPTION**

PIN NO.	PIN NAME	DESCRIPTION
1	V _{CC}	Power supply input.
2	R _{OSC}	Frequency adjust pin.
3	NC	No connect.
4	COMP	Error amp output.
5	GATE(H)	High-side switch FET driver pin.
6	GATE(L)	Low-side synchronous FET driver pin.
7	V _{FB}	Feedback voltage
8	GND	Ground

■ **BLOCK DIAGRAM**



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65~150	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	165	°C/W
Junction to Case	θ_{JC}	48	°C/W

■ MAXIMUM RATING

PARAMETER	SYMBOL	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{CC}	20V	-0.5V	N/A	1.5A Peak, 450mA DC
Compensation Capacitor	COMP	6.0V	-0.5V	10mA	10mA
Voltage Feedback Input	V_{FB}	6.0V	-0.5V	1.0mA	1.0mA
Frequency Adjust	R_{OSC}	6.0V	-0.5V	1.0mA	1.0mA
High-Side FET Driver	GATE(H)	20V	-0.5V, -2.0V for 50ns	1.5A Peak, 200mA DC	1.5A Peak, 200mA DC
Low-Side FET Driver	GATE(L)	20V	-0.5V, -2.0V for 50ns	1.5A Peak, 200mA DC	1.5A Peak, 200mA DC
Ground	GND	0.5V	-0.5V	1.5A Peak, 450mA DC	N/A

■ ELECTRICAL CHARACTERISTICS

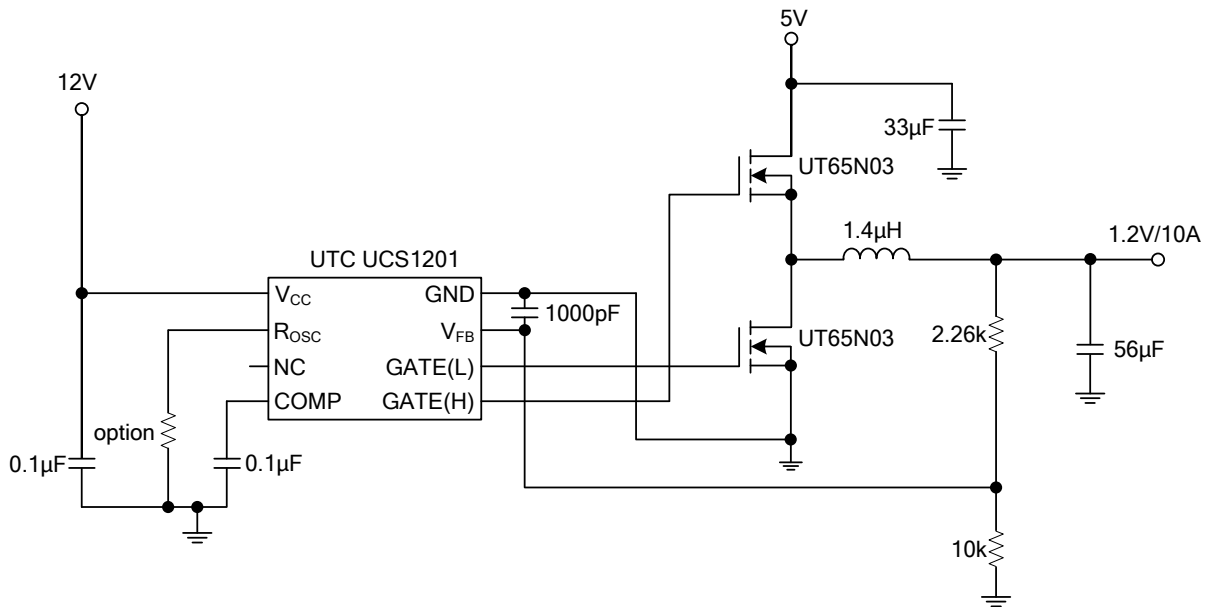
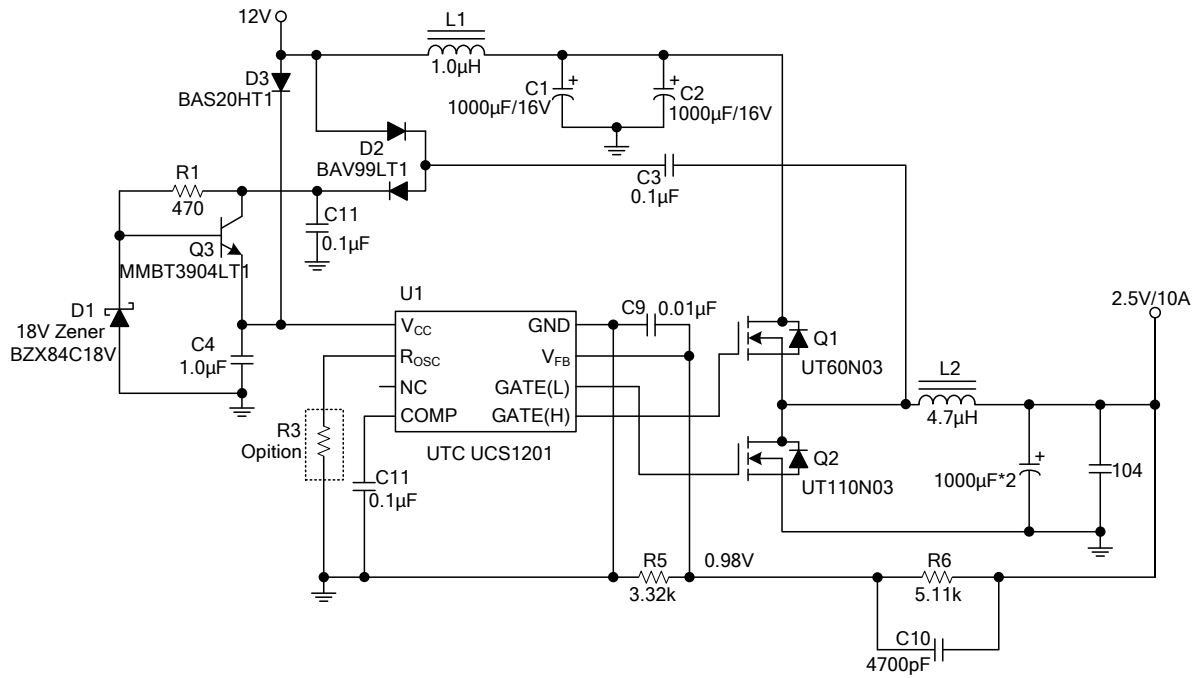
(0°C<T_J<125°C, 9.0V<V_{CC}<20V, C_{GATE(H)}=C_{GATE(L)}=3.3nF, C_{COMP}=0.1μF, R_{OSC}=74kΩ, unless otherwise specified.)
(Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Error Amplifier						
V _{FB} Bias Current	I _{FB}	V _{FB} =0V		0.4	2.0	μA
COMP Source Current	I _{SOURCE}	COMP=1.5V, V _{FB} =0.8V	15	30	60	μA
COMP Sink Current	I _{SINK}	COMP=1.5V, V _{FB} =1.2V	15	30	60	μA
Reference Voltage	V _{REF}	COMP=V _{FB}	0.970	0.980	0.990	V
		T _J <25°C	0.965	0.980	0.995	V
COMP Max Voltage	V _{COMP-MAX}	V _{FB} =0.8V	2.4	3.1		V
COMP Min Voltage	V _{COMP-MIN}	V _{FB} =1.2V		0.1	0.2	V
COMP Fault Discharge Current at UVLO	I _{CHARGE}	COMP=1.2V, V _{CC} =6.9V	0.5	1.2		mA
COMP Fault Discharge Threshold to Reset UVLO	V _{RESET}		0.1	0.25	0.3	V
GATE(H) and GATE(L)						
Rise Time	t _R	1.0V<GATE(L), GATE(H)<V _{CC} -2.0V, V _{CC} =12V		40	80	ns
Fall Time	t _F	V _{CC} -2.0V<GATE(L), GATE(H)<1.0V, V _{CC} =12V		40	80	ns
GATE(H) to GATE(L) Delay	t _{DH}	GATE(H)<2.0V, GATE(L)>2.0V	40	60	105	ns
GATE(L) to GATE(H) Delay	t _{DL}	GATE(L)<2.0V, GATE(H)>2.0V	40	60	105	ns
Minimum Pulse Width	t _{PULSE}	GATE(X)=4.0V		250		ns
High Voltage (AC)	V _H	Measure GATE(L) or GATE(H) 0.5nF<C _{GATE(H)} =C _{GATE(L)} <10nF, (Note 2)	V _{CC} -0.5	V _{CC}		V
Low Voltage (AC)	V _L	Measure GATE(L) or GATE(H) 0.5nF<C _{GATE(H)} =C _{GATE(L)} <10nF, (Note 2)		0	0.5	V
PWM Comparator						
PWM Comparator Offset	V _{PWM-MIN}	V _{FB} =0V, Increase COMP Until GATE(H) Starts Switching	0.415	0.465	0.525	V
Ramp Max Duty Cycle				80		%
Artificial Ramp		Duty Cycle=50%, R _{OSC} =74kΩ	50	63	75	mV
Transient Response		COMP=1.5V, V _{FB} 20mV Overdrive. (Note 2)		200	300	ns
V _{FB} Input Range		(Note 3)	0		1.4	V
Oscillator						
Switching Frequency	F _{OSC}	R _{OSC} Not Used	170	200	230	kHz
	F _{OSC}	R _{OSC} =74kΩ	240	280	320	kHz
General Electrical Specifications						
V _{CC} Supply Current	I _Q	COMP=0V (No Switching)		9.0	12	mA
Start Threshold		GATE(H) Switching, COMP Charging	8.0	8.5	9.0	V
Stop Threshold		GATE(H) Not Switching, COMP Discharging	7.0	7.5	8.0	V
Hysteresis	V _{HYS}	Start-Stop	0.75	1.0	1.25	V

Notes: 1. Characteristics at temperature extremes are guaranteed via correlation using quality statistical control methods.

2. Guaranteed by design. Not tested in production.

■ TYPICAL APPLICATION CIRCUIT



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