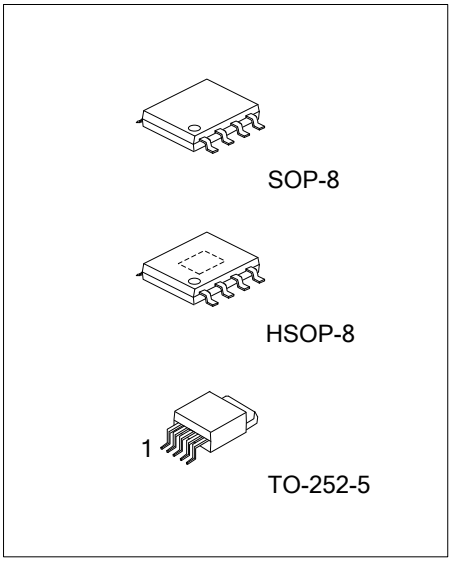
UR5512

LINEAR INTEGRATED CIRCUIT

2A DDR BUS TERMINATION REGULATOR



Lead-free: UR5512L
Halogen-free: UR5512G

■ DESCRIPTION

The UTC **UR5512** is a linear regulator which provides up to 2 Amp bi-directional driving and sinking capability for DDR SDRAM bus terminator application. The output termination voltage tracks the reference voltage applied at V_{REF} pin. A resistor divider connected to V_{IN}, GND and V_{REF} pins is used to force a reference voltage to V_{REF} pin.

The UTC **UR5512** contains a high-speed operational amplifier to provide excellent response to line/load transient. An active-low shutdown (V_{REF}) pin provides Suspend to RAM (STR) functionality. Additional features include current limiting protection, on-chip thermal shut-down protection.

■ FEATURES

* DDR-I and DDR-II termination voltage applications
* Driving and sinking current up to 2A
* Low output voltage offset (within 20mV@±2A)
* Adjustable output voltage by external resistors
* Suspend to RAM (STR) functionality
* Current limiting protection
* Thermal protection
* Cost-effective and easy to use

■ ORDERING INFORMATION

Ordering Number			Package	Packing
Normal	Lead Free Plating	Halogen Free		
UR5512-S08-R	UR5512L-S08-R	UR5512G-S08-R	SOP-8	Tape Reel
UR5512-SH2-R	UR5512L-SH2-R	UR5512G-SH2-R	HSOP-8	Tape Reel
UR5512-TN5-R	UR5512L-TN5-R	UR5512G-TN5-R	TO-252-5	Tape Reel

UR5512L-S08-R (1)Packing Type (2)Package Type (3)Lead Plating	(1) R: Tape Reel (2) S08: SOP-8, SH2: HSOP-8, TN5: TO-252-5 (3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

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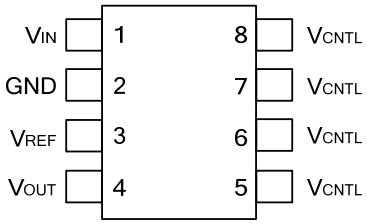
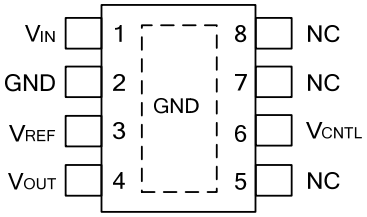
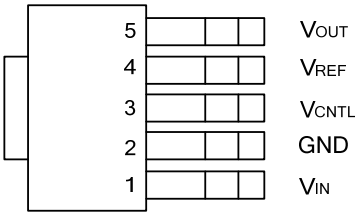
■ PIN CONFIGURATIONS



SOP-8



HSOP-8



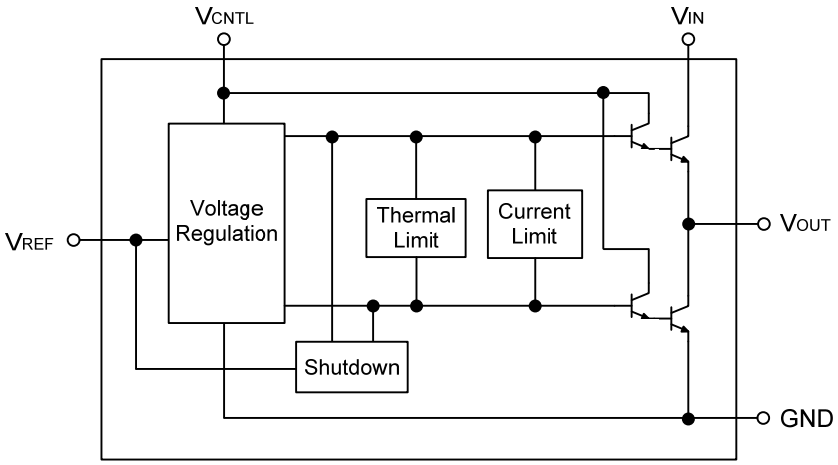
TO-252-5

NC: No Connection

■ PIN DESCRIPTION

PIN NAME	PIN TYPE	PIN DESCRIPTION
V_{IN}	I	Power input pin
GND	O	Ground pin
V_{CNTL}	I	Power input pin for internal control circuit
V_{REF}	I	Reference voltage input and active-low shutdown control pin
V_{OUT}	O	Output voltage pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
V_{CNTL} Control Voltage	V_{CNTL}	-0.2 ~ 7	V
V_{IN} Supply Voltage	V_{IN}	-0.2 ~ 6	V
Power Dissipation	P_D	Internally Limited	W
Junction Temperature	T_J	+125	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RANGE	UNIT
V_{CNTL} Control Voltage (Note 1)	V_{CNTL}	3.1 ~ 6	V
V_{IN} Supply Voltage	V_{IN}	1.6 ~ 5.5	V
V_{REF} Input Voltage	V_{REF}	0.85 ~ 1.75	V
V_{OUT} Output Voltage (Note 2)	V_{OUT}	V_{REF} ± 0.02	V
V_{OUT} Output Current	I_{OUT}	-2 ~ +2	A
Junction Temperature	T_J	0 ~ +125	°C

Notes: 1. Please always keep V_{CNTL}-V_{OUT}> 1.9V for good regulation.
2. The V_{OUT} tracks the V_{REF} with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS

(V_{IN} = 1.8V, V_{CNTL} = 5V, V_{REFEN} = 0.5V_{IN}), Ta = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
Operation Current of V_{CNTL}	I_{CNTL}	I_{OUT} = 0A		2	4	mA
		V_{REF}=GND (Shutdown)		1.9		mA
Current into V_{REF} Pin	I_{REF}	V_{REF} =1.25V		200	500	nA
		V_{REF} = GND (Shutdown)		20	40	μA
Standby Current	I_{STB}	V_{REF} < 0.2V, R_{LOAD} = 180Ω		50	90	μA
OUTPUT VOLTAGE						
Output Voltage Offset (V_{OUT} - V_{REF})	$V_{O(OFF)}$	I_{OUT} = 0A	-20	6	+20	mV
Load Regulation	ΔV_{LOAD}	I_{OUT} = ±1.5A	-20		+20	mV
PROTECTION						
Current limit	I_{LIMIT}		2.0			A
Thermal Shutdown Temperature	T_{SD}	V_{CNTL} = 5V	125	180		°C
Thermal Shutdown Hysteresis	ΔT_{SD}	V_{CNTL} = 5V		40		°C
REFEN Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.6			V
	V_{IL}	Shutdown			0.15	V

■ FUNCTIONAL DESCRIPTION

General Information

The UTC **UR5512** is a linear regulator designed for DDR SDRAM bus terminator application. The output, V_{OUT} is capable of sourcing or sinking current up to 2A peak while regulating the output voltage to within 20mV offset. The UTC **UR5512** has excellent response to load regulation while preventing shoot through. Active-low shutdown mechanism and fault protections. The UTC **UR5512** is available in several packages to meet different power dissipation and surface mount applications.

Output Voltage Regulation

The output voltage tracks the reference voltage applied at V_{REF} pin. Two internal NPN pass transistors act as the buffered output regulate the output voltage by sourcing current from V_{IN} pin or sinking current to GND pin. An internal Kelvin sensing scheme is use at the V_{OUT} pin to improve load regulation at various load current. Since the UTC **UR5512** exhibits excellent response to load transient, lesser amount of capacitors can be used.

Current Limit

An internal current limiting sensor is used to monitor the maximum output current to prevent damages from overload or short-circuit condition. Increasing the input voltage of V_{IN} or V_{CNTL} will get higher current-limit points.

Shutdown and Soft-Start

An additional function of the V_{REF} pin is acting as a shutdown control input that can be used for suspend to RAM functionality. Applying and holding a voltage below 0.15V to V_{REF} pin shuts down the output of the regulator. An external NPN transistor or N-channel MOSFET is used to pull down the V_{REF} pin voltage; while applying a “high” signal to turn on the transistor. During shutdown condition, the two pass transistors are turned off and the output V_{OUT} will tri-state; sourcing or sinking no current. When releasing the V_{REF} pin, the current through the resistor divider charges the capacitor Css to initiate a soft-start cycle.

Thermal Shutdown

If the junction temperature exceeds the thermal shutdown (T_J= +150°C) then the part will enter a shutdown state. A thermal sensor turns off both pass transistors, allowing the device to cool down. After the junction temperature reduces by 40°C, the regulator starts to regulate again; resulting in a pulsed output during continuous thermal overload conditions.

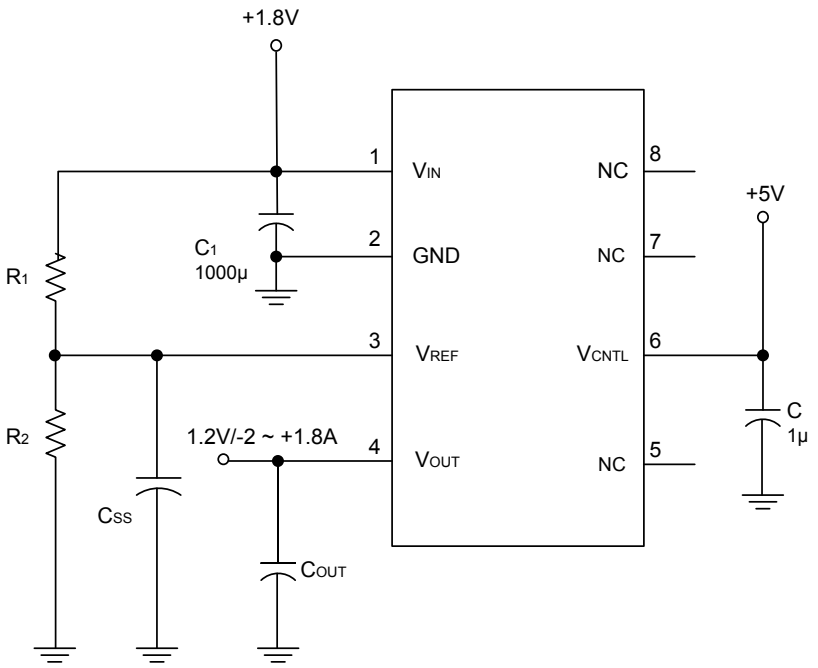
Power Inputs

Input powers up sequence are not required for V_{IN} and V_{CNTL}. Be careful; do not apply voltage to V_{OUT} when there is no V_{CNTL} voltage presented. This is due to the internal parasitic diodes between V_{OUT} to V_{IN} and V_{OUT} to V_{CNTL} which will be forward bias.

Reference Voltage

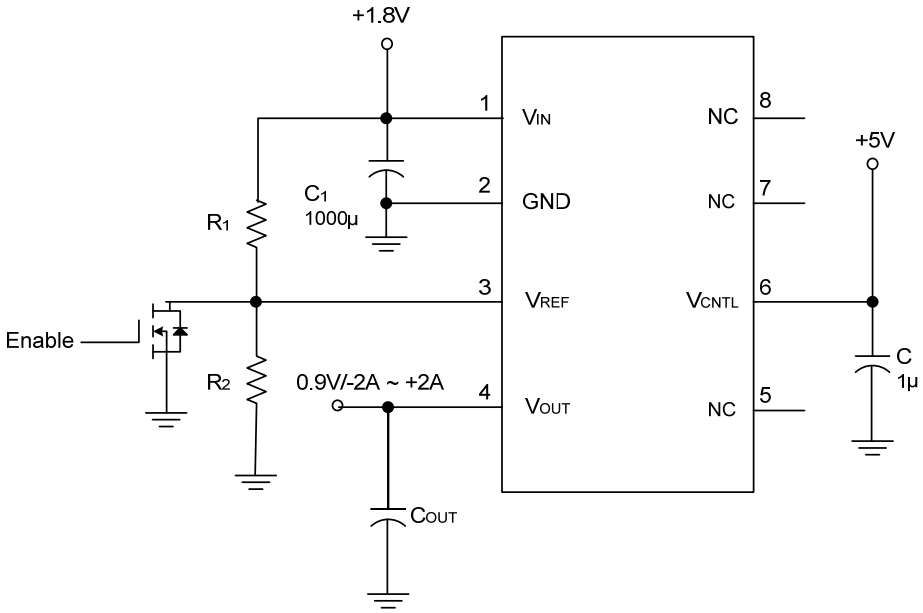
The reference voltage is programmed by a resistor divider between V_{IN} and GND pins. The recommended resistor is < 5kΩ to maintain the accuracy of the output voltage. For improved the performance, an external bypass capacitor can be used, located close to V_{REF} pin to help with noise. A ceramic capacitor can be use and is selected to be greater than 0.1μF. Do not place any additional loading on this reference input pin.

■ TYPICAL APPLICATIONS CIRCUIT



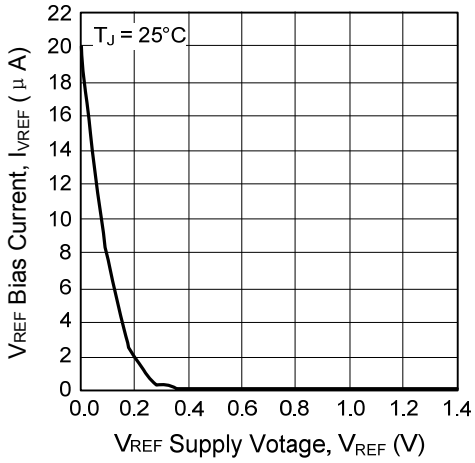
$$V_{REF} = V_{IN} \cdot \frac{R_2}{R_1+R_2} \text{ (V)}$$

V_{OUT} track V_{REF}

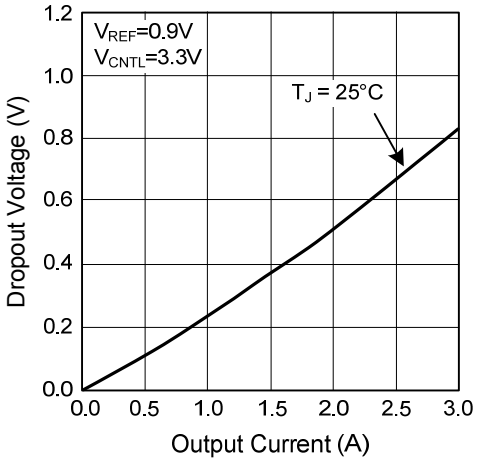


■ TYPICAL CHARACTERISTICS

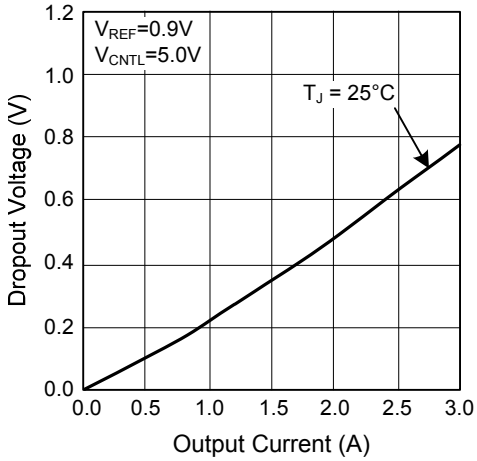
V_{REF} Bias Current vs. V_{REF} Supply Voltage



V_{IN} Dropout Voltage vs. Output Current



V_{IN} Dropout Voltage vs. Output Current



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