



LD1985

LINEAR INTEGRATED CIRCUIT

VERY LOW DROP AND LOW NOISE VOLTAGE REGULATOR LOW ESR CAP. COMPATIBLE, WITH INHIBIT FUNCTION

DESCRIPTION

The UTC **LD1985** is a 150mA fixed output voltage regulator. The ultra low drop voltage and the low quiescent current make them particularly suitable for low noise, low power applications, and in battery powered systems. In sleep mode quiescent current is less than 1µA when INHIBIT pin is pulled low. Shutdown Logic Control Function is available on pin 3 (TTL compatible). This means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption.

An external capacitor, $C_{BYP}=10nF$, connected between bypass pin and GND reduce the noise to 30µVrms.

Typical application is in cellular phone, palmtop laptop computer, personal digital assistant (PDA), personal stereo, camcorder and camera.

FEATURES

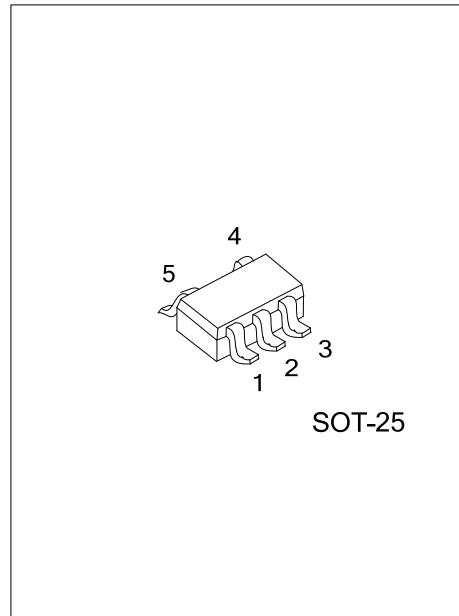
- * Very Low Dropout Voltage (280mV at 150mA and 7mV at 1mA Load)
- * Very Low Quiescent Current (2mA Typ. at 150mA Load and 80µA at no Load)
- * Output Current up to 150mA
- * Logic Controlled Electronic Shutdown
- * Output Voltage of 1.5, 1.8, 2.5, 2.8, 2.85, 3, 3.1, 3.2, 3.3, 3.5, 3.6, 3.8, 4, 4.7, 5V
- * Internal Current and Thermal Limit
- * Low Output Noise Voltage 30µVrms

ORDERING INFORMATION

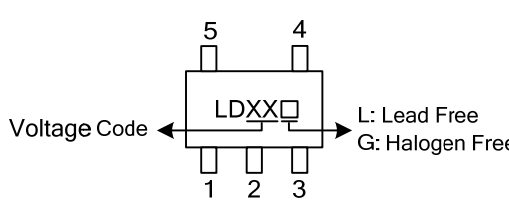
Ordering Number		Package	Packing
Lead Free	Halogen Free		
LD1985L-xx-AF5-R	LD1985G-xx-AF5-R	SOT-25	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

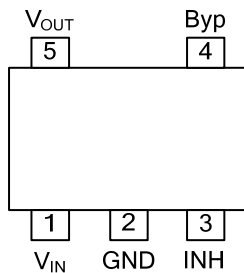
<p>LD1985L-xx-AF5-R</p>	<ul style="list-style-type: none"> (1) R: Tape Reel (2) AF5: SOT-25 (3) xx: Refer to Marking Information (4) G: Halogen Free, L: Lead Free
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MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-25	15:1.5V	
	18:1.8V	
	25:2.5V	
	28:2.8V	
	2J:2.85V	
	30:3.0V	
	31:3.1V	
	32:3.2V	
	33:3.3V	
	35:3.5V	
	36:3.6V	
	38:3.8V	
	40:4.0V	
	47:4.7V	
50:5.0V		

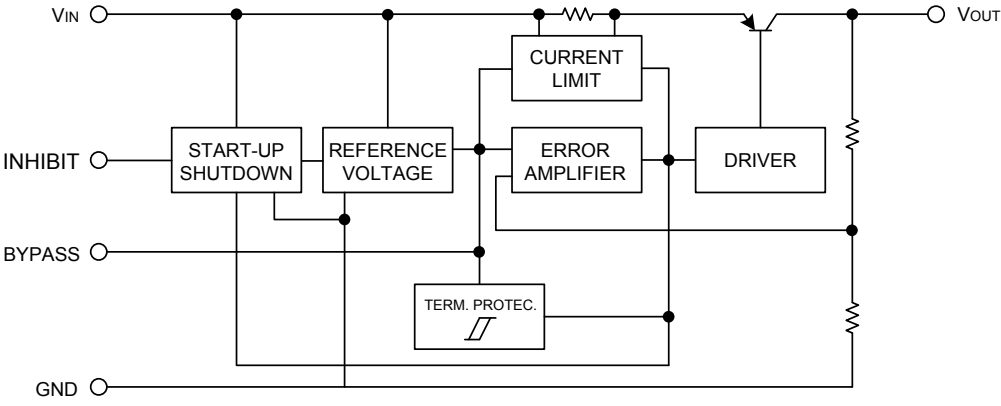
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V _{IN}	Input port
2	GND	Ground Pin
3	INHIBIT	Control switches ON/OFF. Inhibit is not internally pulled-up; it cannot be left floating. Disable the device when connected to GND or to a positive voltage less than 0.18V
4	Bypass	Bypass pin: capacitor to be connected to GND in order to improve the thermal noise performances.
5	V _{OUT}	Output port

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Input Voltage	V _{IN}	7	V
INHIBIT Input Voltage	V _{INH}	7	V
Output Current	I _{OUT}	Internally limited	
Power Dissipation	P _D	Internally limited	
Operating Junction Temperature	T _{OPR}	-40 ~ +85	°C
Storage Temperature	T _{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Case	θ _{JC}	81	°C/W

■ ELECTRICAL CHARACTERISTICS

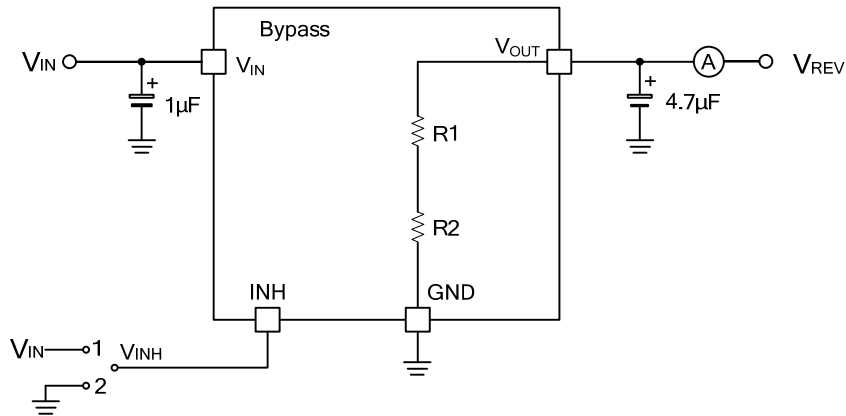
(T_J=25°C, V_{IN}=V_{OUT}+1V, I_{OUT}=1mA, V_{SHDN}=2V, C_I=1μF, C_O=1μF, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage	V _{I(OPR)}		2.5		7	V
Output Voltage	V _{OUT}	V _{IN} =2.5V	1.470	1.5	1.530	V
		I _{OUT} =1 ~ 150mA	1.455		1.545	V
Output Voltage	V _{OUT}	V _{IN} =2.8V	1.764	1.8	1.836	V
		I _{OUT} =1 ~ 150mA	1.746		1.854	V
Output Voltage	V _{OUT}	V _{IN} =3.5V	2.450	2.5	2.550	V
		I _{OUT} =1 ~ 150mA	2.425		2.575	V
Output Voltage	V _{OUT}	V _{IN} =3.8V	2.744	2.8	2.856	V
		I _{OUT} =1 ~ 150mA	2.716		2.884	V
Output Voltage	V _{OUT}	V _{IN} =3.85V	2.793	2.85	2.907	V
		I _{OUT} =1 ~ 150mA	2.764		2.936	V
Output Voltage	V _{OUT}	V _{IN} =4.0V	2.940	3.0	3.060	V
		I _{OUT} =1 ~ 150mA	2.910		3.090	V
Output Voltage	V _{OUT}	V _{IN} =4.1V	3.038	3.1	3.162	V
		I _{OUT} =1 ~ 150mA	3.007		3.193	V
Output Voltage	V _{OUT}	V _{IN} =4.2V	3.136	3.2	3.264	V
		I _{OUT} =1 ~ 150mA	3.104		3.296	V
Output Voltage	V _{OUT}	V _{IN} =4.3V	3.234	3.3	3.366	V
		I _{OUT} =1 ~ 150mA	3.201		3.399	V
Output Voltage	V _{OUT}	V _{IN} =4.5V	3.430	3.5	3.570	V
		I _{OUT} =1 ~ 150mA	3.395		3.605	V
Output Voltage	V _{OUT}	V _{IN} =4.6V	3.528	3.6	3.672	V
		I _{OUT} =1 ~ 150mA	3.492		3.708	V
Output Voltage	V _{OUT}	V _{IN} =4.8V	3.724	3.8	3.876	V
		I _{OUT} =1 ~ 150mA	3.686		3.914	V
Output Voltage	V _{OUT}	V _{IN} =5.0V	3.920	4	4.080	V
		I _{OUT} =1 ~ 150mA	3.880		4.120	V
Output Voltage	V _{OUT}	V _{IN} =5.7V	4.606	4.7	4.794	V
		I _{OUT} =1 ~ 150mA	4.559		4.841	V
Output Voltage	V _{OUT}	V _{IN} =6.0V	4.900	5	5.100	V
		I _{OUT} =1 ~ 150mA	4.850		5.150	V
Short Circuit Current	I _{SC}	R _L =0		400		mA

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Regulation	ΔV_{OUT}	$V_{IN} = V_{OUT} + 1V \sim 7V, I_{OUT} = 1mA$			30	mV
Dropout Voltage	V_D	$I_{OUT} = 0$		1	3	mV
		$T_J = -20 \sim 125^\circ C, I_{OUT} = 0$			5	mV
		$I_{OUT} = 1mA$		7	10	mV
		$I_{OUT} = 1mA, T_J = -20 \sim 125^\circ C$			15	mV
		$I_{OUT} = 10mA$		40	60	mV
		$I_{OUT} = 10mA, T_J = -20 \sim 125^\circ C$			90	mV
		$I_{OUT} = 50mA$		120	150	mV
		$I_{OUT} = 50mA, T_J = -20 \sim 125^\circ C$			225	mV
		$I_{OUT} = 150mA$		280	350	mV
		$I_{OUT} = 150mA, T_J = -20 \sim 125^\circ C$			575	mV
Quiescent Current	I_Q	$I_{OUT} = 0$		80	100	μA
		$T_J = -20 \sim 125^\circ C, I_{OUT} = 0$			150	μA
		$I_{OUT} = 1mA$		100	150	μA
		$I_{OUT} = 1mA, T_J = -20 \sim 125^\circ C$			200	μA
		$I_{OUT} = 10mA$		200	300	μA
		$I_{OUT} = 10mA, T_J = -20 \sim 125^\circ C$			400	μA
		$I_{OUT} = 50mA$		600	1050	μA
		$I_{OUT} = 50mA, T_J = -20 \sim 125^\circ C$			1200	μA
		$I_{OUT} = 150mA$		2000	3000	μA
		$I_{OUT} = 150mA, T_J = -20 \sim 125^\circ C$			4000	μA
		OFF MODE $V_{INH} < 0.18V$		0		μA
		OFF MODE $V_{INH} < 0.18V$ $T_J = -20 \sim 125^\circ C$			2	μA
Supply Voltage Rejection	SVR	$C_{BYP} = 0.01\mu F, C_O = 10\mu F, f = 1KHz$		45		dB
Control Input Logic Low	V_{IL}	$T_J = -20 \sim 125^\circ C$			0.15	V
Control Input Logic High	V_{IH}	$T_J = -20 \sim 125^\circ C$	2			V
Control Input Current	I_{INH}	$T_J = -20 \sim 125^\circ C, V_{SHDN} = 5V$		5	15	μA
		$T_J = -20 \sim 125^\circ C, V_{SHDN} = 0V$		0	-1	μA
Output Noise Voltage	eN	$B = 300Hz \sim 50KHz$ $C_{BYP} = 0.01\mu F, C_O = 10\mu F$		30		μV

■ REVERSE CURRENT TEST CIRCUIT



■ APPLICATION INFORMATION

EXTERNAL CAPACITORS

Like any low-dropout regulator, the UTC **LD1985** requires external capacitors for regulator stability. This capacitor must be selected to meet the requirements of minimum capacitance and equivalent series resistance. We suggest soldering input and outputting capacitors as close as possible to the relative pins.

INPUT CAPACITOR

An input capacitor whose value is $1\mu\text{F}$ is required with the UTC **LD1985** (amount of capacitance can be increased without limit). This capacitor must be located a distance of not more than 0.5" from the input pin of the device and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitors can be used for this capacitor.

OUTPUT CAPACITOR

The UTC **LD1985** is designed specifically to work with ceramic output capacitors. It may also be possible to use Tantalum capacitors, but these are not as attractive for reasons of size and cost. By the way, the output capacitor must meet both the requirement for minimum amount of capacitance and E.S.R. (equivalent series resistance) value. Due to the different loop gain, the stability improves for higher output versions and so the suggested minimum output capacitor value, if low E.S.R. ceramic type is used, is $1\mu\text{F}$ for output voltages equal or major than 3.8V, $2.2\mu\text{F}$ for V_{OUT} going from 1.8 ~ 3.3V, and $3.3\mu\text{F}$ for the other versions. However, if an output capacitor lower than the suggested one is used, it's possible to make stable the regulator adding a resistor in series to the capacitor.

IMPORTANT:

The output capacitor must maintain its ESR in the stable region over the full operating temperature to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times. This capacitor should be located not more than 0.5" from the output pin of the device and returned to a clean analog ground.

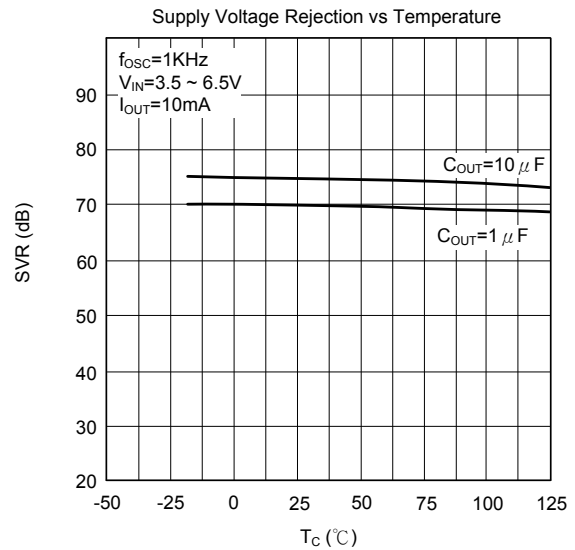
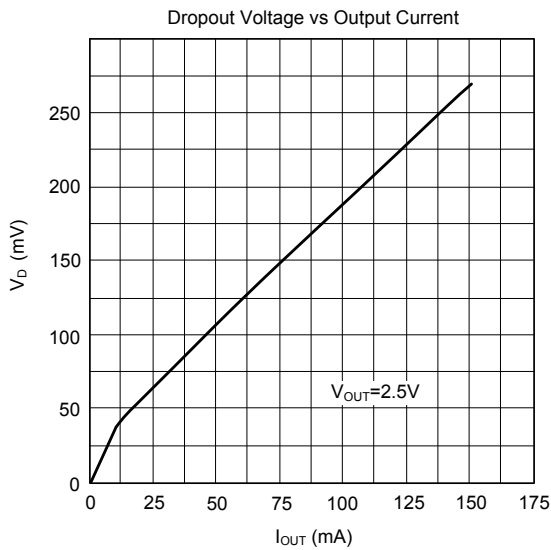
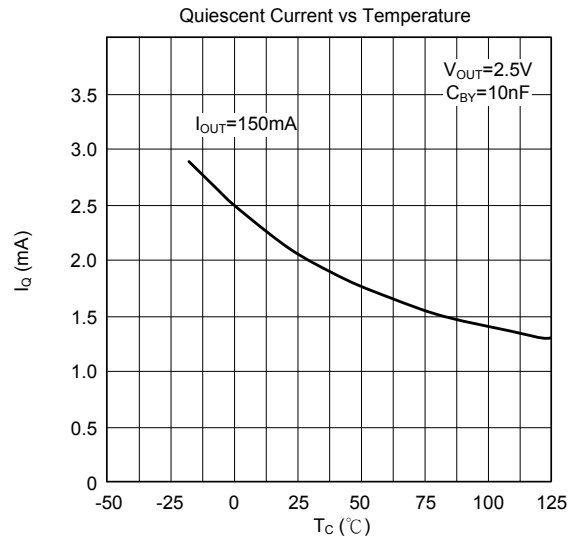
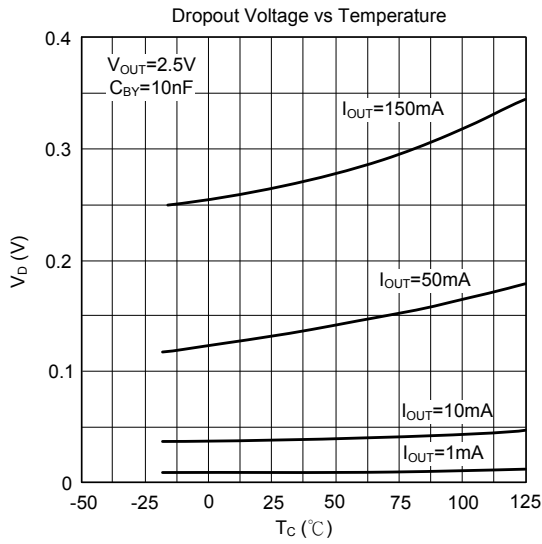
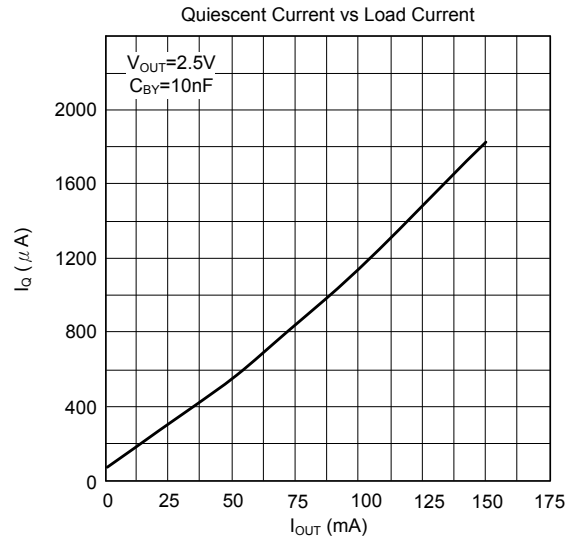
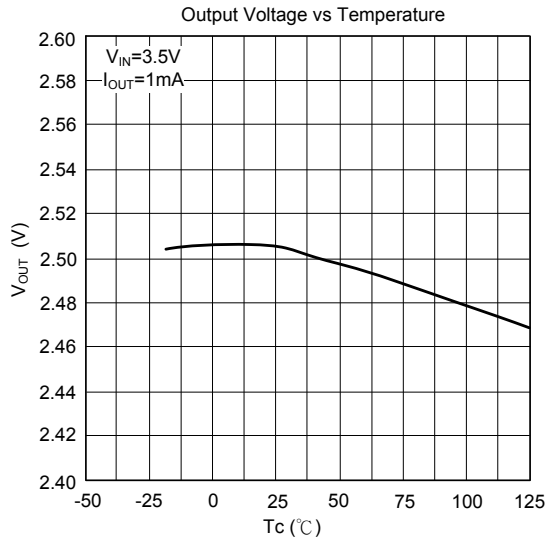
INHIBIT INPUT OPERATION

The inhibit pin can be used to turn OFF the regulator when pulled low, so drastically reducing the current consumption down to less than $1\mu\text{A}$. When the inhibit feature is not used, this pin must be tied to V_{IN} to keep the regulator output ON at all times. To assure proper operation, the signal source used to drive the inhibit pin must be able to swing above and below the specified thresholds listed in the electrical characteristics section under V_{IH} V_{IL} . Any slew rate can be used to drive the inhibit.

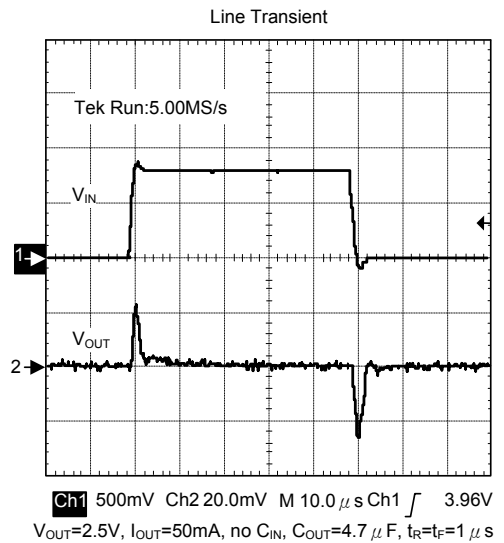
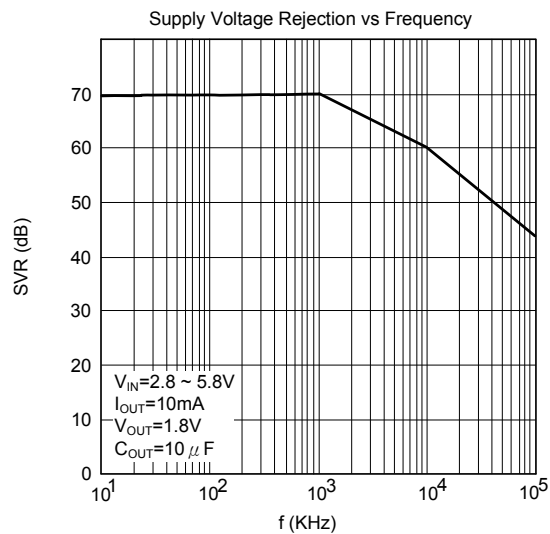
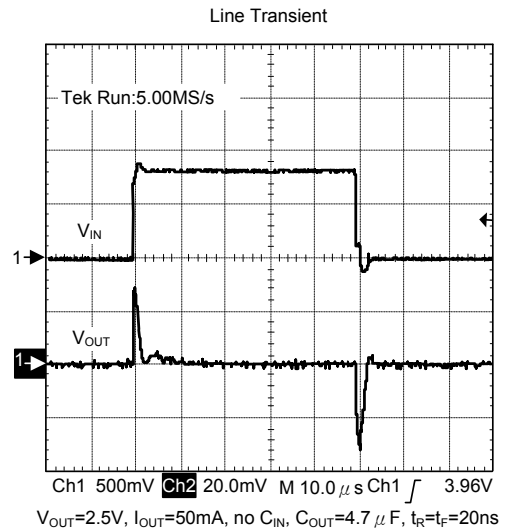
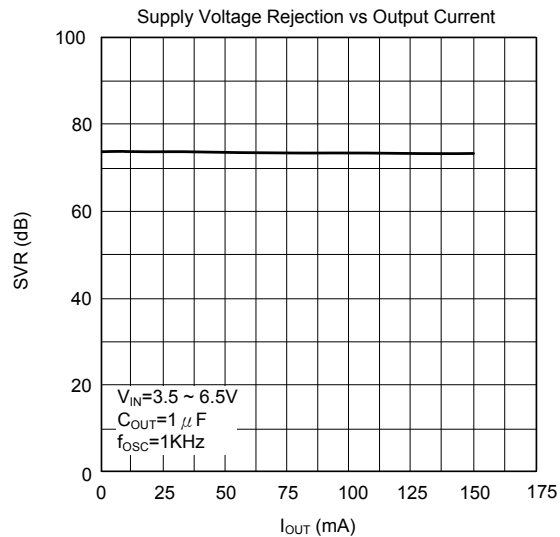
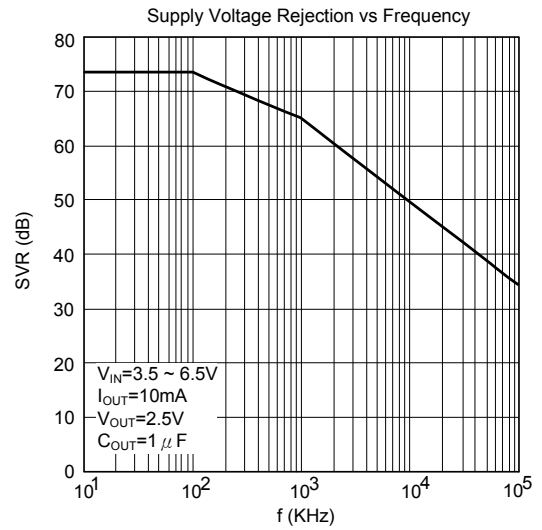
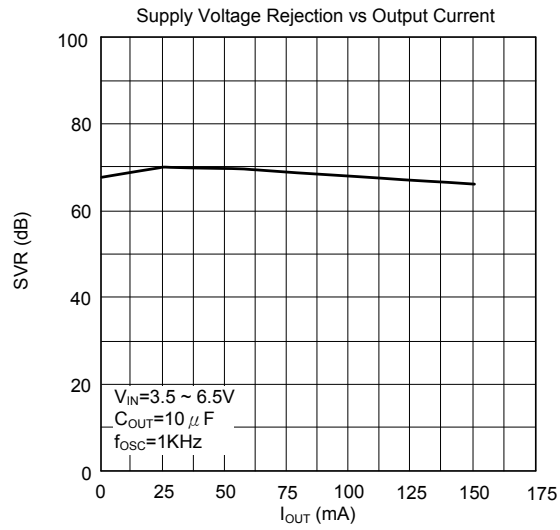
REVERSE CURRENT

The power transistor used in the UTC **LD1985** has not an inherent diode connected between the regulator input and output. If the output is forced above the input, no current will flow from the output to the input across the series pass transistor. When a V_{REV} voltage is applied on the output, the reverse current measured flows to the GND across the two feedback resistors. This current typical value is $160\mu\text{A}$. R1 and R2 resistors are implanted type; typical values are, respectively, 42.6 K Ω and 51.150 K Ω .

■ TYPICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, $C_{IN}=1\mu\text{F}$, $C_{OUT}=2.2\mu\text{F}$, $C_{BYP}=100\text{nF}$)

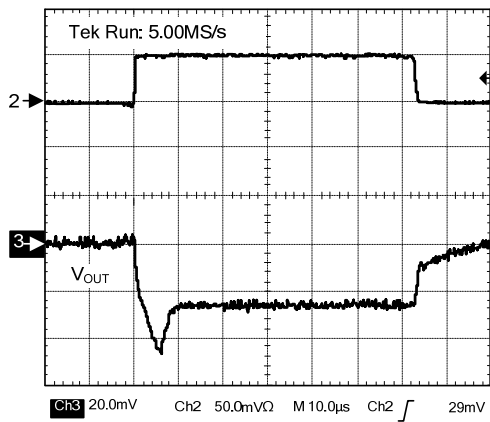


■ TYPICAL CHARACTERISTICS(Cont.)



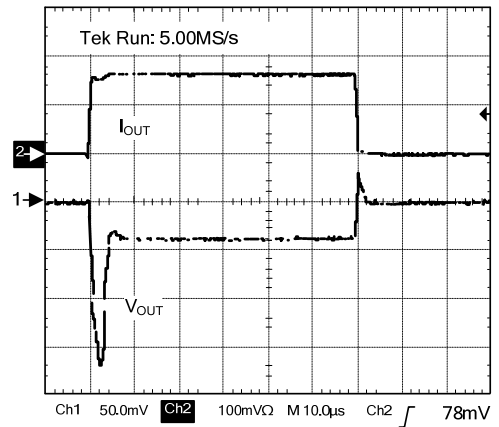
■ TYPICAL CHARACTERISTICS(Cont.)

Load Transient



$V_{OUT}=2.5V$, $I_{OUT}=0\sim 50mA$, no C_{IN} , $C_{OUT}=10\mu F$, $t_S=t_F=2ns$

Load Transient



$V_{OUT}=2.5V$, $I_{OUT}=50mA$, no C_{IN} , $C_{OUT}=4.7\mu F$, $t_S=t_F=20ns$

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