PSG5410

DATA SHEET
Preliminary

Synchronous Buck Controller with On-Demand Power® for DDR Memory VDDQ

Features

- Programmable output voltage (0.8V to 1.8V) supporting standard and low power DDR memory
- Configurable On-Demand Power® algorithm to adaptively scale regulated output voltage in correlation with monitored system activity
- System sensory interface to monitor activity and demand for regulated voltage domains
- Constant-on-time, voltage feed-forward, synchronous step-down PWM controller
- Input voltage range: 6.5V to 24V
- PWM and light-load operation
- Temperature compensated RDS(ON) current sensing
- Internal softstart
- Output over and under voltage protection
- Built-in output discharge circuit
- Power good output
- 1.8V linear regulator
- Serial programming interface
- QFN package

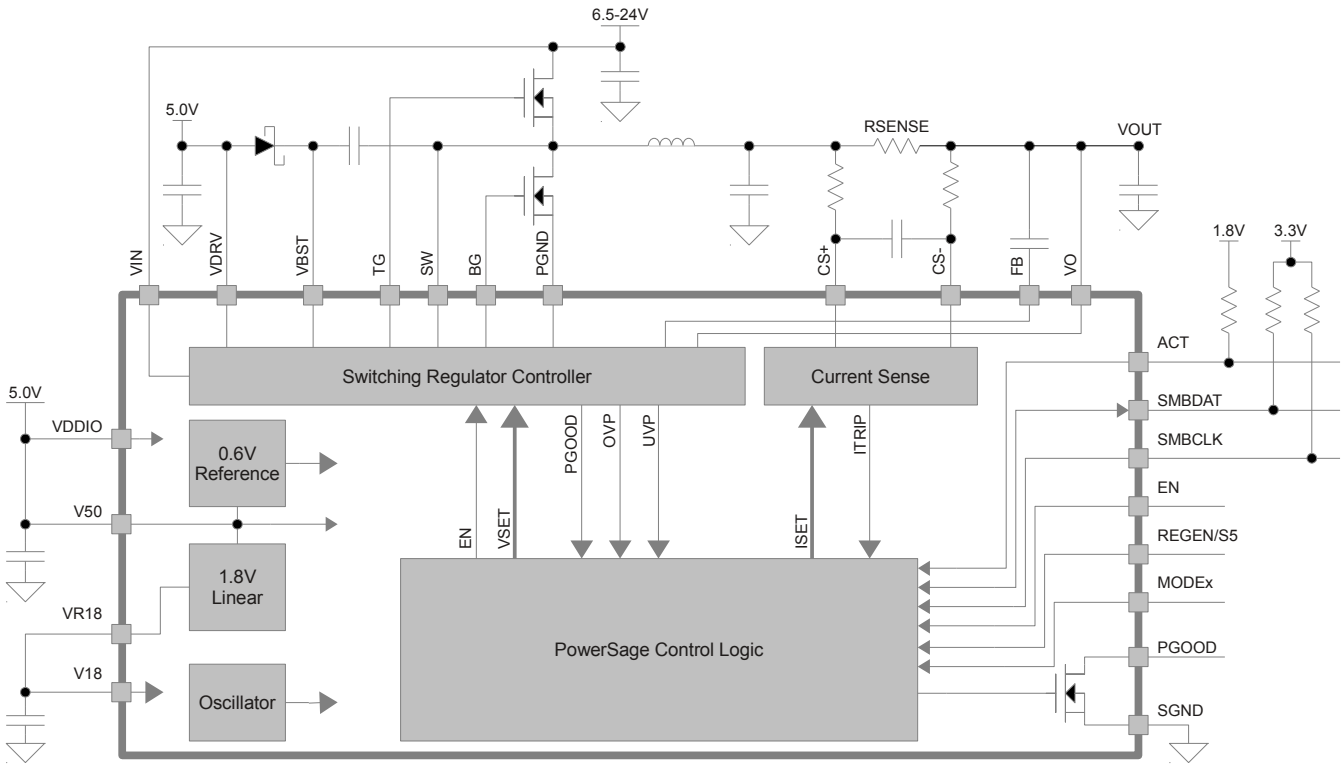
Description

The PSG5410 is a highly integrated power management IC with a synchronous step-down controller designed to supply VDDQ to DDR memory. A programmable interface for monitoring activity in the system, coupled with an advanced On-Demand Power® algorithm, enable the regulated output voltage of the integrated switching regulator to be adaptively scaled in correlation with actual system demand. The real-time tracking of supply voltage to system activity enables maximum system power savings by minimizing the power spent on maintaining worst-case headroom in the power distribution network.

Applications

- DDR2, DDR2L, LV-DDR2, LPDDR2 Memory Power Supplies
- DDR3, DDR3L, LV-DDR3, LPDDR3 Memory Power Supplies
- DDR4 Memory Power Supplies
- GDDR3, GDDR4, and GDDR5 Memory Power Supplies
- Mobile computers
- Servers

Functional Diagram

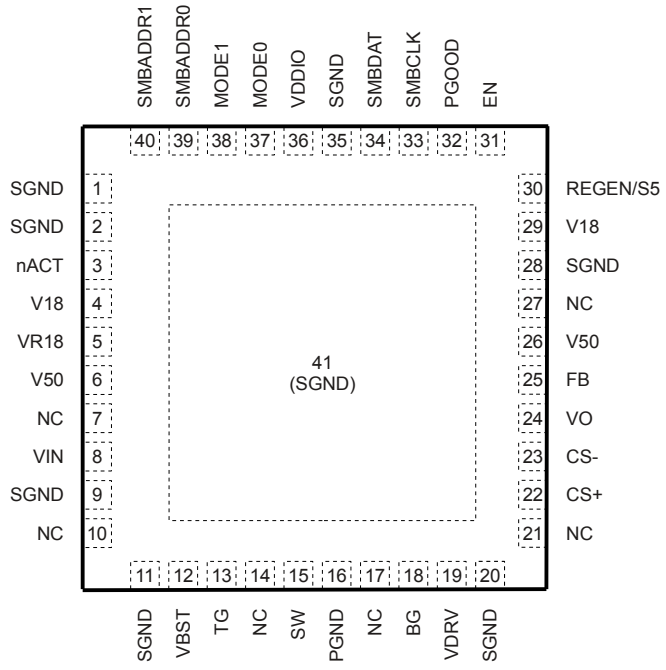


Absolute Maximum Ratings (Note 1)

PARAMETER	VALUE	UNIT
VIN to SGND	-0.3 to 30	V
V50 to SGND	-0.3 to 6	V
VDRV to PGND	-0.3 to 6	V
VBST to SW	-0.3 to 6	V
VR18 to SGND	-0.3 to 2.0	V
V18 to SGND	-0.3 to 2.0	V
VO, CS+, and CS- to SGND	-0.3 to 6	V
CS+ and CS- to V50	0.3	V
FB to SGND	-0.3 to 2.0	V
VBST to PGND	-0.3 to 30	V
SW to PGND	-2 to 30	V
BG to PGND	-0.3 to 6	V
BG to VDRV	0.3	V
TG to PGND	-2 to 30	V
TG to SW	-0.3 to 6	V
TG to VBST	0.3	V
All other pins to SGND	-0.3 to 6.0	V
All other pins to V50	0.3	V
Maximum Junction Temperature	125	°C

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PINOUT



40-LEAD (5mm x 5mm) PLASTIC QFN
EXPOSED PAD (PIN 41) IS SGND. MUST BE SOLDERED TO PCB.

Electrical Characteristics

Unless otherwise noted: V_{VIN} = 12V, V_{V50} = V_{VDRV} = 5V, V_{V18} = 1.8V, V_{SGND} = V_{PGND} = 0V, V_{EN} = V_{REGEN} = 3.3V, V_{SMBDAT} = V_{SMBCLK} = 3.3V, V_{nACT} = 3.3V, V_{PGOOD} = 3.3V, VR18 = No external load, T_A = 0°C to 85°C (Note 2). Typical values are at T_A = 25°C.

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		6.5		24	V
V_{V18}	Digital and analog supply voltage		1.62	1.8	1.98	V
V_{V50}	Analog supply voltage		4.5	5	5.5	V
V_{VDDIO}	Digital IO supply voltage		4.5	5	5.5	V
V_{VDRV}	Bottom gate drive supply voltage		4.5	5	5.5	V
V_{TGDRV}	Top gate drive supply voltage	V_{TGDRV} = V_{VBST} - V_{SW}	4.5	5	5.5	V
T_A	Operating ambient temperature		0		85	°C

Power Supplies

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{V18}	Digital and analog supply current Enabled Disabled	 V_{EN} = V_{REGEN} = 5V V_{EN} = V_{REGEN} = 0V			 1.7 28	 mA µA
I_{V50}	Analog supply current Enabled Disabled	No load on LDO18 output V_{EN} = V_{REGEN} = 5V V_{EN} = V_{REGEN} = 0V			 1.6 48	 mA µA
I_{VDRV}	Bottom gate driver supply current Enabled Disabled	All gate drivers are output low V_{EN} = V_{REGEN} = 5V V_{EN} = V_{REGEN} = 0V			 250 34	 µA µA
I_{VBST}	Top gate driver supply current Enabled Disabled	All gate drivers are output low. V_{EN} = V_{REGEN} = 5V V_{EN} = V_{REGEN} = 0V			 300 150	 µA µA

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SMBDAT, SMBCLK Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			5	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-5	µA
nACT Input						
V_{IH}	Input high voltage	nACT Low Voltage Input = 0 nACT Low Voltage Input = 1			1.4 0.65	V
V_{IL}	Input low voltage	nACT Low Voltage Input = 0 nACT Low Voltage Input = 1	0.8 0.35			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-10	µA
EN, REGEN						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			-10	µA
SMBDAT Output						
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.4	V
I_{OH}	High level output leakage current	Output Voltage = 5V			5	µA
PGOOD Output						
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.4	V
I_{OH}	High level output leakage current	Output Voltage = 5V			10	µA

Two-Wire Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus clock frequency		10		100	kHz
$t_{TIMEOUT}$	SMBDAT and SMBCLK time low for reset of SMBus	(Note 3)	25		35	ms

5MHz Oscillator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{1MHZ}	Internal oscillator frequency		4.5		5.5	MHz

Switching Regulators

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Gate Drivers						
$R_{TG(UP)}$	TG driver pull-up on resistance	TG high		2.1	8	Ω
$R_{TG(DOWN)}$	TG driver pull-down on resistance	TG low		1.5	4	Ω
$R_{BG(UP)}$	BG driver pull-up on resistance	BG high		1.4	8	Ω
$R_{BG(DOWN)}$	BG driver pull-down on resistance	BG low		0.7	4	Ω
$t_{DEAD(TG/BG)}$	Dead time	TG low to BG high (Note 4)		53		ns
$t_{DEAD(BG/TG}$	Dead time	BG low to TG high (Note 4)		30		ns
V_{OUT} Discharge						
I_{DISCHG}	V_{OUT} discharge current	V_{EN} = 5V, V_{REGEN} = 0V, V_{VO} = 0.5V	10			mA
Duty and Frequency Control						
$t_{ON(1)}$	On time	V_{VIN} = 20V, VSET[7:0] = 5Dh		315		ns
$t_{ON(2)}$	On time	V_{VIN} = 20V, VSET[7:0] = 00h		324		ns
$t_{ON(3)}$	On time	V_{VIN} = 15V, VSET[7:0] = 5Dh		432		ns
$t_{ON(4)}$	On time	V_{VIN} = 15V, VSET[7:0] = 00h		448		ns
$t_{ON(5)}$	On time	V_{VIN} = 10V, VSET[7:0] = 5Dh		686		ns
$t_{ON(6)}$	On time	V_{VIN} = 10V, VSET[7:0] = 00h		729		ns
$t_{OFF(MIN)}$	Minimum off time			312		ns
$t_{DEAD(MAX)}$	DCM timeout			1026	1130	ns
Softstart						
t_{SS}	Softstart time	MODE0 = 1, MODE1 = 0	1.2		2.5	ms
Power good (PG)						
$V_{PG(L)}$ $V_{PG(H)}$	PG trip voltage Lower PG trip voltage Upper PG trip voltage	With respect to set regulated voltage V_{VO} = 0.8V to 2V V_{VO} ramping negative V_{VO} ramping positive	 -0.21 0.10	 -0.16 0.16	 -0.10 0.21	V
t_{PGDEL}	PG delay	Entering PG window	115	130	145	µs
Over Voltage Protection (OVP)						
$V_{OVP(D)}$	Dynamic OVP trip voltage	With respect to set regulated voltage V_{VOx} = 0.8V to 2V	0.31	0.41	0.52	V
t_{OVPDEL}	OVP prop delay			10		µs
Under Voltage Protection (UVP)						
V_{UVP}	UVP trip voltage		0.54		0.66	V
t_{UVPDEL}	UVP prop delay		25		40	µs
t_{UVPEN}	UVP enable delay	From rising edge of REGxEN	1.9		3.8	ms
Over Current Protection (OCP)						
$V_{OCP(OFF)(6)}$	Over current protection offset voltage	OCPROG=6h		35		mV
$TC_{OCP(6)}$	Over current protection temperature coefficient	OCPROG=6h		131		µV/°C
$V_{OCP(OFF)(8)}$	Over current protection offset voltage	OCPROG=8h		45		mV
$TC_{OCP(8)}$	Over current protection temperature coefficient	OCPROG=8h		168		µV/°C
$V_{OCP(OFF)(A)}$	Over current protection offset voltage	OCPROG=Ah		55		mV

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$TC_{OCP(A)}$	Over current protection temperature coefficient	OCPROG=Ah		205		µV/°C
$V_{OCP(OFF)(C)}$	Over current protection offset voltage	OCPROG=Ch		65		mV
$TC_{OCP(C)}$	Over current protection temperature coefficient	OCPROG=Ch		243		µV/°C
V_{ZC}	Zero cross detection comparator offset		-5		5	mV

1.8V Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VR18}	1.8V linear regulator output voltage	$0 < I_{VR18} < 5mA$	1.71		1.98	V

Current Sense

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_p	Propagation delay	$V_{CS+} - V_{CS-}$ = 10mV to 40mV, ITRIP = 25mV			10	µs
I_{CS+}	CS+ input bias current	V_{CS+} = 1.8V, V_{CS-} = 0.8V to 1.8V			120	nA
I_{CS-}	CS+ input bias current	V_{CS+} = 1.8V, V_{CS-} = 0.8V to 1.8V			120	nA
$V_{TRIP(40)}$	Programmable trip voltage	ISETx[7:0] = AFh		40		mV
$V_{TRIP(10)}$	Programmable trip voltage	ISETx[7:0] = 1Dh		10		mV

Note 2 Parts are tested at 25°C and 85°C. Temperature limits established by characterization and are not production tested.
Note 3 Exceeding $t_{TIMEOUT}$ will reset the SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.
Note 4 Delay times are measured using 50% levels.
Note 5 Guaranteed by design. Not Production Tests.

Pin Functions

NAME	PIN	IO (Note 6)	DESCRIPTION
V18	4, 29	P	1.8V power supply for both digital and analog circuitry. Decouple each pin to SGND with a capacitor.
V50	6, 26	P	5V power supply for analog circuitry. Decouple each pin to SGND with a capacitor.
VDDIO	3, 6	P	IO power supply. Decouple to SGND with a capacitor. This is the input supply for digital IO drivers and receivers.
VIN	8	P	High voltage sense input. Decouple to SGND with a capacitor.
SGND	1, 2, 9, 11, 20, 28, 35	P	Small signal ground. All small signal components should connect to this ground. Connect SGND to PGND at one point. Pin 41 is the exposed pad.
PGND	16	P	Regulator power grounds. Connect these closely to the appropriate sources of the bottom external N-channel MOSFET and the negative terminal of the VDRV decoupling capacitors. Connect PGND to SGND at one point. Refer to Layout Guidelines.
VDRV	19	P	Bottom gate driver supply. Decouple to its respective PGND with a capacitor.
VR18	5, 29	PO	Internal 1.8V linear regulator output. Decouple to SGND with a capacitor. This output can be connected to V18 as the 1.8V supply.
CS+	22	A	Current sense differential amplifier input. The positive input to the amplifier is normally connected to current sensing resistors through an RC filter.
CS-	23	A	Current sense differential amplifier input. The negative input to the amplifier is normally connected to current sensing resistors through an RC filter.
VO	24	A	Output voltage remote sense inputs.
FB	25	A	Output voltage feedback. Connection point for external ripple injection circuitry or leave floating.
nACT	3	I	Activity input. Logic threshold level is digitally programmable. A logic low indicates that the respective load is active. A logic high indicates that the respective load is idle. Connect directly to VDDIO if not used. Do not leave floating.
SMBDAT	34	IOD	SMBus data input/output. The PSG5410 is configured as an SMBus device.
SMBCLK	33	IOD	SMBus clock input. The PSG5410 is configured as an SMBus device.
SMBADDRx	39, 40	I	SMBUS address input. This configures the PSG5410 device to one of four different SMBUS addresses
PGOOD	32	O	Power good indicator output. This open-drain output is pulled to ground when the regulated output voltages leave the regulation window. The regulator has a fixed 512us power good delay, additional programmable delay, and mask.
EN	31	I	Enable input. A logic low disables the switching regulator and forces the PSG5410 into a low-power standby mode. A logic high enables the PSG5410. Switching regulator operation is dependent on the REGEN input. Connect directly to V50 if not used. Do not leave this pin floating. The output discharge circuit is disabled when EN is a logic low.
REGEN/S5	30	I	Regulator enable input. A logic low disables the switching regulator and activates the output discharge circuit. When the input is a logic high, the operational state of the regulator is dependent on the internal regulator enable bit. Connect directly to V50 if not used. Do not leave this pin floating. Connect this to the S5 state node to shut-down the regulator during soft-off or suspend-to-disk.
MODEx	37, 38	I	Mode-select for default output voltage. These digital inputs indicate whether the regulator should start-up for DDR2 (1.8V), DDR3, DDR2L (1.5V), DDR3L (1.35V), or DDR4, LPDDR3, LPDDR2 (1.2V).
VBST	12	P	Boosted floating driver supplies for the top gate driver.
SW	15	A	Switch node connections to power inductors.
TG	13	AO	Top gate driver output.
BG	18	AO	Bottom gate driver output.
NC	7, 10, 14, 17, 21, 27	X	No Connect. These pins should be left floating.

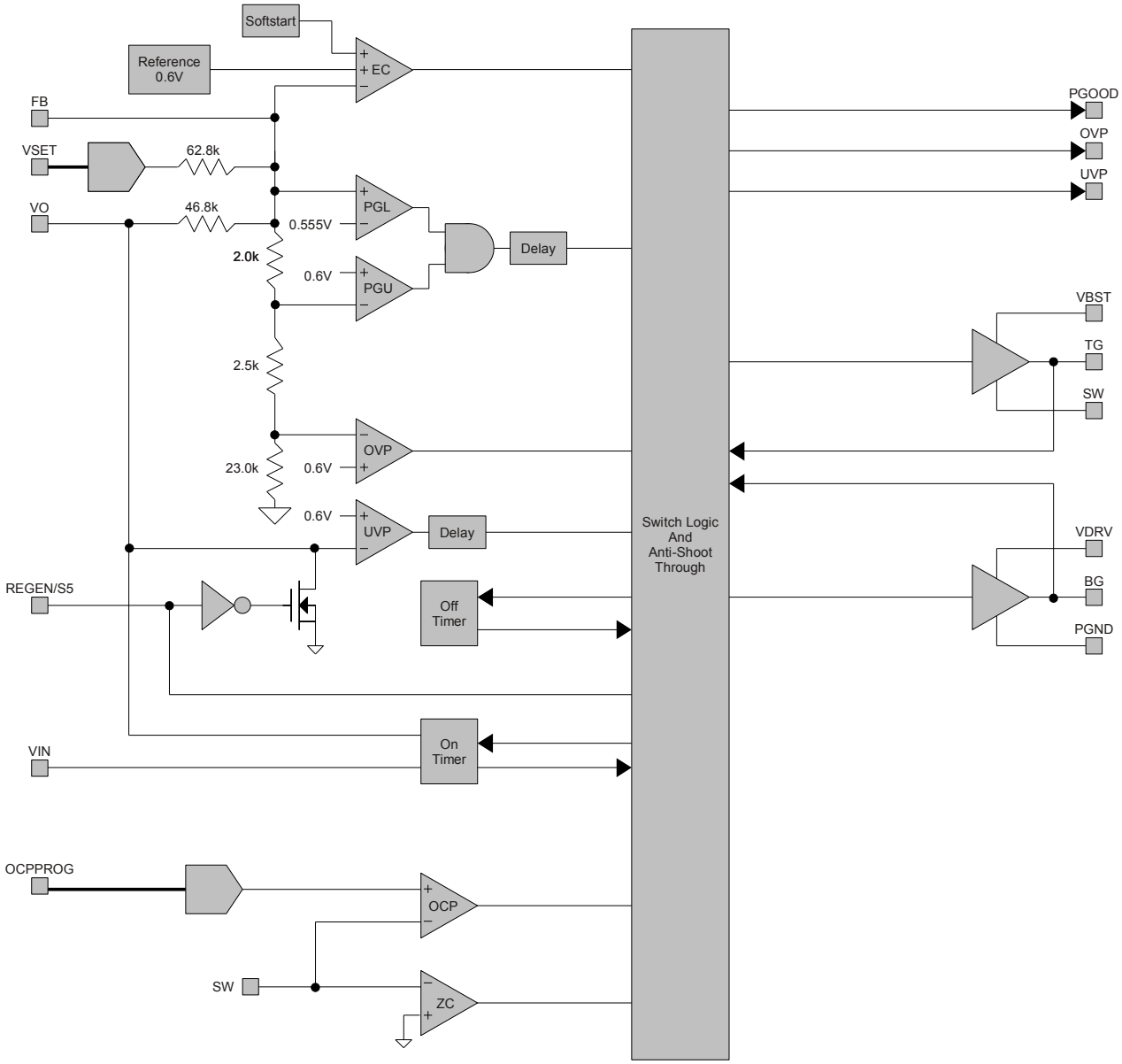
Note 6 P = Power, A = Analog, I = Input, O = Output, OD = Open Drain, IOD = Bidirectional Open Drain, X = Unconnected

1 Synchronous PWM Controller

This is a high efficiency constant on time input voltage feed-forward step-down synchronous PWM controller. The controller automatically switches between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) depending on the average inductor current.

In CCM, the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. The top external MOSFET remains on for a fixed amount of time that is dependent on the input and output voltage relationship. When the top external MOSFET is turned off, the bottom external MOSFET is turned on until the inductor current is less than the valley current limit and the error comparator shows that output voltage is in error.

In DCM, the inductor current is not allowed to reverse. Therefore, the bottom MOSFET is turned off when the inductor current reaches zero. Both the top and bottom external MOSFETs remain off until the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. During the time that both external MOSFETs are turned off, the output voltage is supplied by the output capacitor.



1.1 On-Time/Off-Time

The on-time of the PWM controller is dynamically adjusted on a cycle-by-cycle basis to maintain a constant ripple current in the power inductor. The input and output voltage of the switching regulator is monitored to adapt the period of a one-shot timer that sets the on-time of the controller. The typical on-time is:

$$t_{ON} = \frac{5.83\,\mu V \cdot s}{V_{VIN} - V_{VO}}$$

The off-time is dependent on the instantaneous voltage error and the minimum off time. For a constant load and constant input/output voltage, the off time can be estimated by:

$$t_{OFF} \approx t_{ON}\frac{(V_{VIN} - V_{VO})}{V_{VO}}$$

Since the on-time and off-time can be estimated for a constant load and constant input/output voltage, the switching frequency for can be estimated in this condition by:

$$f_{SW} \approx \frac{1}{t_{ON} + t_{OFF}}$$

1.2 DCM Operation

During light load, the PWM controller enters discontinuous conduction mode, DCM, to maintain high conversion efficiency. DCM is entered when the inductor valley current reaches zero and the bottom external MOSFET is turned off to prevent the inductor current from reversing. This decreases the effective switching frequency of the controller and reduces conversion losses in the MOSFET drivers. When both the top and bottom external MOSFETs are off, the output voltage is maintained by the output capacitance. Once the light load discharges the output capacitance to the point where the error comparator detects that the output voltage is in error, a new switching cycle is started by turning on the top external MOSFET. The on-time is not effected. The load current where the controller transitions between CCM and DCM is:

$$I_{LOAD,trans} = \frac{1}{2}\left(\frac{V_{VIN} - V_{VO}}{L}\right)t_{ON}$$

The time both external MOSFETs can remain off is dependent on the instantaneous voltage error and the DCM timeout. For a constant load and constant input/output voltage, the DCM time can be estimated by:

$$t_{DCM} \approx \frac{(t_{ON} + t_{OFF})I_{LOAD,trans}}{I_{VO}} - (t_{ON} + t_{OFF})$$

Since the on-time, off-time, and DCM time can be estimated for a constant load and constant input/output voltage, the switching frequency can be estimated in this condition by:

$$f_{SW} \approx \frac{1}{t_{ON} + t_{OFF} + t_{DCM}}$$

The maximum time both external MOSFETs can remain off while in DCM mode is limited to 1026µs. In the event of a DCM timeout, the bottom external MOSFET is turned on for the minimum off-time to recharge the boost capacitor. Subsequently, the top external MOSFET is only turned on if the error comparator detects that the output voltage is in error. If the output voltage is not in error, the PWM controller will immediately re-enter DCM mode.

1.3 MOSFET Drivers

Both the top and bottom MOSFET drivers are designed to drive N-channel external power MOSFETs. The bottom MOSFET driver pulls BG down to PGND to turn off the external MOSFET, and it pulls BG up to VDRV to turn on the external MOSFET. Likewise, the top external MOSFET driver pulls TG down to SW to turn off the external MOSFET, and it pulls TG up to VBST to turn on the external MOSFET. The combined power dissipation of both MOSFET drivers in a PWM controller attributed to switching events is:

$$P_{DIS} = V_{VDRV} \times f_{SW} \times (Q_T + Q_B)$$

where f_{SW} is the switching frequency, Q_T is the gate charge of the top external MOSFET, and Q_B is the gate charge of the bottom external MOSFET.

The top MOSFET driver has a floating power supply V_{VBST} - V_{SW} that is derived from the 5V supply using a boost capacitor and boost diode. The boost capacitor is recharged through the boost diode from the 5V supply whenever the bottom external MOSFET is turned on and SW is pulled to PGND.

1.4 Anti-Shoot Through Circuitry

In a synchronous PWM topology, it is possible to get shoot-through current from VIN to PGND when both the top and bottom external MOSFETs are fully or partially conducting. To prevent this, a dead time where both MOSFETs are off is internally generated by adding a delay from the turn off of the top external MOSFET to the turn on of the bottom external MOSFET and

from the turn off of the bottom external MOSFET to the turn on of the top external MOSFET. The voltage and discharge current of both the top and bottom external MOSFETs are monitored to dynamically optimize the driver dead time and increase conversion efficiency.

1.5 Start-Up

The PWM controller is enabled when both the EN and REGEN/S5 pins are driven high. When enabled, there is a brief delay while the internal analog circuitry is powered-on and stabilized. Next, an internal DAC, linearly ramps the error comparator reference voltage from 0V to VREF. This forces the regulated output voltage to linearly increase from 0V to the final programmed output voltage in 1.5ms.

1.6 Shutdown

The PWM controller is disabled when either the EN or REGEN pins are driven low. When disabled, the internal analog circuitry of the PWM controller is forced into a low power mode.

1.7 Output Discharge Circuitry

A 10mA minimum output discharge current sink is connected through VO. The output discharge is active when the REGEN pin is driven low. The output discharge circuitry is not active when EN is driven low.

1.8 Power good

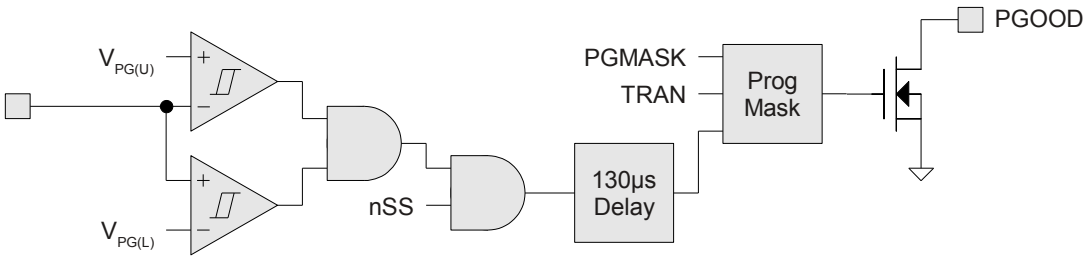
The PGOOD pin is an open-drain output that indicates if the output voltage of the PWM controller, measured at pin VO, is within regulation. In fixed output voltage operation, the PGOOD pin is high impedance if the regulator output is within regulation, and the PG pin is pulled to ground if the regulator output is out of regulation. Additionally, the PG pin is pulled low if the regulator is disabled or operating in soft-start. The power good regulation window is defined in the Electrical Characteristics table.

To minimize the effect of noise on the VO pin, there is an internal fixed 130µs delay on the PGOOD output. Thus, VO must be inside the regulation window for at least 130µs before the PGOOD pin becomes high impedance. However, the PGOOD pin will be pulled low immediately after VO leaves the regulation window.

During controlled output voltage transitions, a programmable masking of the PGOOD signal is enabled. While the On-Demand Power controller is ramping VSET control voltage from one fixed voltage to a new fixed voltage, the PGOOD pin will retain its state previous to the beginning of an output voltage transition until the output voltage is complete. Thus, if the PGOOD pin was pulled low at the beginning of a voltage transition, the PGOOD pin will remain pulled low throughout the entire output voltage transition, even if the transition event causes the output voltage to enter the regulation window. Likewise, if the PGOOD pin was high impedance at the beginning of a voltage transition, the PGOOD pin will remain high impedance throughout the entire output voltage transition, even if the transition event causes the output voltage to leave the regulation window. The programmable mask during output voltage transitions enable the On-Demand Power® controller to adjust the programmed output voltage VSET at a rate faster than the output of the PWM controllers can respond without inadvertently causing the PGOOD pin to be pulled low.

Furthermore, the programmable mask can be optionally extended for a programmable time period past the completion of an output voltage transition event. This feature allows the PWM controller output voltage some time to settle within the regulation window after a voltage transition occurs. This can be important when the output voltage step is large and/or the slew rate of VSET is high.

The complete power good logic is shown below. nSS is low when the respective PWM controller is operating in softstart mode. TRAN indicates if VSET is transitioning. PGMASK sets the programmable mask time period.



Power good logic

1.9 Output Voltage Programming

The regulated output voltage of the PWM controllers is controlled with a DAC that is programmed by the On-Demand Power® controller. The output voltage is determined by the VSET register which is assigned through VMAN or VODPx settings. The valid output voltage range is 2V to 0.8V corresponding to codes 0x00 to 0xE0. The output voltage is defined by:

$$V_{VO} = 2 - \left[1.2\frac{VSET[7:0]}{0xE0}\right]$$

1.10 Mode Select

The PSG5410 is designed to support Standard DDR Memory (DDR2, DDR3, DDR4), lower voltage versions of DDR Memory (DDR2L, DDR3L, LV-DDR2, LV-DDR3), and Mobile Memory (LPDDR2 and LPDDR3). The mode select pins should be set to define the system memory. This controls the default state of VMAN and VODPx and allows the regulator to start-up to the appropriate voltage level without serial programming. The MODE pins are monitored by the PSG5410 only at power-on-reset (before the soft-start ramp) and the VMAN and VODPx registers are immediately written. Tie each MODE pin to AGND for logic 0 and 5V for logic 1. The following table outlines MODE0/MODE1 pin operation:

MODE1	MODE0	Voltage	ODPVOUTx	Memory Mode
0	0	1.8V	0x25	DDR2
0	1	1.5V	0x5D	DDR3, DDR2L, LV-DDR2
1	0	1.35V	0x79	DDR3L, LV-DDR3
1	1	1.2V	0x95	DDR4, LPDDR3, LPDDR2

Please note: Other voltages can be supported if required. Please contact Packet Digital with special requests.

1.11 Over Current Protection

Over current protection is provided by monitoring the drain-to-source voltage across the bottom external MOSFET when it is turned on. As long as the sensed voltage drop is greater than the programmed voltage threshold, the bottom external MOSFET is forced to remain on. This effectively limits the maximum value of the power inductor valley current.

The over current protection limit is programmed with the OCPROG bits over the SMBus interface. The voltage threshold is temperature compensated to match the temperature dependency of the bottom external MOSFET. The programmed voltage threshold is:

$$V_{TH} = 0.37893(OCPROG+1)((4.94\times10^{-5})T_J+0.01196)$$

For improved accuracy, there should be a good thermal connection between the MOSFET and the PSG5410.

1.12 Output Over and Under Voltage Protection

The output voltage of the PWM controller is sensed at the VO pin. If the sensed voltage exceeds either the fixed output over voltage threshold or the dynamic over voltage threshold, the bottom external MOSFET is turned on to discharge the output capacitance and return the output voltage to safe operating level. Once the over voltage condition is no longer sensed, the PWM controller resumes normal operation.

When the sensed output voltage drops below the under voltage threshold, the PWM controller condition is automatically disabled. The EN pin or REGEN/S5 pin must be toggled to clear the under voltage condition. This response is desired because an under voltage condition will follow an output short circuit that triggers the over current protection circuitry. This protects the PWM controller and associated circuitry against an output short circuit.

1.13 UVLO Protection

All power supplies are monitored to ensure they are of suitable voltage before the PWM controller is enabled.

2 Regulator Circuit Design

2.1 Inductor Selection

The maximum load current and inductor ripple current determine the value of the inductor. The value of the inductor ripple current ΔI_L can be calculated with input voltage V_{IN}, output voltage V_O, and on time t_{ON}:

$$\Delta I_L = t_{ON}\left(\frac{V_{VIN}-V_{VO}}{L}\right)$$

Since the on-time of the PWM controller is adjusted to maintain a constant ripple current, ΔI_L is determined solely by the inductance value. A lower ripple current improves efficiency by reducing losses in the inductor and ESR losses in the input and output capacitors at the cost of a physically larger inductor. A ΔI_L that is 25% to 50% of $I_{LOAD(MAX)}$ is reasonable for balancing efficiency and inductor size.

An inductor should be selected to have the lowest possible DC resistance to maximize efficiency. Care must be taken to not saturate at the peak inductor current which can be determined by:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

2.2 Output Capacitor Selection

Equivalent series resistance (ESR) is a dominant qualification for output capacitor selection. Specialty polymer capacitors, such as Kemet KO-CAP, are recommended due to high ripple current capability and low ESR at operation frequencies.

Output capacitance should be selected to provide an acceptable output voltage ripple ΔV_{VO} which can be determined by the ESR and magnitude of the output capacitor. The capacitance must be sufficiently large for stability, however the capacitance value relates to the increasing physical size needed to decrease ESR. Consequently, the selection of C_{OUT} is primarily driven by ESR and can be found by:

$$ESR \leq \frac{\Delta V_{VO}}{\Delta I_L}$$

2.3 Input Capacitor Selection

Select the input capacitors based on the expected maximum input ripple RMS current. This current varies with the load and input voltage. The maximum input ripple RMS current occurs at maximum load and can be estimated by:

$$I_{RMS(MAX)} \approx \frac{I_{LOAD(MAX)}}{V_{VIN}}\left[(V_{VO})(V_{VIN} - V_{VO})\right]^{1/2}$$

2.4 MOSFET Selection

The top and bottom MOSFET should be chosen for low $R_{DS(ON)}$ for increased efficiency, however this must be weighed with increased gate capacitance which increases switching losses. Switching losses are increased in the top MOSFET at high input voltages.

The bottom MOSFET should be placed in parallel with a Schottky diode. Many manufacturers provide a single package device for the MOSFET and diode.

3 1.8V Linear Regulator

One 1.8V, 25mA linear regulator is provided. This regulator powers the internal digital logic of the PSG5410 through power pins V18 and may be used for light loads in the system. An external decoupling capacitor is required between VR18 and SGND. This capacitor may be ceramic and should be at least 4.7uF.

4 On-Demand Power® Operation

PSG5410 internal registers are programmable via SMBus to control On-Demand Power (ODP) circuitry. Activity is monitored by the programmed current sense and the ACT input. When the ODPEN bit of ODPCON is set, the corresponding output voltage will be managed based on configuration settings and signals gathered from activity sensing inputs.

4.1 Output Voltage

Once ODP is enabled, output voltage will vary based on system demand, managed by ODP algorithms. Voltages for activity states correspond to the voltage levels set in the ODPVOUTx registers. At power-on, the ODPVOUTx registers will be set corresponding to the mode-select pins. SMBus writes are required to modify the registers for ODP operation.

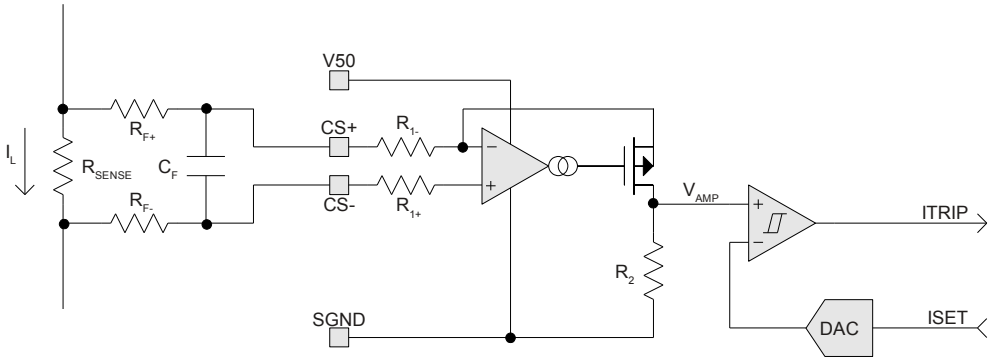
4.2 nACT Input

nACT is a system control input to the ODP algorithm. A logic low signal on this pin indicates a transition to a higher power state. Configuring this input signal to the ODP algorithm is done through the configuration register ODPACT. The nACT input can be used to control a state transition of the ODP state machine.

The nACT input can be selected for standard or low voltage digital input though the ACTCON register. V_{IH} and V_{IL} levels for standard and low voltage inputs are defined in the electrical characteristics.

4.3 Current Sense

The load current sense circuit detects if the load current I_L is above or below a programmable threshold I_{TRIP}. A high-side current sense amplifier gains the voltage V_{CS} across a sense resistor R_{SENSE} in response to the load current I_L. The output of the current sense amplifier is compared to a programmable threshold voltage V_{TRIP} that is set using an internal 8-bit DAC. The output of the comparator circuit is high if I_L is greater than I_{TRIP} and low if I_L is less than I_{TRIP}. The comparator includes internal hysteresis to help reject noise.



Current sense circuitry

The load current sense resistor R_{SENSE} should be selected such that the maximum voltage drop $V_{cs(MAX)}$ across the sense resistor does not exceed the maximum differential input voltage of the current sense amplifier. For a maximum load current of I_{MAX}, the maximum value of R_{SENSE} is:

$$R_{SENSE(MAX)} = \frac{V_{CS(MAX)}}{I_{MAX}}$$

Likewise, the minimum value for R_{SENSE} depends on the minimum load current $I_{TRIP(MIN)}$ that must be detected:

$$R_{SENSE(MIN)} = \frac{V_{CS(MIN)}}{I_{TRIP(MIN)}}$$

The positive and negative sense traces should be routed as a differential pair and Kelvin connected to the sense resistor.

The additional amplifier input offset voltage induced by input resistors R_{F+} and R_{F-} is:

$$V_{OS} = I_{CS-}R_{F-} - I_{CS+}R_{F+}$$

4.4 Activity Selection

The ODPACT register is used to select the types of activity inputs that will be used for ODP. The following table shows how the inputs are controlled by these bits:

ODPACT1	ODPACT0	Activity
0	0	None
0	1	Digital Only
1	0	Current Sense Only
1	1	Digital OR Current Sense

5 Two Wire Interface

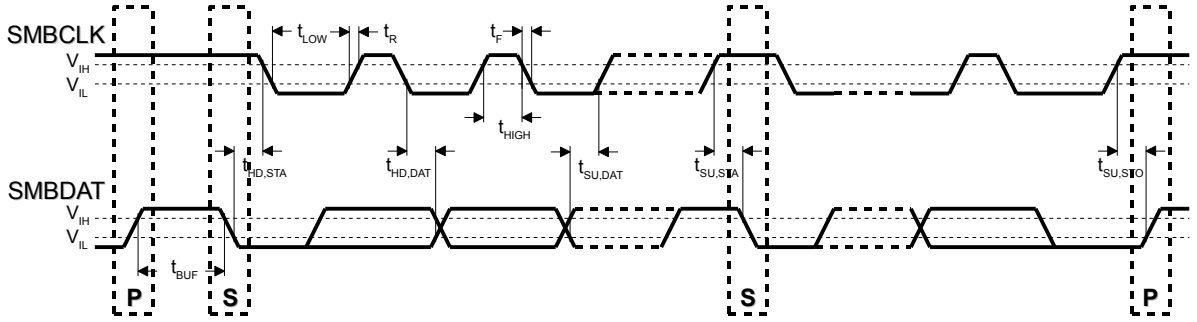
The PSG5410 serial interface is compatible with the SMBus 2.0 specification. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5410 supports 'read byte', 'write byte', and 'block write' as described by the SMBus specification.

5.1 Serial Address

PSG5410 is configured as a slave and has a fixed 7-bit slave address of 1100XX (0x60 – 0x63), configurable through digital input pins SMBADDR0 and SMBADDR1. Tie each SMBADDRx pin to AGND for logic 0 and 5V for logic 1. The following table outlines SMBADDR0/SMBADDR1 pin operation:

SMADDR1	SMADDR0	Serial Address
0	0	0x60
0	1	0x61
1	0	0x62
1	1	0x63

5.2 Timing Diagram

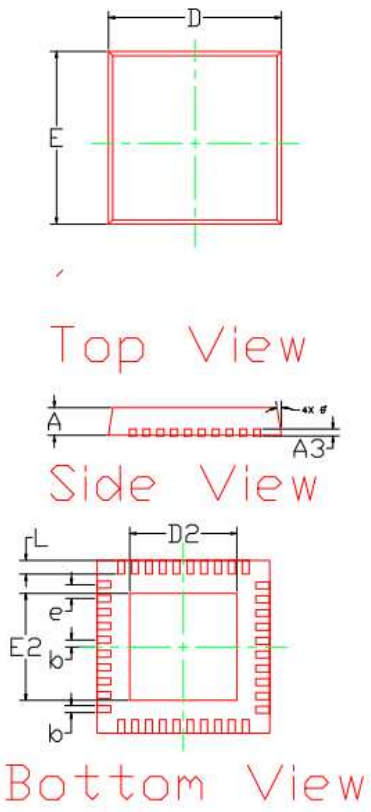


5.3 Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
00H-03H	Reserved								RESERVED	
04H	Reserved							LV Input	ACTCON	0x00
05H-0FH	Reserved								RESERVED	
10H	Reserved				REGEN STAT	PGSTAT	OVP STAT	UVP STAT	VREG1STAT	0x00
11H	Reserved				OCPROG				VREGCON	0x00
12H	Reserved		ODP_STATE		Reserved	PGOOD_ MASK	REG_EN	ODP_EN	ODPCON	0x00
13H	ODP Static Output Voltage								ODPVOUT0	MODE1/MODE0
14H	ODP State 1 Output Voltage								ODPVOUT1	MODE1/MODE0
15H	ODP State 2 Output Voltage								ODPVOUT2	MODE1/MODE0
16H	Reserved								RESERVED	
17H	ODP State 1 Current Threshold								ODPITH1	0x00
18H	ODP State 2 Current Threshold								ODPITH2	0x00
19H	ODP Timeout 0 [7:0]								ODPTOUT0_0	0x00
1AH	ODP Timeout 0 [15:8]								ODPTOUT0_1	0x00
1BH	ODP Timeout 0 [23:16]								ODPTOUT0_2	0x00
1CH	ODP Timeout 1 [7:0]								ODPTOUT1_0	0x00
1DH	ODP Timeout 1 [15:8]								ODPTOUT1_1	0x00
1EH	ODP Timeout 1 [23:16]								ODPTOUT1_2	0x00
1FH	Prescale	ODP Rising Slew Rate 0							ODPSLEWUP0	0x00
20H	Prescale	ODP Rising Slew Rate 1							ODPSLEWUP1	0x00
21H	Prescale	ODP Falling Slew Rate 0							ODPSLEWDOWN0	0xFF
22H	Prescale	ODP Falling Slew Rate 1							ODPSLEWDOWN1	0xFF
23H	PGOOD Blank Time								ODPPGBLANK	0xFF
24H	Reserved						ODP Input Select 1:0		ODPACT	0x08
32H-FFH	Reserved								RESERVED	

Packaging

The PSG5410 is packaged in a 5mmX5mm 40-pin QFN. All dimensions are in millimeters unless otherwise noted.



DIMENSION (mm)				
SYMBOL	MIN	NOM	MAX	TOL.
A		0.800		+/- 0.1
A3		0.200		
b	0.150	0.200	0.250	
D		5.000		
D2	2.950	3.100	3.250	
E		5.000		
E2	2.950	3.100	3.250	
e		0.400		
L	0.300	0.400	0.500	
θ	0 deg.		14 deg.	