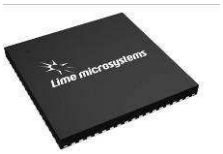
MYRIAD RF



MyriadRF

Development Kit

Rev: 1.0r4
Last modified: 03/05/2013

Contents

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1

Introduction

The Myriad – RF Development Kit is a low cost universal radio development platform, based on flexible, multi standard LMS6002DFN transceiver and Altera FPGA module. It enables developers to implement their products for a wide variety of wireless communication applications efficiently. The main ideas are to:

- Make use of a ready-made design and implementation to accelerate the development time.
- Experiment and evaluate new modulation schemes and wireless systems, operating over a wide frequency range.
- Easily modify and manufacture the platform for new designs using the Open Source database for the complete Kit.

This document provides the following information:

- Detailed description of the hardware platform including setup.
- Software installation, setup and programing of the LMS6002DFN.
- Example files on running of the complete platform including the Altera FPGA module.

2

Development System Contents

Fully operational development system contains Myriad-RF board, Digital interface board (interface board) and DEO – Nano development kit. See Figure 1 Development System below:

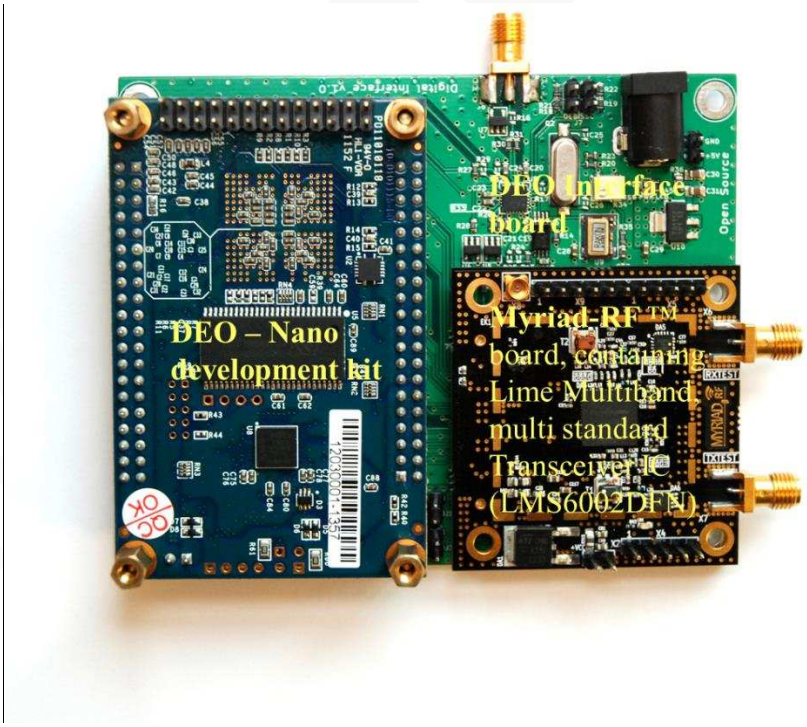
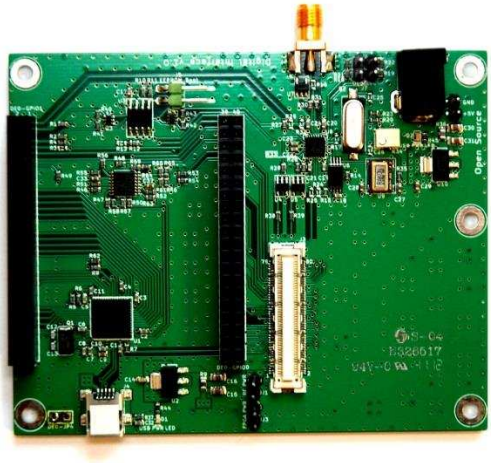
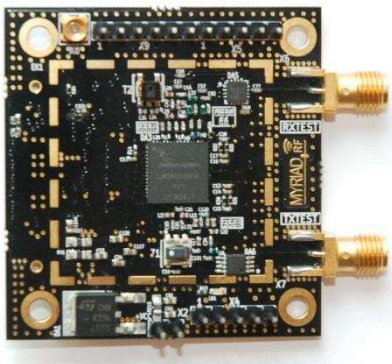


Figure 1 Development System

DEO – Nano
Development Kit



Digital Interface Board



Myriad-RF Board

AC – DC adaptor +5 V

Software

Figure 2 Development System Content

3

Development Kit Connections

3.1 Basic Connections

The Myriad-RF Board can be used as a standalone board or in conjunction with the interface board for a direct connection to the TerAsic DEO – Nano development kit. The Myriad-RF board is connected to the interface board via the standard connector FX10A-80P, connecting digital interface to DEO – Nano development kit. The following sections describe the connections on both boards as well as the overall functionality with the DEO board.

3.2 Myriad-RF Board Connections

The analog differential IQ interface is also available on Myriad-RF board and provided via X3 and X4 connectors, see figure 3. X6 and X7 are the RF connection for receive input and transmitter output on the RF board, see figure 3. The RF board is tuned to support band 1 (Tx 2140 MHz and Rx 1950 MHz) and broadband operation. The front end switches are configurable for selected receiver input and transmitter output via GPIO's. The GPIO's are controlled by FPGA module. The truth table for each selection mode (RX and/or TX) is shown in truth table, section 3.7.

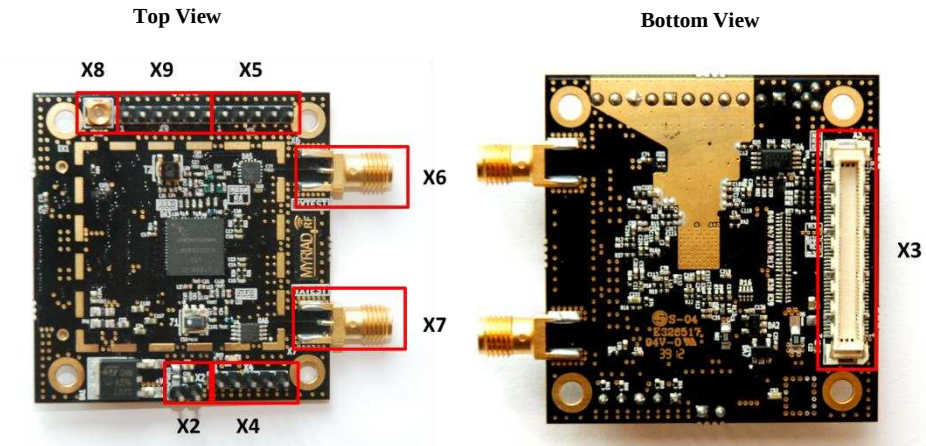


Figure 3 Myriad-RF board connection descriptions.

The following table describes the pin assignment for each connector on the Myriad-RF board.

Connector	Name	Description
X2	+5 V supply	External +5 V supply.
X3	Digital I/O	The FX10A-80P is a standard connector used to interface the RF board directly to interface board or any other baseband board.
X4	TX Analog I/Q	Connector used to supply Transmit analog I/Q signals.
X5	RX Analog I/Q	Connector used to measure Receive analog I/Q signals.
X6	RXTEST	SMA connector provides connection to low band or high band RX input. Requires preselected RF switch configuration.
X7	TXTEST	SMA connector that provides connection to low band or high band TX output. Requires preselected RF switch configuration.
X8	Ext – CLK	Connector used to supply PLL clock externally Please refer to section 3.7 for more information.
X9	Ext – SPI	Connector used to control LMS6002DFN SPI registers externally. SPI register are controlled via X3 connector. Please refer to section 3.6 for more information.

Table 1 Myriad-RF Board Connector Assignments

3.2.1. X2 – +5V Supply Connector

The pin header type connecter used to supply +5 V for Myriad-RF board in standalone mode.

3.2.2. X3 – Digital I/O Connector

The Myriad-RF board X3 connector (type FX10A-80P0) is pin compatible with J1 connector on interface board, see figure 4. It provides the digital and SPI interface for LMS6002DFN together with the supply voltage and GPIO control for RF switches for Myriad-RF board. The pin descriptions on this connector are given in the table below:

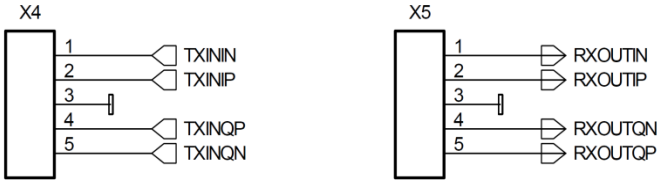
Pin No	Pin Name	Type	Description
1	+5 V	in DC	+5 V power supply
2	+5 V	in DC	+5 V power supply
3	+5 V	in DC	+5 V power supply
4	+5 V	in DC	+5 V power supply
5	GND		Ground pin
6	GND		Ground pin
7	+3.3V	in DC	+3.3 V power supply optional
8	+3.3 V	in DC	+3.3 V power supply optional
9	+3.3V	in DC	+3.3 V power supply optional
10	+3.3V	in DC	+3.3 V power supply optional
11	GND		Ground pin
12	GND		Ground pin
13	-		Not used
14	-		Not used
15	-		Not used
16	-		Not used
17	GND		Ground pin
18	GND		Ground pin
19	TXIQSEL	in cmos	TX digital interface IQ flag
20	-		Not used
21	-		Not used
22	-		Not used
23	TXD0	in cmos	DACs digital input, bit 0 (LSB)
24	TXD1	in cmos	DACs digital input, bit 1
25	TXD2	in cmos	DACs digital input, bit 2
26	TXD3	in cmos	DACs digital input, bit 3
27	GND		Ground pin
28	GND		Ground pin
29	TXD4	in cmos	DACs digital input, bit 4
30	TXD5	in cmos	DACs digital input, bit 5

31	TXD6	in cmos	DACs digital input, bit 6
32	TXD7	in cmos	DACs digital input, bit 7
33	TXD8	in cmos	DACs digital input, bit 8
34	TXD9	in cmos	DACs digital input, bit 9
35	TXD10	in cmos	DACs digital input, bit 10
36	TXD11	in cmos	DACs digital input, bit 11 (MSB)
37	GND		Ground pin
38	GND		Ground pin
39	RXIQSEL	out cmos	RX digital interface IQ flag
40	-		Not used
41	-		Not used
42	-		Not used
43	RXD0	out cmos	ADCs digital output, bit 0 (LSB)
44	RXD1	out cmos	ADCs digital output, bit 1
45	RXD2	out cmos	ADCs digital output, bit 2
46	RXD3	out cmos	ADCs digital output, bit 3
47	GND		Ground pin
48	GND		Ground pin
49	RXD4	out cmos	ADCs digital output, bit 4
50	RXD5	out cmos	ADCs digital output, bit 5
51	RXD6	out cmos	ADCs digital output, bit 6
52	RXD7	out cmos	ADCs digital output, bit 7
53	RXD8	out cmos	ADCs digital output, bit 8
54	RXD9	out cmos	ADCs digital output, bit 9
55	RXD10	out cmos	ADCs digital output, bit 10
56	RXD11	out cmos	ADCs digital output, bit 11 (MSB)
57	GND		Ground pin
58	GND		Ground pin
59	RXCLK	in cmos	RX digital interface clock
60	TXCLK	in cmos	TX digital interface clock
61	-		Not used
62	-		Not used
63	GND		Ground pin
64	GND		Ground pin
65	GPIO0		
66	RESET	in cmos	Hardware reset, active low
67	GPIO1		
68	SPI_MOSI	out cmos	Serial port data out
69	GPIO2		
70	SPI_MISO	in/out cmos	Serial port data in/out
71	-		Not used
72	SPI_CLK	in cmos	Serial port clock, positive edge sensitive

73	GND		Ground pin
74	SPI_NCSO	in cmos	Serial port enable, active low
75	CLK_IN	in cmos	PLL reference clock input
76	-		Not used
77	GND		Ground pin
78	-		Not used
79	TXEN	in cmos	Transmitter enable, active high
80	RXEN	in cmos	Receiver enable, active high
81	GND		Ground pin
82	GND		Ground pin
83	GND		Ground pin
84	GND		Ground pin
85	GND		Ground pin
86	GND		Ground pin
87	GND		Ground pin
88	GND		Ground pin

Table 2 X3 connector pin description

3.2.3. X4 and X5 – Analog IQ Connectors



Pin header type connectors on the Myriad-RF board, provide analog IQ signals I/O.

3.2.4. X6 and X7 – RF Input and Output

The X6 and X7 are SMA type connectors which provide Receive input and Transmit output to the LMS6002DFN, respectively. These are generally used to connect to antenna or test equipment.

3.2.5. X8 – External CLK Connector

The X8 is micro miniature coaxial connector (MMCX8400). It is optional and used to supply external clock in standalone mode.

3.2.6. X9 – External SPI Connector

This is a pin header type connector used for SPI interface to LMS602DFN. This is optional, if the board is used in standalone mode.

3.3 Digial Interface Board Connections

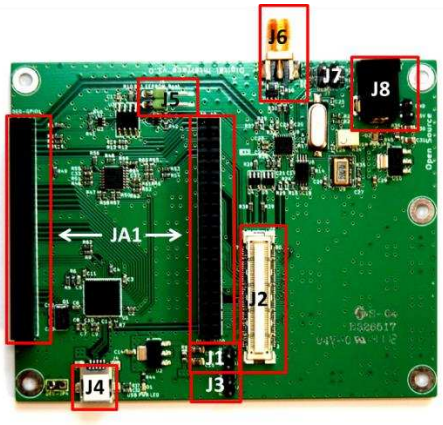


Figure 4 DEO – Interface board connection descriptions.

The following table describes the pin assignment for each connector on the digital interface board.

Connector	Name	Description
J1	RF PWR	Optional +5 V power supply for Myriad-RF board.
J2	Digital I/O	The FX10A-80P is a standard connector used to interface the Myriad-RF board directly to a base band board.
J3	FPGA PWR	Optional +5 V power supply for FPGA Module.
J4	Mini USB	Port used to connect to USB microcontroller.
J5	EEPROM Boot	Enables memory access for USB microcontroller.
J6	CLK output	Used to synchronize measurement equipment. Clock output generated with onboard frequency synthesizer.
J7	Frequency synthesizer Enable	Programmable synthesizer operation control. Enables synthesizer outputs.
J8	Main power supply	+ 5V power supply feed for digital interface board as well and Myriad-RF board. Connector type SPC4077.
J9	Main power supply	+ 5V power supply feed for digital nterface board as well and Myriad-RF board. Connector type 2 way pin header.
JA1	FPGA Module connectors array	The connector array designed to plug DEO - Nano development board on to the DEO Interface Board.

Table 3 Interface board connectors

3.3.1. J1 and J3 - + 5 V power Connectors

The pin header type connectors used as jumpers to supply +5 V for Myriad-RF board and FPGA module. The options are used as shown below:

- Use jumper on J1 if Myriad-RF power from interface board.
- Use jumper on J3 if DEO – Nano Development Kit is supplied from interface board.

3.3.2. J2 – Digital I/O Connector

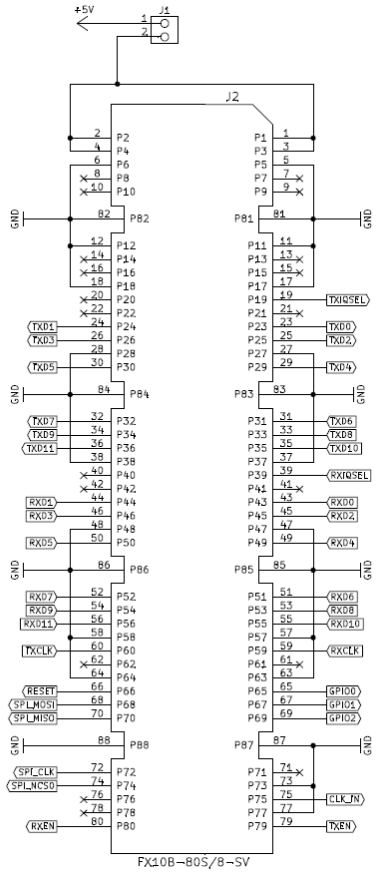


Figure 5 Digital I/O connector

The Myriad-RF board is directly plugged into the J1 connector. The digital I/Q connector is a digital transmit (TX) and receive (RX) interface to the ADC/DAC of the LMS6002D. The SPI interface for LMS6002DFN can also be established via J1 connector.

3.3.3. J4 – Mini USB Connector

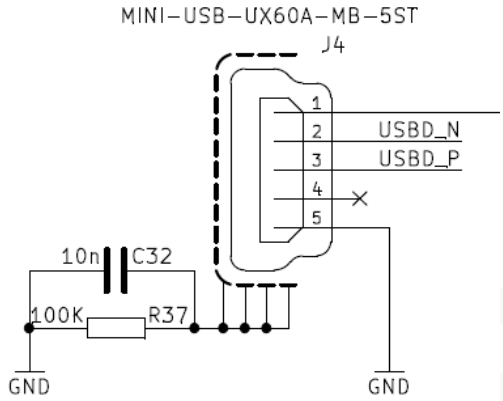


Figure 6 Mini USB conector.

The interface with USB microcontroller and PC is established via mini USB connector. This connector also powers up the microcontroller.

3.3.4. J5 – EEPREOM Boot memory connector

This connector enables USB microcontroller to load the firmware at startup.

3.3.5. J6 – CLK Output Connector

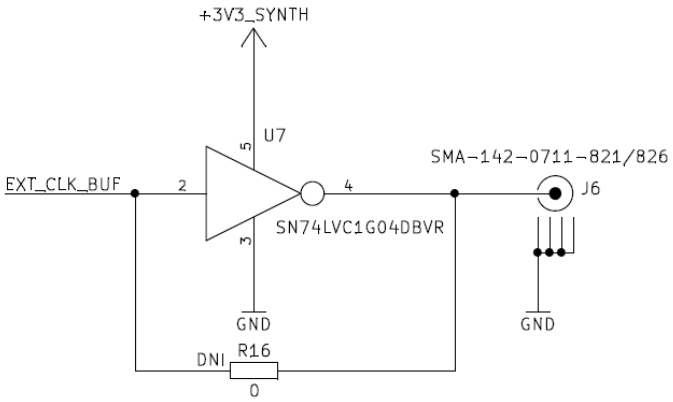


Figure 7 CLK output connector.

J6 is SMA type connector, used to synchronize measurement equipment with development kit.

3.3.6. J7 – Frequency Synthesizer Enable Connector

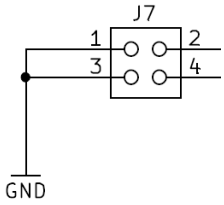


Figure 8 Frequency synthesizer enable connector

This is a pin header type connector. Pin 3 and pin 4 have to be shorted in normal operation, thus enabling frequency synthesizer outputs.

3.3.7. J8 and J9 – Main Power Supply Connector

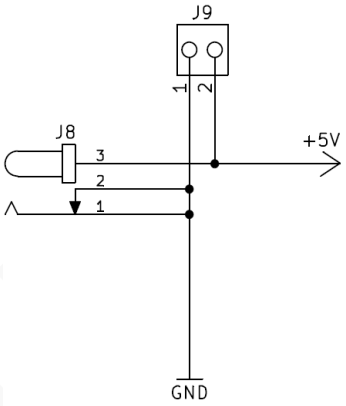


Figure 9 Main power supply connector

The main power supply connector is on interface the board, providing power to both the interface as well as the Myriad-RF board.

3.3.8. JA1 – FPGA Module Connectors Array

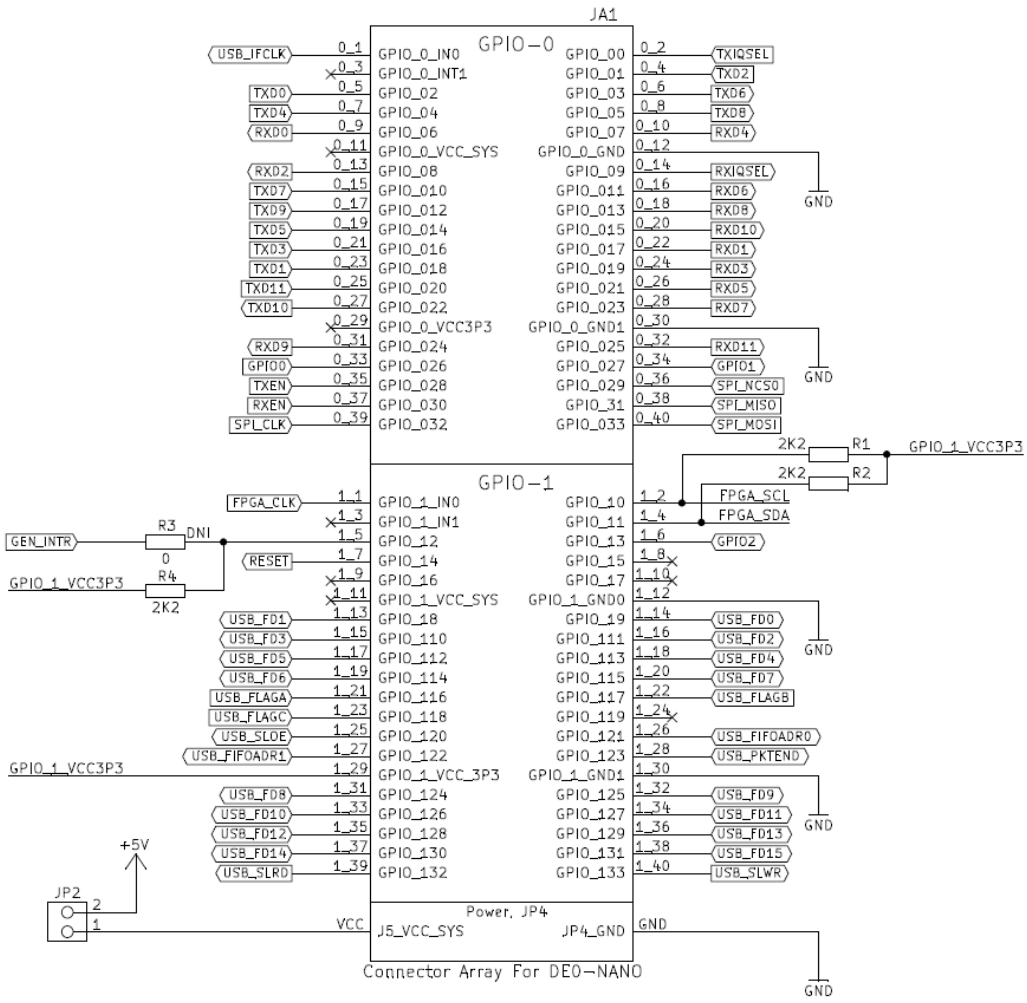


Figure 10 FPGA Module connectors array.

JA1 is a connection array for the DEO – Nano development kit. Physically, there are two separate connectors on the board. This connector establishes the interface between Myriad-RF board digital interface and FPGA module with the PC.

3.4 Hardware options: Clocking, SPI, GPIO truth table & Standalone.

This section describes the configurations and set up procedures for:

- Reference frequency and data clocks distribution (Section 3.6).
- GPIO control truth table (Section 3.7).
- Standalone mode (Section 3.8).

The board is shipped in a default mode for basic operation. Various options are available depending on the system configuration required for testing or development work. The options are summarized below and the following sections describe the board modifications required to achieve these configurations.

3.5 Reference Frequency and Data Clocks Distribution

The LMS6002D device provides a flexible clocking scheme which enables the PLL clock, RX clock and TX clock to be independently set.

The development kit is shipped with a default mode using the on board 30.72MHz clock for PLL clock only. The board can be reconfigured to allow users to provide clock frequency for digital interface and PLL clock using programmable clock generator from Silicon Labs (Si5356) which is capable of synthesizing four independent frequencies. The device has four outputs connected to LMS6002DFN PLL clock, RX data interface clock, TX data interface clock and to the J6 connector.

In order to reprogram the frequency from the default setting of 30.72 MHz, please use component change as given in the table below. Please note that NF denotes that component is not fitted:

Reference clock options		
Description / Component	**Default mode. PLL clock set to 30.72 MHz**	**Programmable mode. PLL clock can be reprogramed.**
R15	0 Ohm	NF
R24	NF	0 Ohm

Table 4 Reference clock configurations

More information how to progra Frequency synthesizer in 4.5.11 cahpter.

3.6 SPI Options

Interface board offer two option for the SPI communication with Myriad RF board:

1. SPI communication established via FPGA (and via interface board USB microcontroller).
2. SPI communication established via USB microcontroller.

In order to make sure stable SPI communication for desired option, the component change on interface board is given in a table below. Please note that NF denotes that component is not fitted:

SPI Options		
Components	**SPI via FPGA**	**SPI via USB controller**
R48	NF	0 Ohm
R58	NF	0 Ohm
R51	NF	0 Ohm
R46	NF	0 Ohm
R52	NF	0 Ohm

Table 5 SPI options

Note: When SPI communication is selected via USB microcontroller the FPGA lines SPI_NCSO, SPI_MISO, SPI_MOSI, SPI_CLK have to be set to tri-state.

Note: When SPI via FPGA option is selected the Cypress microcontroller has to be programed using firmware version 6 (firmware_v1r06). When SPI via USB microcontroller ption is selected the Cypress microcontroller has to be programed using firmware version 7 (firmware_v1r08). More information how to program Cypress chip in chapter "4.2 Firmware installation for USB microcontroller"

3.7 GPIO control truth table

The RF switches on the RF board are controlled via the GPIO 0-2 logic signals, provided by the FPGA module on the interface board. This enables the user to choose RF input/output depending on the operation frequency. The truth table of the GPIO 0-2 settings is shown below.

LMS6002D RF Input/output	**GPIO 0**	**GPIO 1**	**GPIO 2**	**Description**
TX out 1	X	X	0	High band output (1500 – 3800 MHz)
TX out 2	X	X	1	Broadband output
Rx in 1	1	1	X	Low band input (300 – 2200 MHz)
Rx in 2	0	1	X	High band input (1500-3800MHz)

Rx in 3	0	0	X	Broadband input

Table 6 GPIO truth table

Note: LMS6002D RF input/output have to be selected/programed with SPI registers. This is done using GUI software.

3.8 Standalone Mode

The Myriad-RF board can operate in standalone mode. Setup for standalone mode is as follows:

- Connect +5 V power supply to X2 connector on the Myriad-RF board.
- Connect SPI control to X9 connector.
- Connect wanted reference clock to X8 connector. Fit R49 resistor.

In this mode you are able to fully control LMS6002DFN chip register and perform some basic RF measurements using IQ Analog inputs/outputs.

4

Installing and Running the PC Software Application

4.1 Windows USB driver installations

Before plugging USB cable to mini USB port on the interface board:

1. Download the software package from Myriad website [download].
2. Log in as Administrator to your Windows machine for the free USB port.

Plug the USB cable to mini USB port on the interface board. Driver installation window will pop-up. After installation procedure begins, exit/cancel Windows search! Select to install drivers manually.

Figure 11 Hardware wizard.

Next, chose to install driver from specific location.

Figure 12 Hardware wizard. Install driver manually

Select to install drivers manually and point to the driver which can be found in the **cyusb_driver** folder. Please choose the driver suitable for your operating system:

- Windows 2000(w2K)
- Windows XP (wxp)
- Windows Vista (wlh)
- Windows 7 (wlh)

CPU type:

- x86(32bit-i386)
- x64(64bit-amd64)

Use the browse function to find this file.

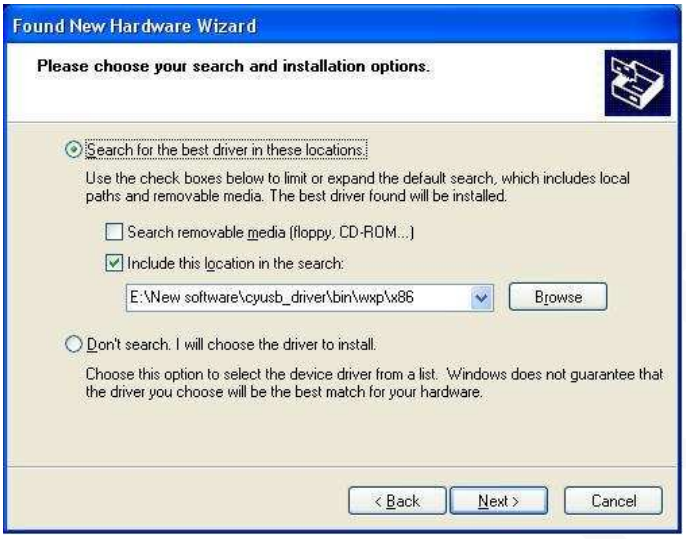


Figure 13 Hardware wizard. Choose the required from the folder

Windows should proceed to install drivers. If everything is successful unplug and then plug in your device again to be able to use it.

Note: if the windows warning window appears, select *"Continue Anyway"*. See picture below.

Figure 14 Hardware installation warning window

4.2 Firmware installation for USB microcontroller

To be able to install firmware to USB microcontroller, please download and install Cypress software "CySuiteUSB_3_4_7_B204.exe" from cypress site [download].

Cypress's FX2LP USB microcontroller has an integrated bootloader, which starts automatically after power-up or reset.

If EEPROM (U3 on interface board) is empty or connector J5 (on interface board) is open, FX2LP boots-up with default (factory) USB firmware with USB descriptors and VID/PID supplied by hardwired internal logic. If you run "USB Control Center" application and expand "Cypress USB Generic Driver (3.4.7.000)" line, you will see 4 Alternate Settings, as shown in Figure 15.

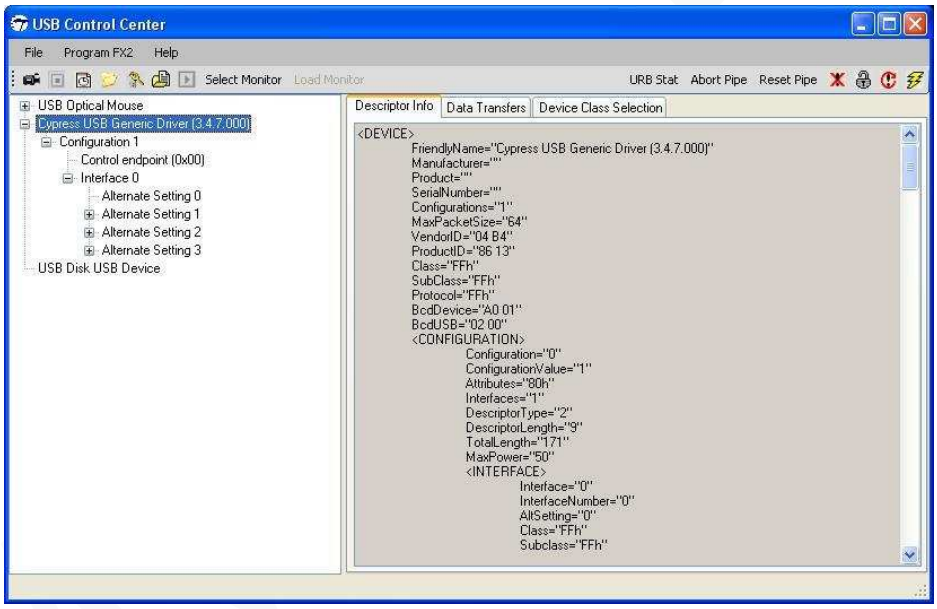


Figure 15 Default FX2LP firmware, supplied by internal logic

To be able to control Myriad board, the USB microcontroller has to be programed with appropriate firmware. It is possible to download firmware to the FX2LP's RAM or onboard EEPROM. If firmware is downloaded to the RAM, it will not be available after power-off and power-on. If the firmware is downloaded to the EEPROM, FX2LP will boot from EEPROM after power-on.

4.2.1. Downloading firmware to the FX2LP's RAM

Start "USB Control Center" application and select "Cypress USB Generic Driver (3.4.7.000)" line, as shown in Figure 15. Choose menu command "Program FX2 -> RAM". Window will appear. Select hex file provided (firmware_v1r06.hex) and press "Open". Status bar of the USB Control Center" application will indicate "Programming RAM of LM Cypress USB Generic Driver (3.4.7.000) device". This message will change to the "Programming succeeded" after programming is done.

If you expand "Cypress USB Generic Driver (3.4.7.000)" line in "USB Control Center" application now, you will see different FX2LP configuration as shown in Figure 16.

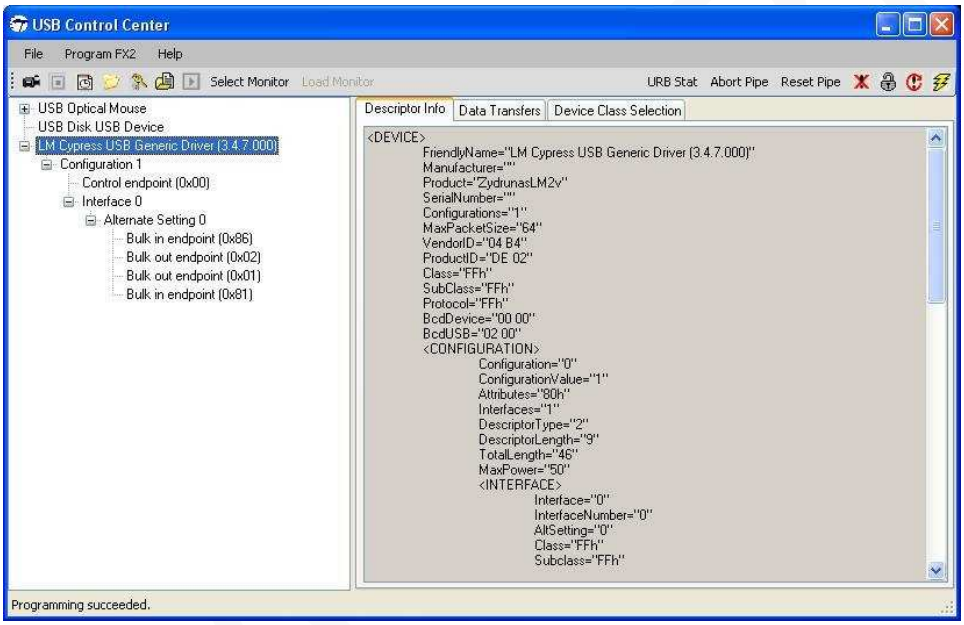


Figure 16 FX2LP after custom firmware is downloaded

Note please, that firmware, downloaded using this method, will be not available after power-off and power-on.

Note: After downloading firmware, you may need to install the USB drivers again. Please follow the chapter "5.1 Windows USB driver installations"

4.2.2. Downloading firmware to the empty EEPROM

If on-board EEPROM is empty, make sure that jumper J5 is shorted, connect carry board to the PC's USB port and then run "USB Control Center" application. Default configuration must be loaded, as described in chapter "**Error! Reference source not found.**".

Choose menu command "Program FX2 -> 64kB EEPROM". Window will appear. Select iic file provided (firmware_v1r06.iic) and press "Open". Status bar of the USB Control Center" application will indicate "Programming EEPROM of Cypress USB Generic Driver (3.4.7.000) device". This message will change to the "Programming succeeded" after EEPROM programming is done.

Note: that FX2LP will boot firmware, downloaded to the EEPROM each time after power-on if jumper J5 is shorted.

Note: that FX2LP will boot the firmware, just downloaded to the EEPROM after next power-up.

4.2.3. Downloading firmware to the not empty EEPROM

If it is necessary to reprogram EEPROM with new firmware, do these steps:

1. Disconnect Myriad board from USB port.
2. Make sure, that jumper J5 is open.
3. Connect Myriad board to USB port.
4. Short jumper J5.
5. Do the steps described in chapter "Downloading firmware to the empty EEPROM".

4.3 FPGA Programming over Embedded USB – Blaster

To be able to control Myriad RF SPI line via DEO – Nano board, the FPGA have to p[programed.

4.3.1. FPGA software Installation procedure

The Quartus II Programmer can be used to configure the DEO – Nano on board FPGA with a specific demo_txcw.sof file. Before configuring FPGA, please ensure that the Quartus II Programmer and the USB – Blaster driver are installed on the host computer. USB cable must be connected to the FPGA development board, the board is powered ON and there are no other applications running that uses JTAG chain. In order to configure the Cyclone IV FPGA please perform the following steps:

- Start the Quartus II Programmer.
- Click Add File and select the path to the desired .sof.
- Turn on the Program/Configure option for the added file.
- Click Start to download the selected file on to the FPGA. Configuration is complete when the progress bar reaches 100%.

The window view of the Quartus II Programmer is shown in Figure 11. This view indicates successful configuration of FPGA.

After Quartus II Programmer is started please ensure that there is "USB-Blaster [USB-0]" line at the right of "Hardware Setup…" button. If the line indicates "No Hardware" instead, press "Hardware Setup…" button. Select "USB-Blaster [USB-0]" from the "Currently selected hardware:" drop-down list. If the drop-down list does not contain USB-Blaster, make sure you have connection between the PC and the board; Note that the driver has been installed.

It is necessary to check if "Mode:" is set to "JTAG" in the Quartus II Programmer window. Choose JTAG, if any another mode is selected.

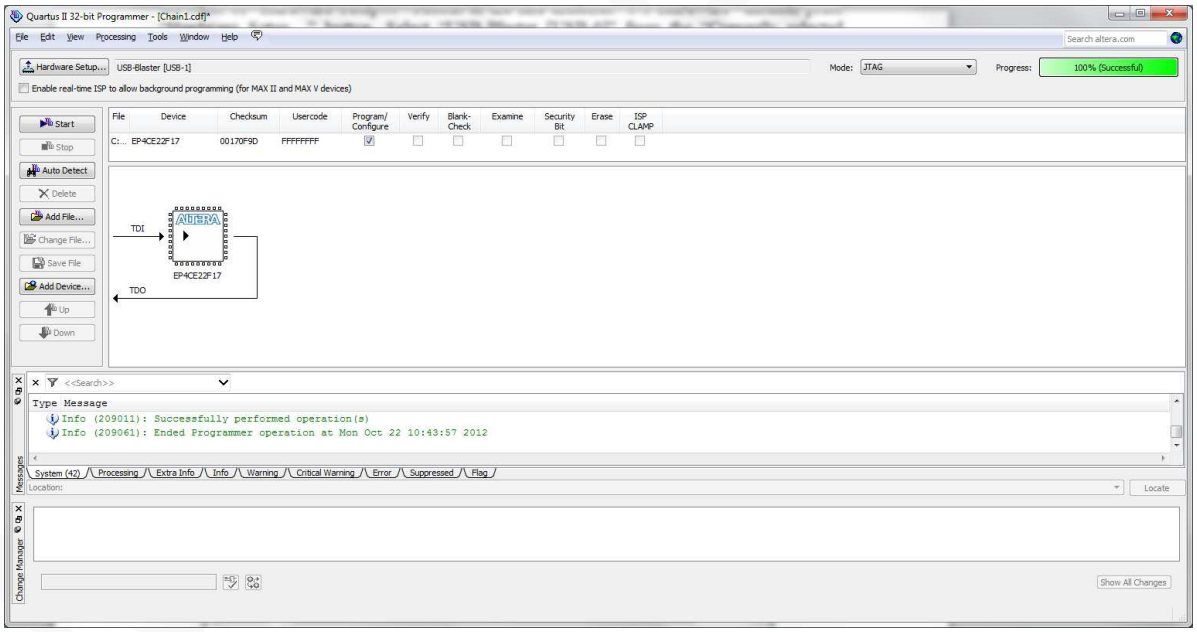


Figure 17 View of the Quartus II Programmer

Note: When, SPI via FPGA option is selected, the FPGA has to be programed using demo_txcw.sof gateware version. When SPI via USB microcontroller option is selected the FPGA has to be programed using myriadRF_NCO_noSPI.sof gatware version.

4.3.2. Software Functionality

Programed FPGA enables user to:

1. Control LMS6002DFN chip registers with crt_6002dr2 graphical user interface software via mini USB connector J4 (if demo_txcw.sof gatware version is selected).
2. Set up the Myriad board RF switches.
3. Verify the interconnection between Myriad RF board and DEO – Nano board generating the CW with implemented 4 values Numerically Controlled Oscillator (NCO). The frequency of wanted CW is equal $f_{cw} = FPGA\_CLK / 8$.
4. Connect Myriad RF digital interface pins for further implementation.

4.4 Turn On and SPI Check

Turn on the +5V power supply to the board. Start Myriad RF control S/W, provided in folder **software**. The SPI APP – picture of ICON is shown below.

Note: For Window 7 operating system, right click on the "ctr_6002dr2.exe" icon above. Next, click on Properties and click on the "Compatibility.

Select "Run this program as an administrator". This will provide administrator privileges which is required for LMS6002 communication via USB.

Go to menu "Options->Communication Settings". The following window appears.

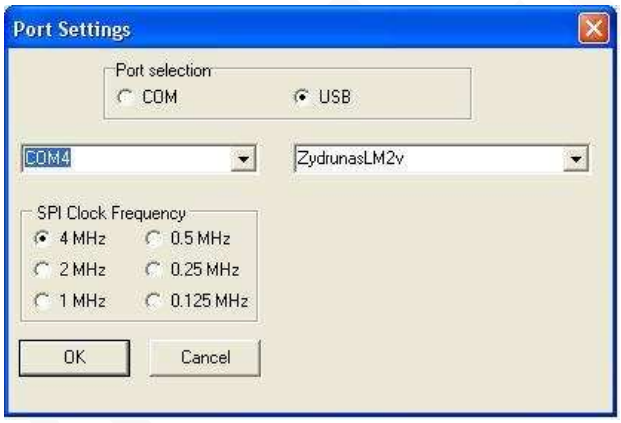


Figure 18 GUI communication settings.

Select USB in port selection, select desired SPI clock frequency and push OK. Now you are able to communicate with the LMS6002D test board using USB to Serial adapter.

To check this is working select the register test sequence by going to menu "Tools->Register Test".

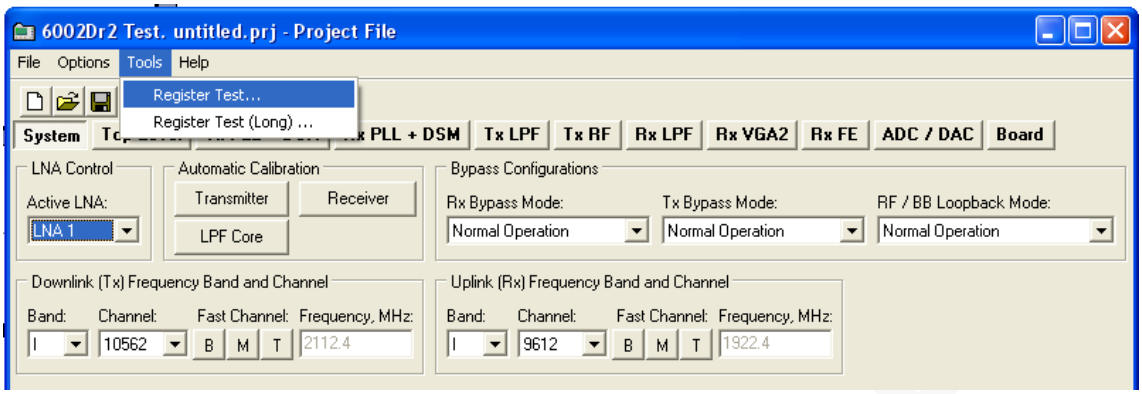
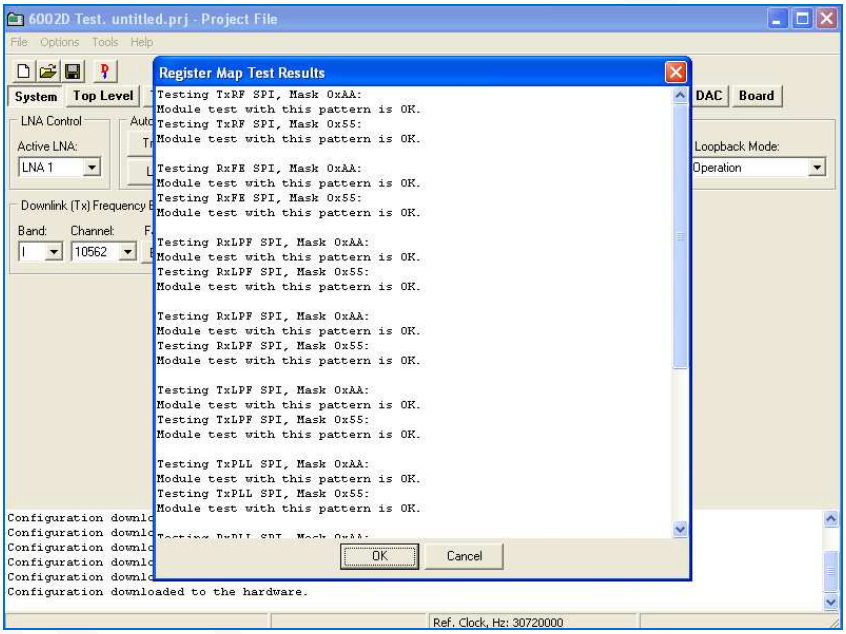


Figure 19 GUI register test.

The system will then return a full registers indicating OK for correct operation as shown below.



.

Figure 20 GUI register test log.

If the system returns OK message you are now ready to commence testing. If the system returns 00 or FF instead of the OK this means there is a communication problem with the LMS6002D.

If the system returns 00 then there is a problem with the connection between the PC and the design kit USB port. You will need to check connection and start the process again.

If the system test returns FF then you know the PC and the USB port are communicating properly. Connect the Myriad-RF board to +5V supply and start the process again. If you now

get an OK for the register test map results then the system is ready for testing. If the system still returns 00 or FF instead of an OK, reboot entire connected system.

Note: When you close the software, the selected communication port and all of the associated settings will be saved under a file with *.CPS extension. Next time you run the software all the settings will be loaded automatically.

4.5 Ctr6002dr2 – Software Description

This section describes the ctr6002dr2 software tool and each of the buttons and embedded controls. Most of the pages in the tool can be read across to the top level sections of the SPI programming map, with the exception of the 'System page' and the 'Board' page.

4.5.1. System Interface

The System interface page allows configuring the synthesizers to the 3GPP bands by channel number and has buttons for bottom, middle and top frequencies for each. This makes changing frequency for the commonly used test channels simpler.

Automatic calibration (the calibrationsthat the device carries out itself under SPI prompt) is also done from this page.

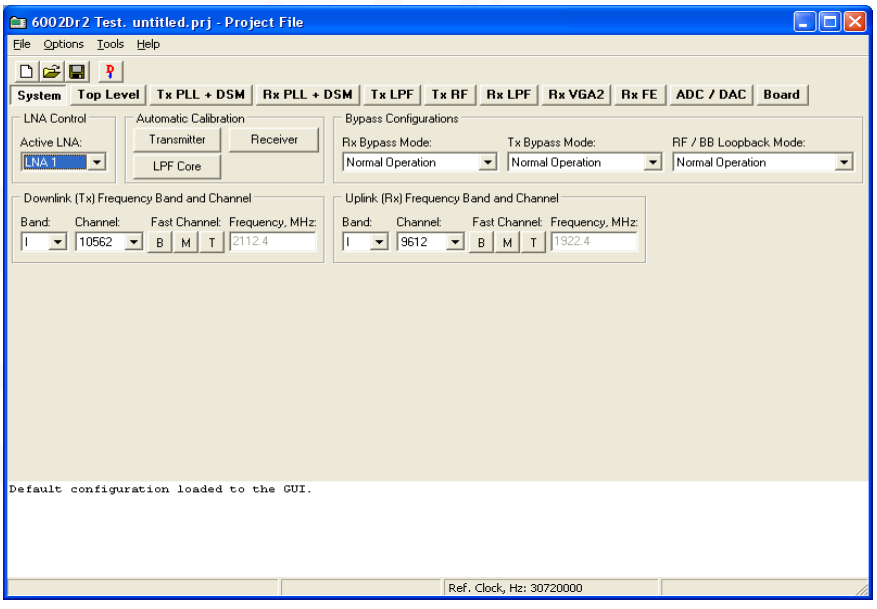


Figure 21 GUI System window.

Downlink and Uplink Frequency setting by band/channel number.

The synthesizers can be configured by channel number to the correct frequency in each 3GPP band. Buttons are provided for bottom, middle and top frequencies for each band. This makes changing frequency for the commonly used test channels easier.

Bypass configurations

The various bypass test modes and loop back test modes can be implemented by selecting from the drop down boxes, default is Normal operation.

Automatic Calibration

The Automatic calibration buttons can be used to run through the series of SPI commands required to implement the various self-calibration routines provided on the chip. Use of these macros is implemented as part of a calibration procedure and each button does not carry out a full calibration, use of the buttons in the wrong context could make the calibration state worse rather than better.

Automatic calibration should be done in the following order:

a. LPF Core – Press LPF core button

Executes the process related resistor capacitor (RC) calibration. LPF Core calibration is performed once per device to ensure that the corner frequencies of the LPFs are optimized. The calibration selects the LPF response which is closest and above the required bandwidth. This ensures modulation quality is not adversely impacted but sufficient rejection is provided for adjacent and alternate channel attenuation.

This should be done 1st as optimum DC calibration values for LPF's will change if this is done after the filter DC calibration.

b. Transmitter

The transmitter calibration executes a DC calibration on the TX LPF (I and Q) circuit. This makes the DC contribution at output of filters zero so that DC level at the mixer input does not change when the TX VGA1 gain is changed.

When executing this calibration make sure that no signal is applied to the transmit path. For better DC calibration low DC level signal can applied from baseband via DAC's to transmit path.

c. Receiver

Executes a DC calibration on the Rx LPF (I and Q), and Rx VGA2 (I and Q). This minimizes the DC contribution at output of filters and Rx VGA2.
When executing this calibration make sure that there is no signal applied to Rx input.

4.5.2. Top level

Various loop back and calibrations are also controlled on this page. They are not needed for basic operation. Automatic calibrations should all be done from the 'System' page where macros have been written to apply the calibration routines automatically.

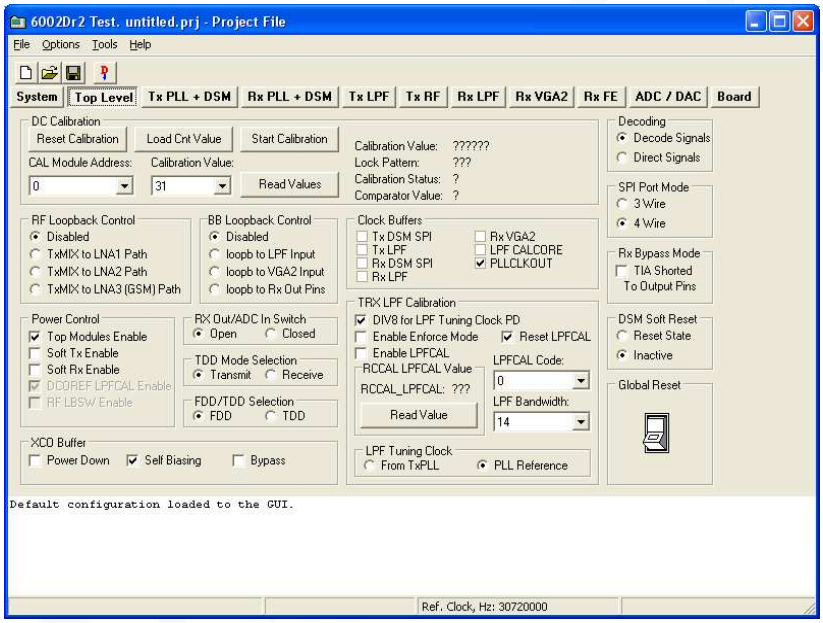


Figure 22 GUI Top Level window

Description of each function available from this page is as follows:

DC Calibration

Carries out the top level DC calibration for the device, this is the R component of the RC cal value which is used in each of the LPF (Tx and Rx) process calibration values. Only calibration module address 0 is used.

.

Clock Buffers control
Enable pins turn the internal clock buffers on and off. These should be enabled when control of the device is needed, however during operation SPI clocks which are not being used should be disabled to reduce the risk of SPI clock spurious.

RF Loopback Control
Test mode. RF loopback control sets the path used for the loopback from Tx to Rx input. Please refer to the SPI programming and calibration document for further details.

BB Loopback Control
Test modes, sets the BB loopback from Tx to Rx input.

Power Control
Soft turn off of Tx and Rx top level blocks of the LMS6002D via SPI. The LMS6002D communication can be easily checked by toggling the "Soft Tx Enable" and "Soft Rx Enable" in the Power Control section. The current change can be observed on power supply.

TRX LPF Calibration
This section is used to calibrate the capacitance of the device to ensure the LPF BW's are correct. To execute the calibration, check then uncheck the reset LPFCAL box (to reset calibration module). Then, check and uncheck the Enable LPFCAL box to execute the calibration. The result can be found in the DC calibration area when the read button is pressed.

Enable Enforce Mode and LPFCAL Code are not used. LPF BW sets the bandwidth used for the calibration. If you are using WCDMA select 2.5MHz. The result should be copied into the TXLPF and RXLPF from 'TRX_LPF_CAL' drop down box.

Decoding
Select 'Decode Signals' or 'Direct Signals' for control of different parts of the SPI memory map. Use 'Decode Signals'.

SPI Port Mode
Selects 3 or 4 wire SPI mode. 4 wire mode is used with the USB board solution.

Rx Bypass Mode
Not used.

DSM Soft Reset
Keep on inactive.

Global Reset
Toggles the reset pin via the USB SPI interface. The LMS6002D should be reset after power up to put it in a known state.

Rx Out/ADC In Switch
Select Closed to monitor receiver analog input. Select Open to route external signal to ADC.

4.5.3. TX PLL + DSM

The Tx PLL is controlled from this page. If the frequency control on the 'System Interface' page is used and the correct 'set up files' have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled:

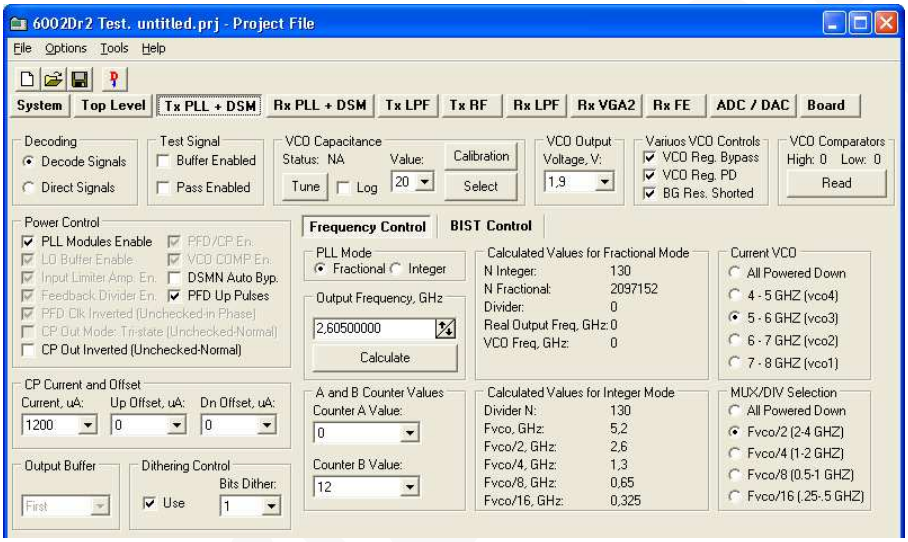


Figure 23 GUI TxPLL + DSM window

Description of each function available from this page is as follows:

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Dithering Control
DSM dithering. Leave it set to 1.

Power Control
Individual parts of the PLL circuitry can be turned on and off – leave as default.

Test Signal
Design test signals – leave unchecked.

VCO Comparators
Reads the state of the VCO Comparators. Truth table is:

VTUNE_H	VTUNE_L	Status
0	0	ok
1	0	Vtune is high (> 2.5V) PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V) PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

Table 7 Comparator readings

Output Buffer
Control not used in TxPLL.

Frequency Control
Sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below:

PLL Mode – selects fractional or integer mode. Use fractional mode.

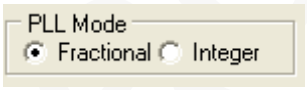


Figure 24 PLL mode.

Output Frequency (GHz) - set the desired Tx LO frequency in the text box.
'Calculate' button – calculates the required divide ratio based on the required LO frequency and reference frequency.

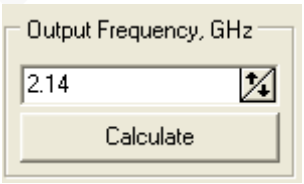


Figure 25 Output Frequency – GHz

These are shown in **'Calculated Values for Fractional Mode'** display box.

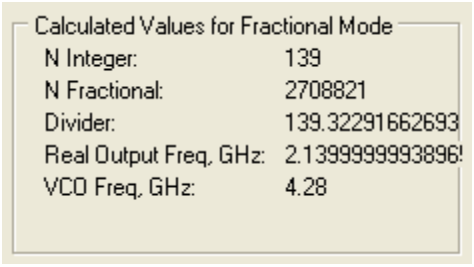


Figure 26 Calculated Values for Fractional Mode

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

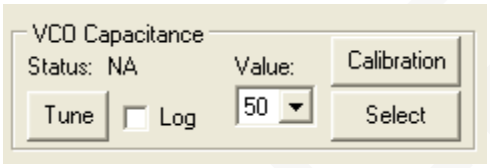


Figure 27 VCO Capacitance

The '**Current VCO**' and the '**MUX/DIV Selection**' show the choice made by pressing **"Calculate"** or **"Tune"** buttons, see below.

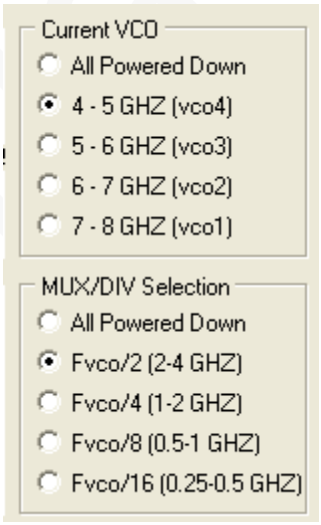


Figure 28 Current VCO and MUX/DIV selections

VCO Capacitance

Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide**.** Selections made when using the **'Calculate'** button however are decided based on the calibration table used in this block.

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

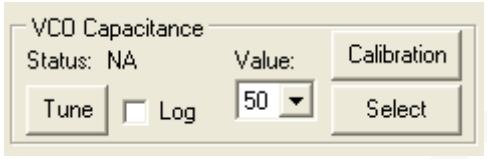


Figure 29 VCO Capacitance

Use of the **'Calibration'** button is described at the end of this section.

Charge Pump(CP) Current and Offset

Figure 30 CP Current and Offset

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the design kit) Current should be 1200uA and Up Offset 30uA, as shown.

PLL Calibration Data and File

Press the 'Calibration' button to enter the Frequency vs Capacitance calibration table data.

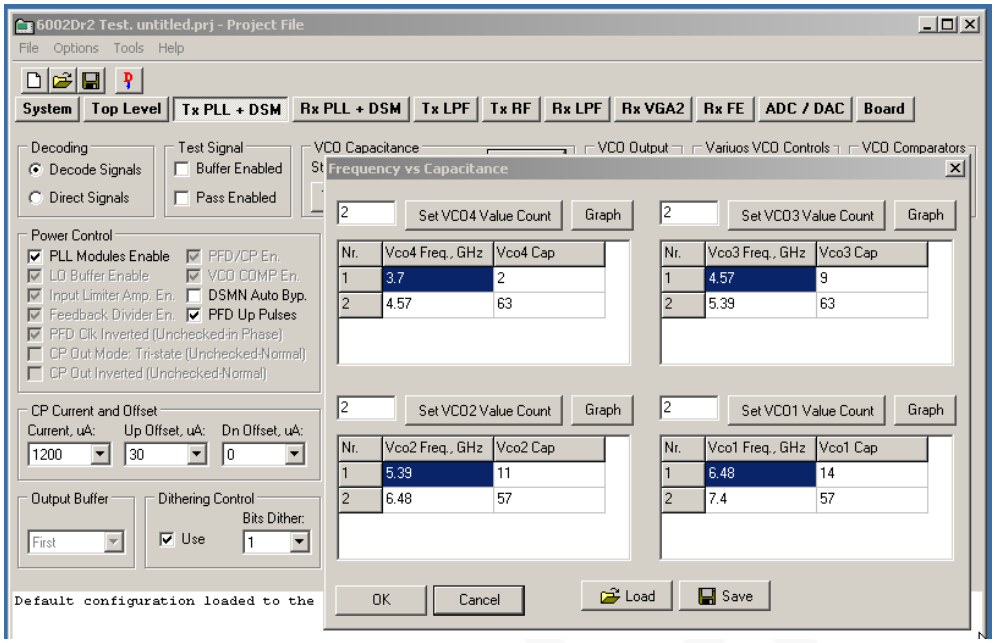


Figure 31 Frequency versus capacitance calibration table data

The calibration data consists of frequency versus capacitance value responses which are defined by minimum 2 point definition. The loaded VCO file should contain the above data. If not file 'Dr2.vco', provided with SW, should be loaded. To load a new VCO file press the 'Load' button and follow the normal windows procedure to load a file. Then press OK. This new file will now be downloaded on subsequent starts of the software.

4.5.4. Rx PLL + DSM

The Rx PLL is controlled from this page, if the frequency control on the 'System Interface' page is used and the correct 'set up files' have been automatically downloaded, then this page should not be needed. However a few points to check are that the tick boxes shown in the diagram below are enabled.

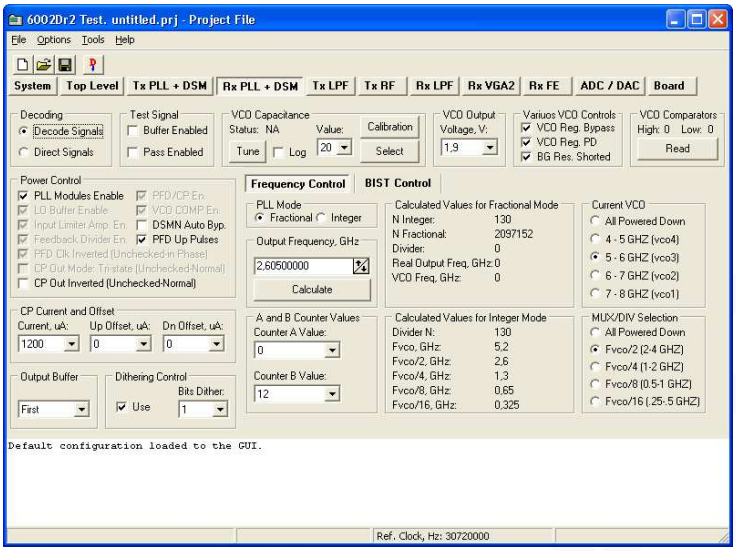


Figure 32 RX PLL + DSM page

Description of each function available from this page is as follows:

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Dithering Control

DSM dithering. Leave it set to 1.

Power Control

Individual parts of the PLL circuitry can be turned on and off – leave as default.

Test Signal

Design test signals – leave unchecked.

VCO Comparators

Reads the state of the VCO Comparators. Truth table is:

VTUNE_H	VTUNE_L	Status
0	0	ok
1	0	Vtune is high (> 2.5V), PLL lock not guaranteed.
0	1	Vtune is Low (< 0.5V), PLL lock not guaranteed.
1	1	Not possible, check SPI connections.

Table 8 Comparator readings

Output Buffer
Sets the correct PLL output buffer for the selected LNA:
LNA 1 = First
LNA 2 = Second
LNA 3 = Third and
Disable.

Selection of LNA in tool on 'System' page automatically selects the correct buffer.

Frequency Control
Sets the PLL divide ratios, VCO and output divider selection. The individual parts of this block are described in more detail below.

PLL Mode – selects fractional or integer mode. Use fractional mode.

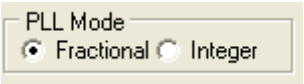


Figure 33 PLL Mode

Output Frequency (GHz) - set the desired Tx LO frequency in the text box.
'Calculate' button – calculates the required divide ratio based on the required LO frequency and reference frequency.

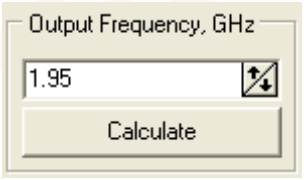


Figure 34 Setting receiver frequency - GHz

These are shown in **'Calculated Values for Fractional Mode'** display box

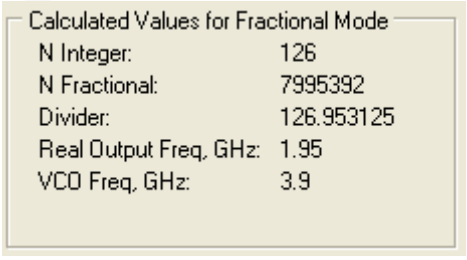


Figure 35 Calculated values for fractional mode

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

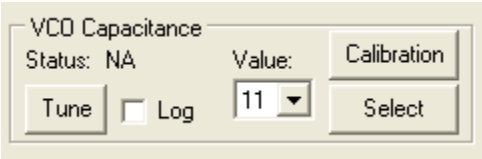


Figure 36 VCO Capacitance

The '**Current VCO**' and the '**MUX/DIV Selection**' show the choice made by pressing **"Calculate"** or **"Tune"** buttons, see below.

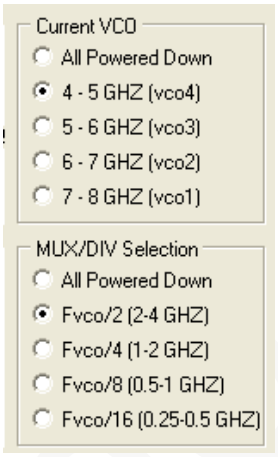


Figure 37 Current VCO and MUX/DIV selections

VCO Capacitance

Correct setting of VCO capacitance is described in LMS6002D Programming and Calibration Guide**.** Selections made when using the **'Calculate'** button however are decided based on the calibration table used in this block.

To properly select the **'VCO Capacitance'** click "**Tune**" after **"Calculate"**. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

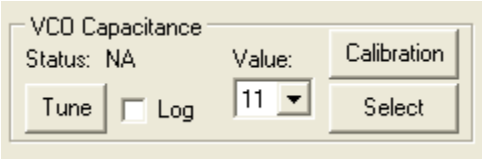


Figure 38 VCO Capacitance

Use of the **'Calibration'** button is described at the end of this section.

Charge Pump(CP) Current and Offset

CP Current and Offset is set based on the selected loop filter and loop BW. For the recommended loop filter (implemented on the design kit). Current should be 1200uA and Up Offset 30uA, as shown.

Figure 39 CP Current and Offset

PLL Calibration Data and File

Press the **'Calibration'** button to enter the Frequency vs Capacitance calibration table data.

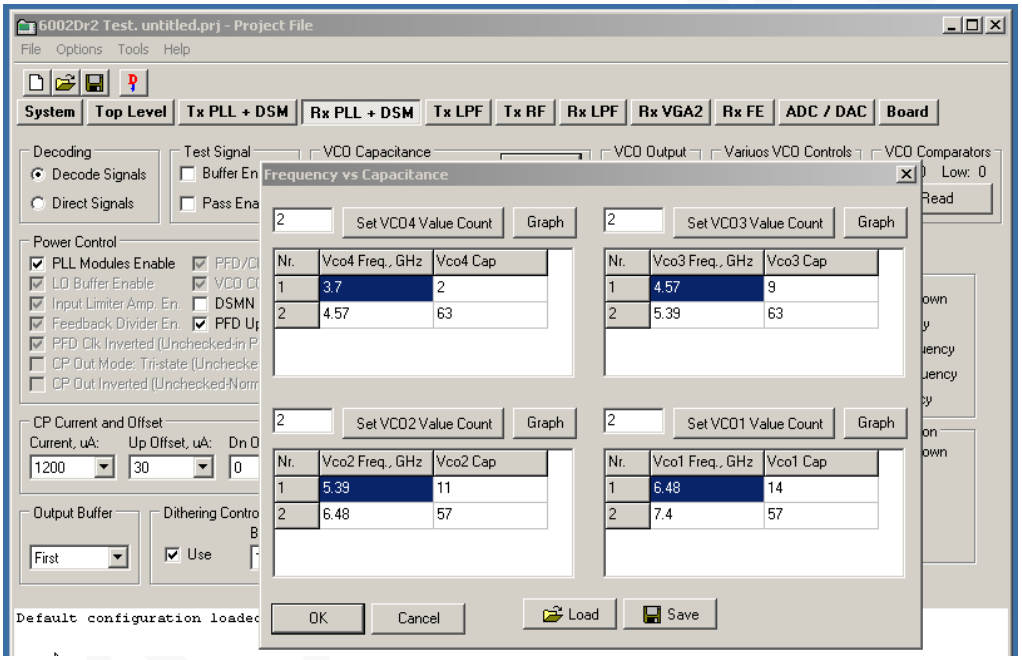


Figure 40 Frequency vs capacitance calibration table data

The calibration data consists of frequency versus capacitance value responses which are defined by minimum 2 point definition. The loaded VCO file should contain the above data. If not file 'Dr2.vco', provided with SW, should be loaded. To load a new VCO file press the 'Load' button and follow the normal windows procedure to load a file. Then press OK. This new file will now be downloaded on subsequent starts of the software.

4.5.5. Tx LPF

The Tx LPF page contains the SPI controls for the transmitter low pass filters, notably the LPF BW and also the controls for the DC calibration.

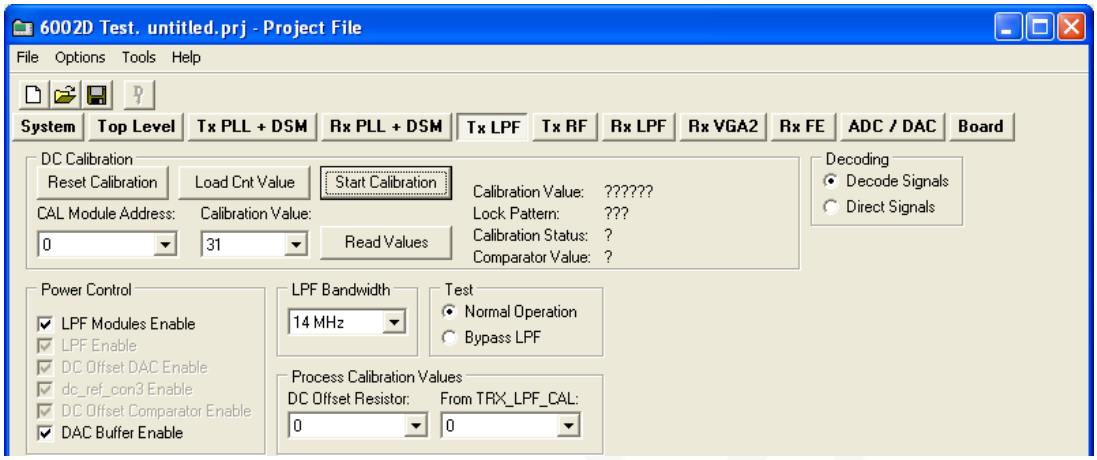


Figure 41 Tx LPF page

Description of each function available from this page is as follows:

DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the TX LPF (controlled by the 'Transmitter' auto-calibration button on the 'System' page).

The Tx LPF DC calibration has 2 stages which can be calibrated:

- TXLPF(I) at Cal module address 0
- TXLPF(Q) at Cal module address 1

Power Control

Powers down the LPF modules, grayed out controls can be accessed by using direct signals mode.

LPF Bandwidth

Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

Test

Enables LPF bypass for test purposes. Ensure 'Normal Operation' is enabled.

Process Calibration Values

RC calibration values used to process trim the LPF BW. Values are calculated in top level calibration and written into these locations (carried out automatically by 'LPF Core' on 'System' page).

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones are grayed out). 'Decode' mode is recommended.

4.5.6. Tx RF

The TX RF page contains the SPI controls for the TX RF stages, including all Tx gain control, LO correction and Tx output selection.

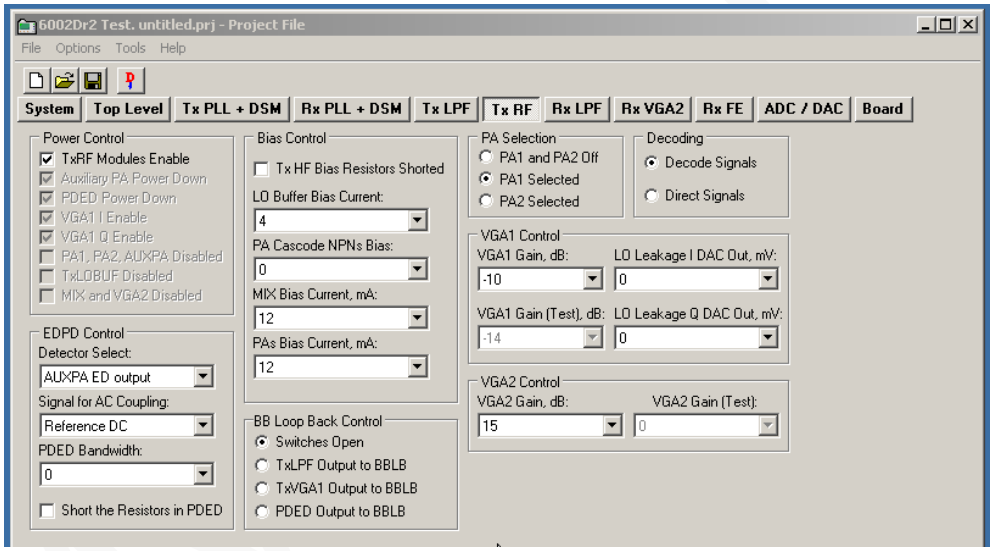


Figure 42 Tx RF page

Description of each function available from this page is as follows:

Power Control

Powers down stages within the Tx RF block – grayed out controls are accessible via 'Direct' decoding mode.

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out). 'Decode' mode is recommended.

VGA1 Control
VGA1 Gain sets VGA1 gain (IF gain stage) from -4 to -36dB via drop down box. VGA1 Gain (Test) sets VGA1 gain in 'Direct Signals' mode by setting 8 bit not log-linear control word directly. 'LO Leakage I DAC Out' and 'LO Leakage Q DAC Out' set DC level injected via the LO correction DACs for LO cancellation.

VGA2 Control
VGA2 Gain sets VGA2 gain (RF gain stage) from 0 to 25dB via drop down box. VGA2 Gain (Test) set VGA2 gain in 'Direct Signals' mode by setting 9 bit not log-linear control word directly.

PA Selection
Select Tx output stage PA1, PA2 or both off.

4.5.7. Rx LPF

The Rx LPF page contains the SPI controls for the receiver low pass filters, notably the LPF BW and also the controls for the DC calibration.

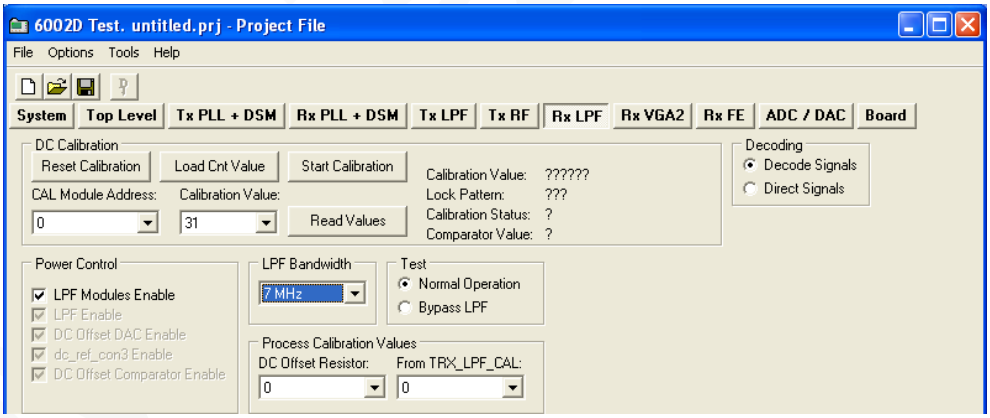


Figure 43 Rx LPF page

Description of each function available from this page is as follows:

DC Calibration
These are the individual controls for the DC correction and auto-calibration routines for the RX LPF (controlled by the 'Receiver' auto-calibration button on the 'System' page).
The Rx LPF DC calibration has 2 stages which can be calibrated:

- RXLPF(I) at Cal module address 0

- RXLPF(Q) at Cal module address 1

Power Control
Powers down the LPF modules, grayed out controls can be accessed by using direct signals mode. Using 'Decode' mode is recommended.

LPF Bandwidth
Set the LPF BW in the drop down box, from 0.75MHz to 14MHz. Note that RF system BW is twice this number, i.e. 0.75MHz LPF BW is 1.5MHz system BW.

Test
LPF bypass for test purposes. Ensure 'Normal Operation' is enabled.

Process Calibration Values
RC calibration values used to process trim the LPF BW, values are calculated in top level calibration and written into these locations (carried out automatically by 'LPF Cal' on 'System' page).

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out).

4.5.8. RX VGA2

SPI controls for the RX VGA2 stage settings.

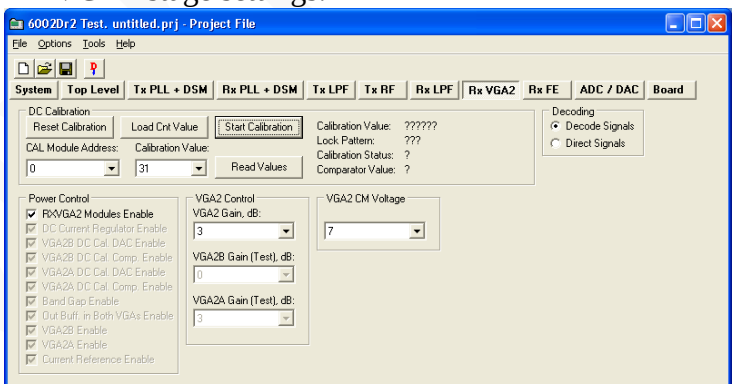


Figure 44 Rx VGA2 page

Description of each function available from this page is as follows:

DC Calibration

These are the individual controls for the DC correction and auto-calibration routines for the RX VGA2 (controlled by the 'Receiver' auto-calibration button on the 'System' page).

The Rx VGA2 DC calibration has 5 stages which can be calibrated:

- RXVGA2 Top at Cal module address 0
- RXVGA2a(I) at Cal module address 1
- RXVGA2a(Q) at Cal module address 2
- RXVGA2b(I) at Cal module address 3
- RXVGA2b(Q) at Cal module address 4

.

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out). Use 'Decode' mode.

Power Control

Powers down the RXVGA2 modules, grayed out controls can be accessed by using direct signals mode.

VGA2 Control

Sets RXVGA2 Gain, available range is 0 to 30dB in 3dB steps. Decoding is set to 'Decode Signals' for normal use.

VGA2B Gain (Test) and VGA2A Gain (Test) are available in test mode to control A and B stages directly. Decoding is set to 'Direct Signals' to use this function. This feature is not used for normal operation.

VGA2 CM Voltage

Sets RXVGA2 output common node voltage to interface to ADCs. Code 12, which corresponds to 780mV, is recommended.

4.5.9. RX FE

Sets the SPI controls for the RX Front End stages, including LNA selection, LNA gain, RXVGA1 gain and RX LO cancellation.

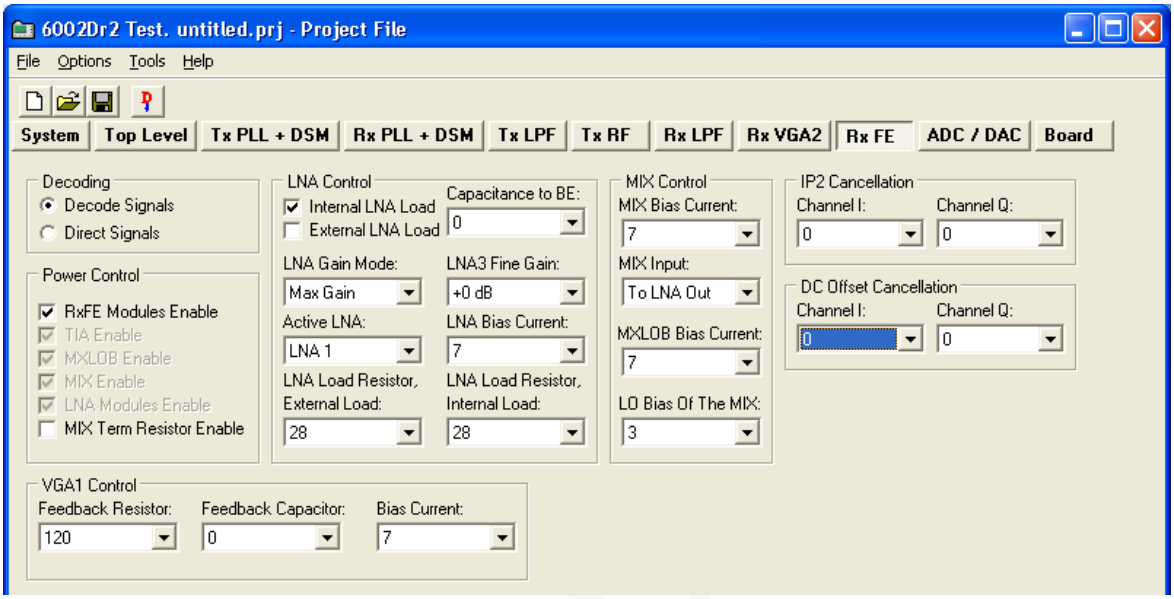


Figure 45 Rx FE (Front End)

Description of each function available from this page is as follows:

Decoding
Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the 2 options the available options are highlighted (and the unavailable ones grayed out).

Power Control
Powers down the RXFE modules, grayed out controls can be accessed by using direct signals mode.

DC Offset Cancellation
Applies DC level to mixer output to cancel DC level from LO leakage.

IP2 Cancellation
Applies offset to mixer to improve IP2 performance. Not required.

LNA Control
Settings for LNA controls are as follows:

- Internal/External LNA load tick boxes – use internal.
- Capacitance to BE – leave as default (0)
- LNA Gain Mode – selects LNA gain, Max, Mid and Bypass.
- LNA3 Fine Gain – fine gain setting for LNA3 which has no bypass mode, 0 to + 3dB.
- Active LNA – Select active LNA 1 to 3, also need to change the RX LO buffer in 'RX PLL + DSM' page when changing LNA. This control changes RX LO buffer automatically.
- LNA bias current – leave at default (7).
- External load – not used when Internal load selected.
- Internal Load (0 to 63) sets LNA gain, max (0dB) = 55, min (-9.2dB) = 0. Do not set above 55.

See figure below for settings

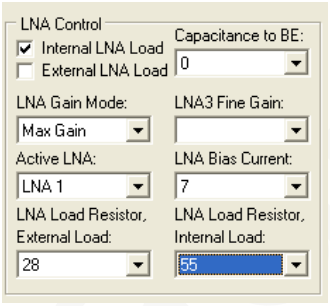


Figure 46 LNA Control setting

MIX Control

Settings for Mix control are shown below, do not change:

- MIX Bias current – '7', leave it at default.
- MIX Input – 'To LNA Out', leave it at default.
- MXLOB Bias Current – '7', leave it at default.
- LO Bias Of The MIX – '3', leave it at default.

See figure below for settings

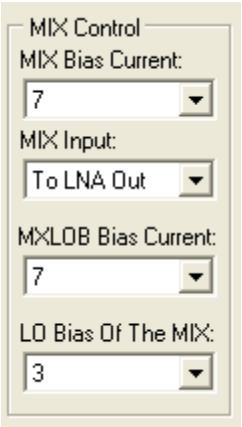


Figure 47 MIX Control settings

VGA1 Control

Feedback Resistor (0 to 123). Only use settings up to 120
Sets VGA1 gain, max (25dB) = 120, min (0 dB) = 0, so do not set above 120. Gain control is not log-linear.

Feedback capacitor (0 to 123)
Introduces a single pole LPF at VGA1 output. Bandwidth dependent on 'Feedback resistor' and 'Feedback capacitor'. For no filtering leave at default (0).

Bias Current - leave at default (7).

4.5.10. ADC/DAC

ADC / DAC page sets all the controls for the data ADCs in the receive path and data DACs in the transmit path.

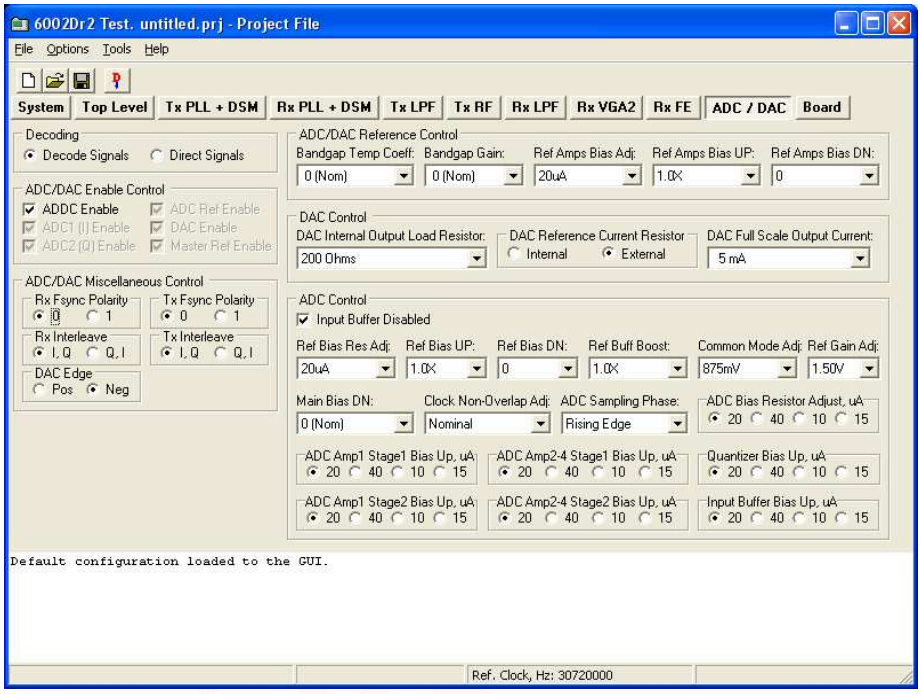


Figure 48 ADC/DAC page

Description of each function available from this page is as follows:

Decoding

Select 'Decode' or 'Direct' signals for control of different parts of the SPI memory map. When swapping between the two options, the available options are highlighted (and the unavailable ones are grayed out).

ADC/DAC Miscellaneous Control

Rx Fsync Polarity – sets the polarity of the RX IQ SEL signal for the first sample of the Rx IQ pair.

Rx Interleave – sets the order of the RX IQ pair.

Tx Fsync Polarity – sets the polarity of the TX IQ SEL signal for the first sample of the Tx IQ pair.

Tx Interleave – sets the order of the TX IQ pair.

See diagram below for explanation:

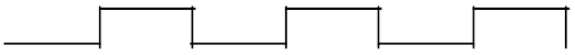
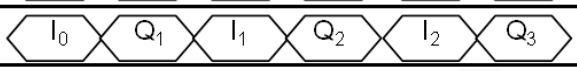
Fsync Polarity	Interleave	IQ Select (Tx)
		
0	I,Q	
0	Q,I	
1	I,Q	
1	Q,I	

Figure 49 DAC enable control timing for TX

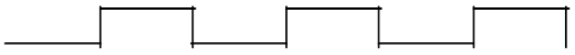
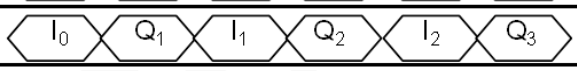
Fsync Polarity	Interleave	IQ Select (Rx)
		
1	I,Q	
1	Q,I	
0	I,Q	
0	Q,I	

Figure 50 ADC enable control timing for RX

DAC Edge

DAC Edge – selects the edge of the DAC clock which the data is clocked from. Negative is usually required.

ADC/DAC Enable Control

Check 'ADC Enable' to enable ADCs and DACs. Sub-blocks are also independently controllable in 'Direct Signals' mode.

DAC Control

- Internal output Load Resistor 50, 66, 100, 200 Ohms or Open Circuit setting (when using external load resistor).
- DAC Reference Current resistor – use External.
- DAC Full Scale Output Current (2.5, 5, 10mA). Use Load resistor and Full scale output current to control DAC output voltage swing.

ADC/DAC Reference Control

Use default settings:

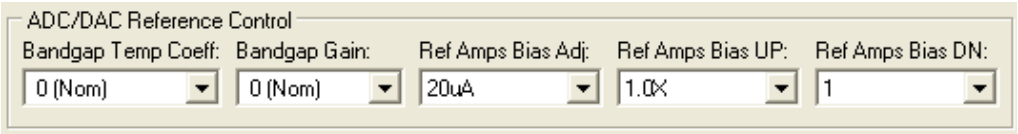


Figure 51 ADC/DAC Reference control – default settings

ADC Control

Use default settings with following exceptions:
Ref Bias Res Adj = 10uA (minimizes ADC noise)
Common mode Adj = 960mV.
Ref Gain Adj = 1.75V.

See diagram below for settings including the exceptions listed above which have been highlighted in red.

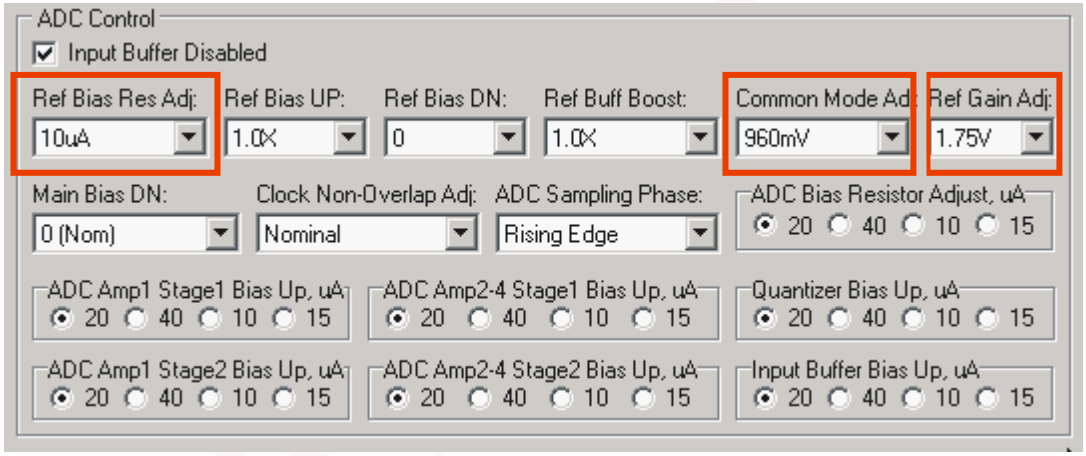


Figure 52 ADC Control settings

4.5.11. Board

The board section programs the onboard frequency synthesizer Si5356 (U8). The frequency synthesizer control frequency of digital interface between the DEO – Nano board and Myriad RF. To upload the configuration press button *"Upload register map to Si5356A"*, see figure below.

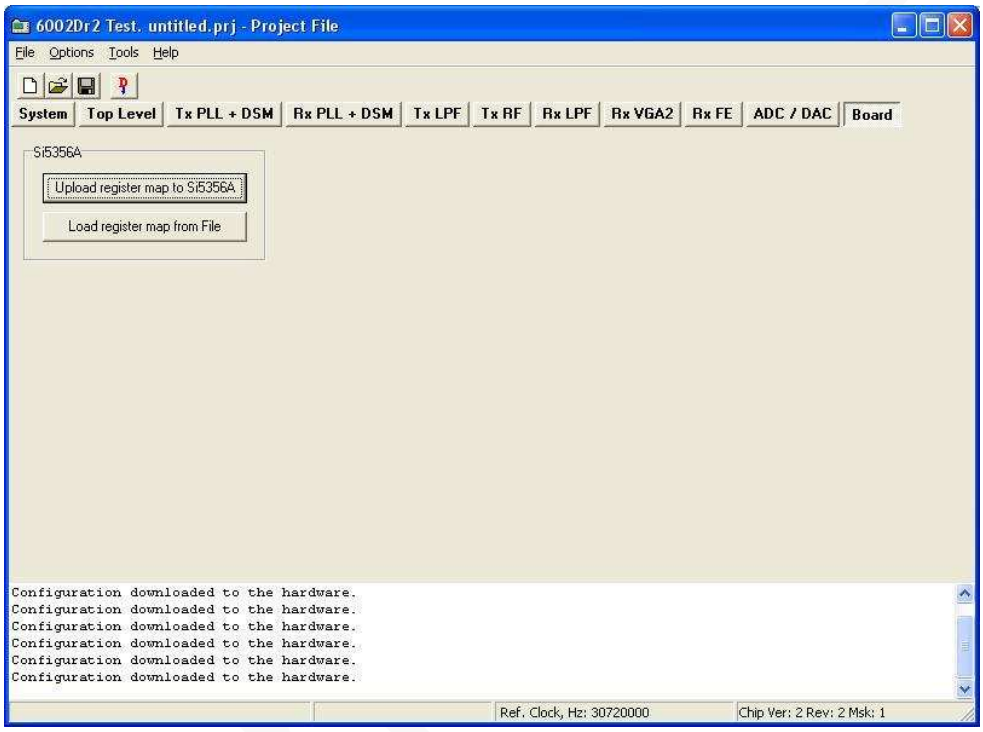


Figure 53 Board section

This program synthesizer to deliver:

- CLK_IN - 30.72 MHz
- TXCLK_BUF - 30.72 MHz
- RXCLK_BUF - 30.72 MHz
- EXT_CLK_BUF - 10 MHz

The desired clcok configuretion can be set by loading the reigeister map for Si5356 controller. For this, the register map file have to be created (in C Code Header file) with Clock Builder Desktop software [download]. When file is created, laod it by pressin *"Load register map from File"*, select *.h and press *"Upload register map to Si5356A"*.

5

Transmitter and Receiver Basic Setup

5.1 Transmitter Setup and Basic Testing

This is a quick check without the need to connect to an external baseband interface. The test using DC to provide LO leakage to test the Tx chain, for accurate repeatable measurements the Baseband Interface (data DACs) should be set to a known state. Also, verify the reference clock frequency is set properly. The reference clock frequency can be set in the top "Options" menu under "Reference Clock". It is typically set to 30.72 MHz but can vary depending upon the frequency of the TCXO installed on the design kit.

5.1.1. Top Level Setting

Using the "Top Level" page. Verify the "Tx DSM SPI" Clock Buffers and the "Soft Tx Enable" Power Control are enabled in the menus as shown below.

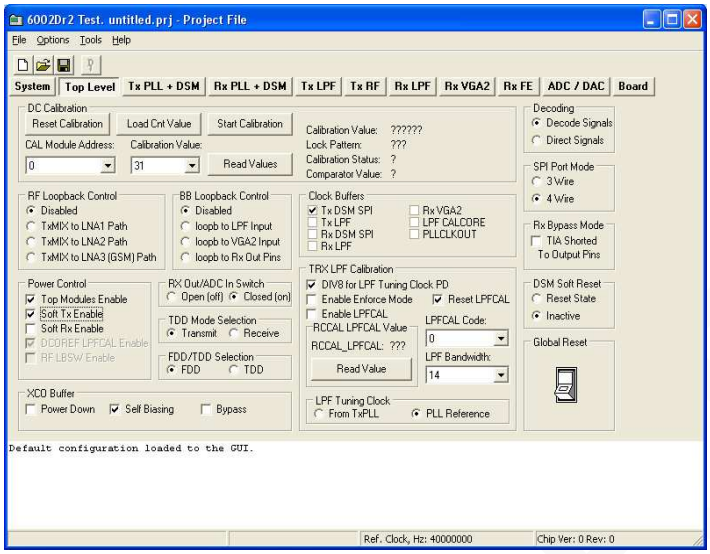


Figure 54 Top Level Settings

Note: The LMS6002 communication can be easily checked by toggling the "Soft Tx Enable" in the Power Control section. The current change can be observed on power supply display.

5.1.2. TX LPF & Gain Setting

Using the 'Tx LPF' page. Set the LPF bandwidth to your desired value; see figure below, example setting is 14 MHz.

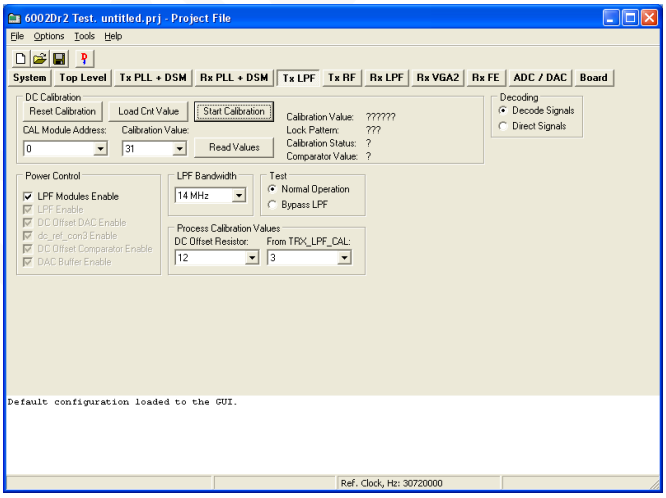


Figure 55 Setting Tx LPF bandwidth

Select Tx RF page to set gain and select Tx Output. For basic operation select the following

- VGA1 gain = -10

- VGA2 gain = 15
- PA1 Selected

See diagram below to check selections.

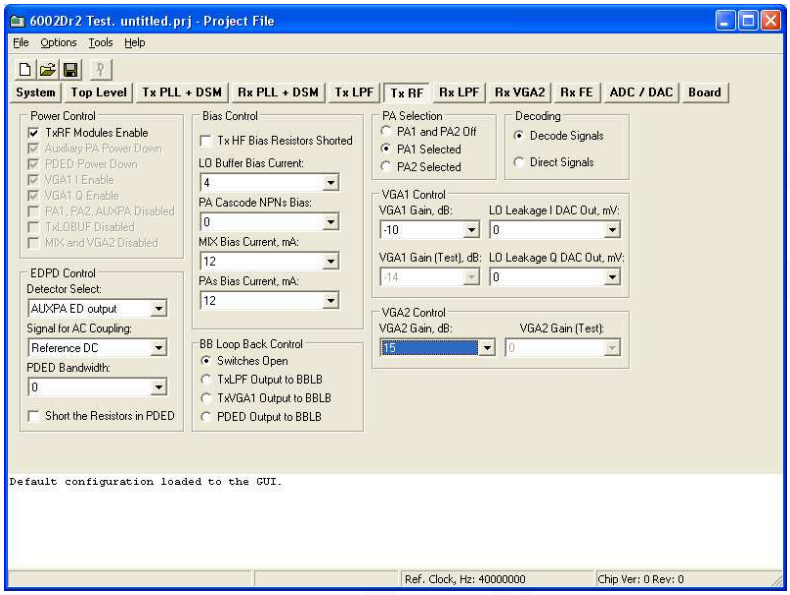


Figure 56 Tx gain setting and PA selection

5.1.3. TX PLL Setup

Select Tx PLL + DSM page to set up the Tx PLL. Please follow the instructions 1 to 3 below in the order shown and illustrated in the figure below.

1. Set **'Output frequency'** (Tx frequency), example shown = 2.14GHz and then press **'Calculate'**, note divider ratios should change.
2. Change **'CP Current and Offset'** (CP = Charge Pump) to the following:
   a. Current , uA = 1200uA
   b. Up offset, uA = 30uA
3. Press "**Tune**" to fine tune VCO capacitor selection. If you want to observe the VCO capacitor selection algorithm results select "**Log**".

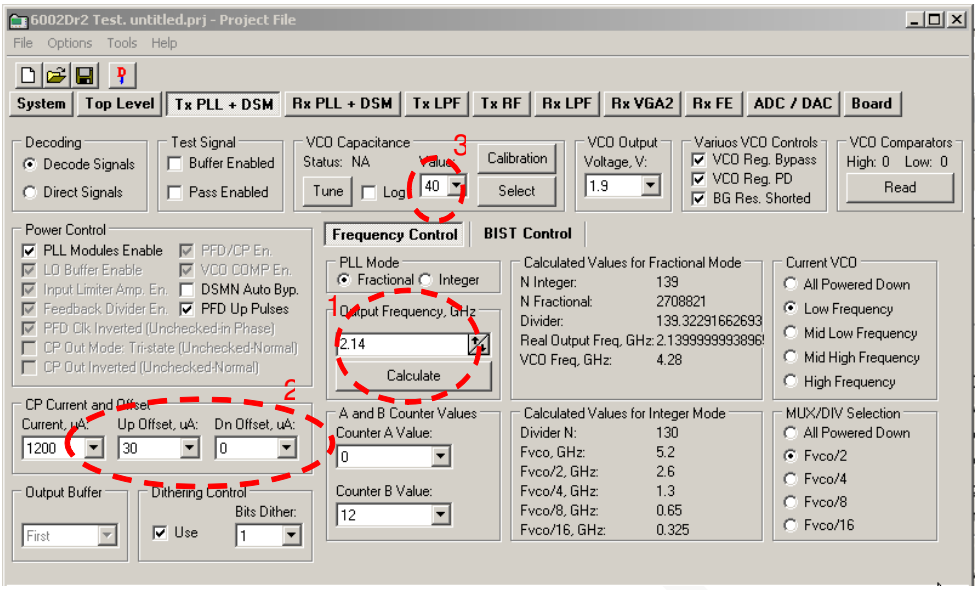


Figure 57 Tx PLL setting

5.2 Testing TX Output

When transmitter is configures as it showed in section 5.1, one of your selected TX output can be connected to spectrum analyzer (SA). In SA you can now observe the results of this basic operational test. The test is looking at the DC offset from the un-programmed data DAC as LO leakage and the example shown below is measuring a value of 2.1dBm. As the DACs are not programmed yet levels may be different from the screen shot example.

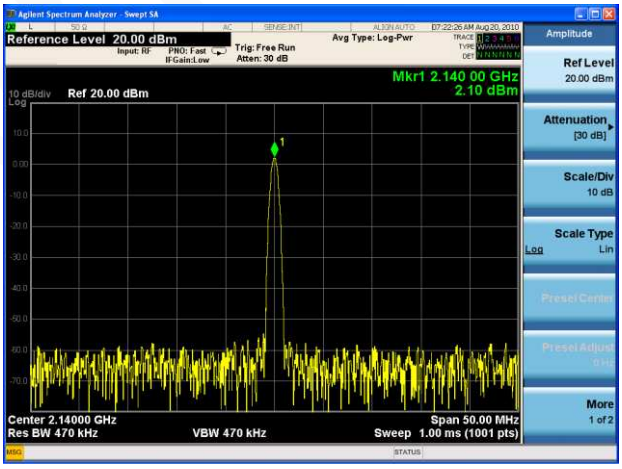


Figure 58 Basic TX testing using DC offset resulting in LO leakage

5.2.1. TX Basic Operation Checks

To check basic TX frequency and gain control conduct some tests changing frequencies and gain settings. The following four tests are recommended:

TX RF – VGA 1 change setting from -4 to -35 and observe results. LO should vary by approx 1 dB steps, 31dB range.
TX RF – VGA 2 change setting from 0 to 25 and observe results. LO should vary by approx 1 dB steps, 25 dB range.
Change frequency from 2.14GHz to 2.11 GHz and press '**Calculate'/'Tune'** (CAP value should change), check Spectrum Analyzer.
Change frequency from 2.11GHz to 2.17 GHz and press '**Calculate'/'Tune'** (CAP value should change), check Spectrum Analyzer.

5.3 Receiver Setup and Basic Testing

Basic functionality checks on the receiver side are achieved by using the Analog output from connector J3, not using the digital output from the data ADCs.

5.3.1. Top Level Settings

Using the "Top Level" page, verify the "Rx DSM SPI" Clock Buffers and the "Soft Rx Enable" Power Control is enabled in the menus as shown below. Also verify the RxOut/ADC in Switch is set to Closed.

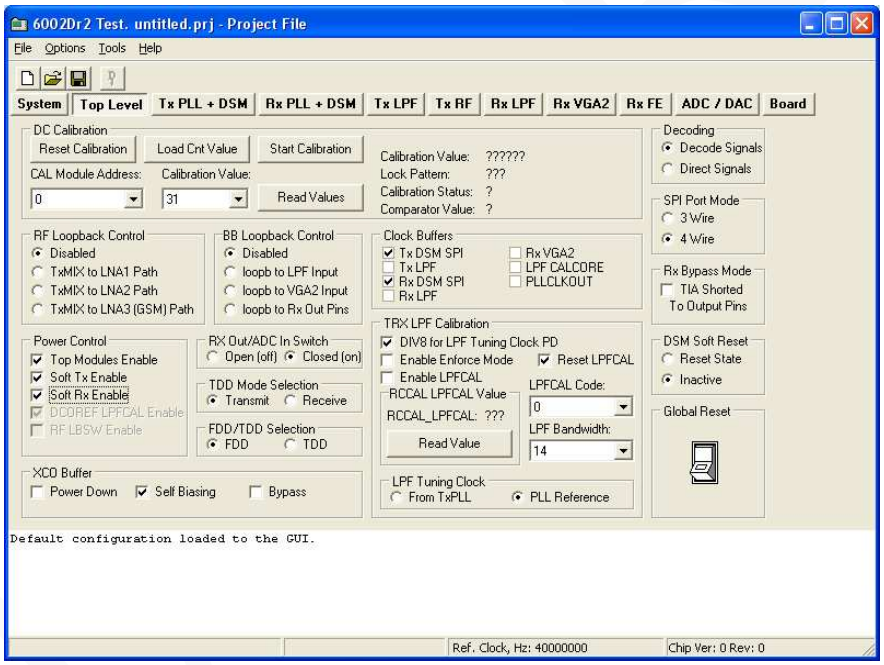


Figure 59 Top Level Settings

5.3.2. RX LPF & Gain Setting

Set LPF bandwidth to 7MHz as illustrated in figure below.

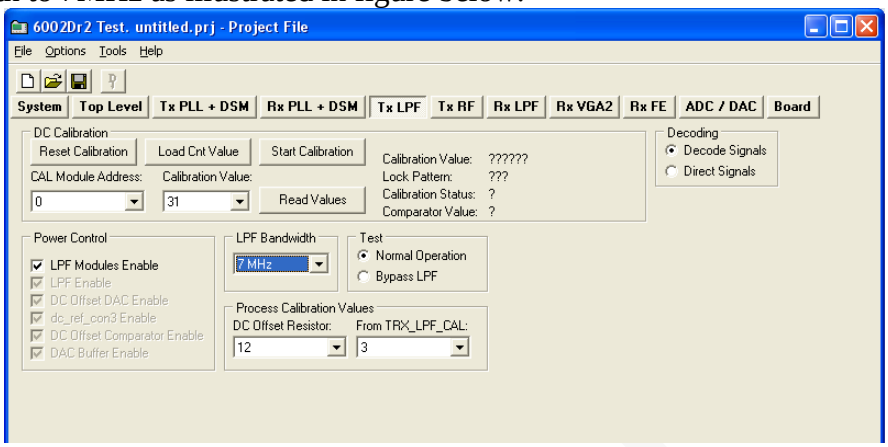


Figure 60 Setting Rx LPF to 7 MHz

Select '**Rx VGA2 page'** to set the gain. For basic operation set VGA2 gain = 30. See figure below.

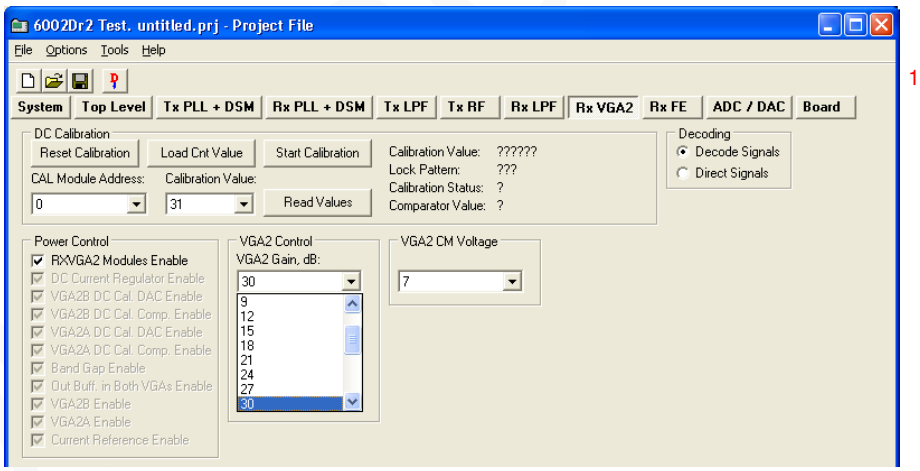


Figure 61 Setting Rx VGA2 gain

Select '**RX FE page'**, check **'VGA1 Control Feedback Resistor'** is set to 120 (Default setting). The feedback resistor controls the gain of VGA1. Set LNA gain by using **'LNA load resistor – Internal load',** set to 55.
Check **'Active LNA'** = LNA1 and **'LNA Gain Mode'** is set to Max Gain.

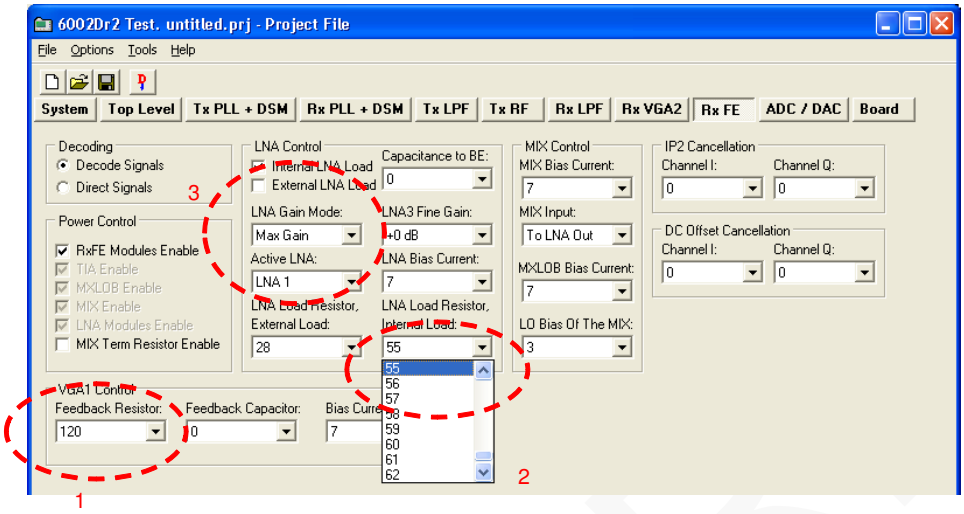


Figure 62 Rx LNA and VGA1 settings

5.3.3. RX PLL Setup

Select **'Rx PLL + DSM'** page to set up the Rx PLL. Please follow the instructions below in the order shown and illustrated in the figure below.

a. Set **'Output Frequency'** (Tx frequency), example shown = 1.95GHz and then press **'Calculate'**, note divider ratios should change.
b. Change **'CP Current and Offset'** (CP = Charge Pump) to the following:
a. Current , uA = 1200uA
b. Up offset, uA = 30uA
c. Press "**Tune**" to fine tune VCO capacitance. If you want to observe the VCO capacitor selection algorithm results select "**Log**".
d. Make sure that '**Output Buffer**' is set to First.

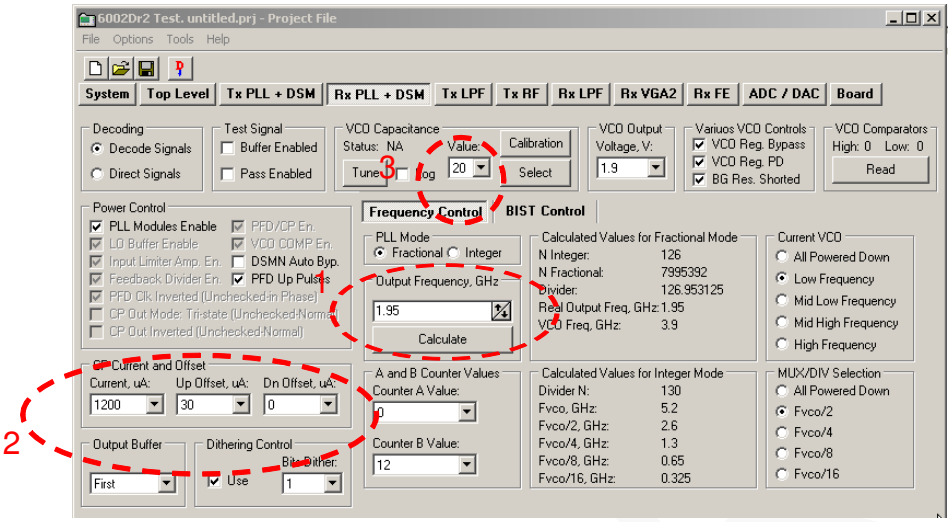


Figure 63 Rx PLL settings

5.4 Testing RX Analogue Output

Set the signal generator to 1951MHz (1MHz offset from PLL frequency selected) and input a sine wave at -60dBm into the reference board antenna connector (connector J2).
Configure receiver as showed in section 5.3. Connect an oscilloscope to J3.20 or J3.18 on the design kit. Correct operation will results in two sine waves, 90° out of phase, being displayed. If the sine wave output for I and Q can be seen then the receiver is operational. See figure below.

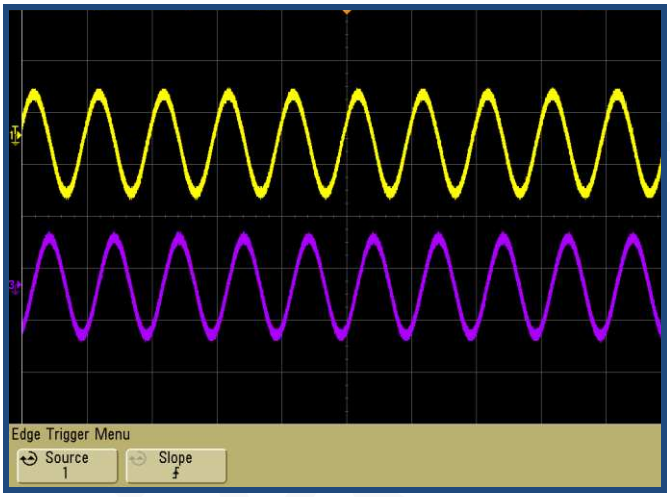


Figure 64 Oscilloscope capture of 1 MHz I & Q Sine wave outputs

5.4.1. RX Basic Operation Checks

To check basic Rx frequency and gain control conduct some tests changing frequencies and gain settings. The following six tests are recommended:

a. RX VGA2 – VGA 2 change setting from 30 to 0, observe results, gain should decrease.
b. RX FE – VGA 1 change feedback resistor from 120 to 0, observe results, gain should decrease.
c. RX FE – LNA gain change from Max to Mid, observe results, gain should decrease.
d. RX FE – LNA gain change from Mid to Bypass, observe results, gain should decrease.
e. Change frequency from 1.95GHz to 1.92GHz and press '**Calculate'/'Tune'**. Change Signal Generator to 1.921GHz (1MHz offset from PLL). Observe results.
f. Change frequency from 1.92GHz to 1.98GHz and press '**Calculate'/'Tune'**. Change Signal Generator to 1.981GHz (1MHz offset from PLL). Observe results.

6

LMS6002D Calibration Procedures

6.1 TX LO Leakage Calibration

This procedure assumes the transmitter has been turned on and initialised, it describes how to then use the parameters within the LMS6002D to cancel any LO leakage from the IQ modulator.

It is intended that this will be a single point calibration per band, the example given uses 3GPP Band I with a centre frequency of 2140 MHz.

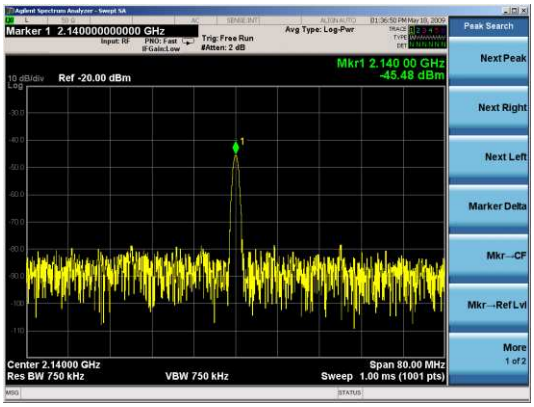
The transmitter should be set up with the following parameters:

Parameter	Page	Value
Transmitter Frequency	System Interface	2140
Soft Tx enable	Top Level	tick box selected
Tx DSM SPI clock buffer	Top Level	Tick box selected
LPF bandwidth	Tx LPF	3.5MHz
PA1 selected	Tx RF	PA1 Selected
VGA1 gain	Tx RF	-10
VGA2 gain	Tx RF	15

Table 9 Transmitter setup

No signal should be applied to DAC's or DC Low signal, generated by BB can be applied. The previous method is more preferable. Note: Set gain settings before calibration.

The output should be observed on the spectrum analyser.



The signal on the screen represents the LO feedthru from the transmit modulator.

In this case the level is -45dBm

Figure 65 Transmit Output

Assuming the LPF Core calibration has been carried out in the initialisation then press the 'Transmitter' button on the System Interface page in the Automatic Calibration area.

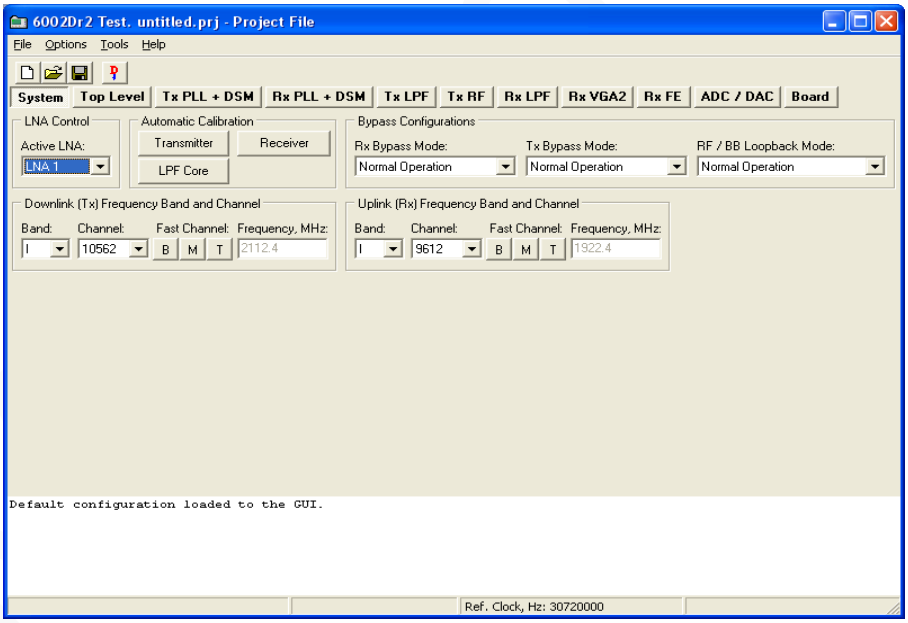


Figure 66 System Window. Use Automated Calibration

'Tx Calibration Done' should appear in the text box in bottom of the display.

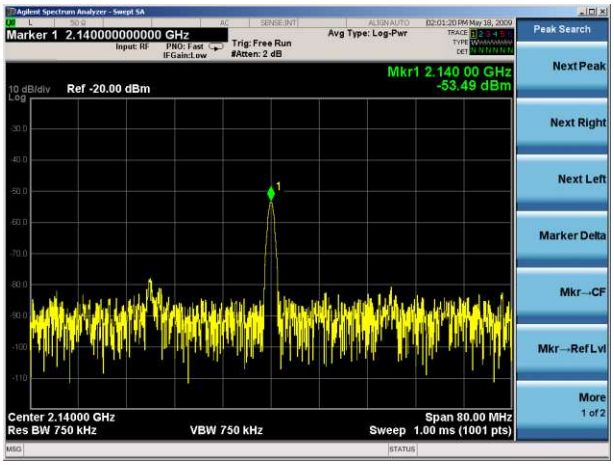


Figure 67 Transmit Output After Calibration

In this case the LO dropped after automatic calibration to -53dBm as shown in Figure 67.

Note. Automatic calibration is intended to make the DC zero at the output of the LPF, this is not the same as cancelling the LO, it just makes the DC contribution from the IQ chain as low as possible.

It may be the case that the level will go up after automatic calibration – do not worry if it does, this is due to the default values on power up cancelling the LO at the selected frequency.

Select the 'Tx RF' page in the SPI software.

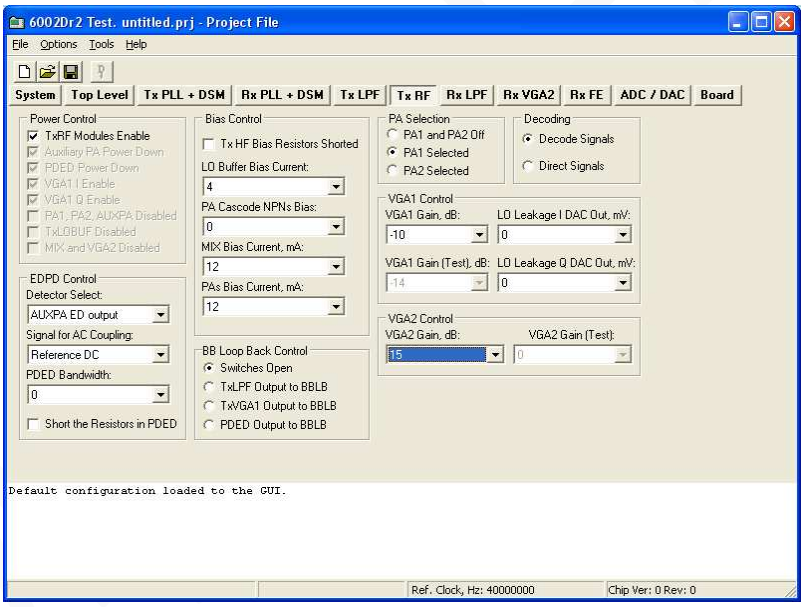


Figure 68 Tx RF window

The LO cancellation DACs level is in the boxes marked' 'LO Leakage DAC I Out' and 'LO Leakage DAC Q Out'. The entry mechanism is different to the LPF DC offset and easier to tune.

LO Leakage DAC I/Q Out boxes contain the value of the DC LO cancellation DAC in mV and ranges from -16 to 15.875.

Click on the VGA1 DC shift box, a drop down menu appears, click again and the drop down menu collapses leaving the entry box blue.

The value in the box can now be adjusted using the up and down arrows on the key board, once the number has changed the register in the LMS6002D is updated, allowing for a simpler search method.

a. Select the I DAC box
b. Increase / decrease until minimum is found.
c. Do same for Q.
d. It is possible that 0 is the best result for both as the optimum has been found during the LPF calibration above.

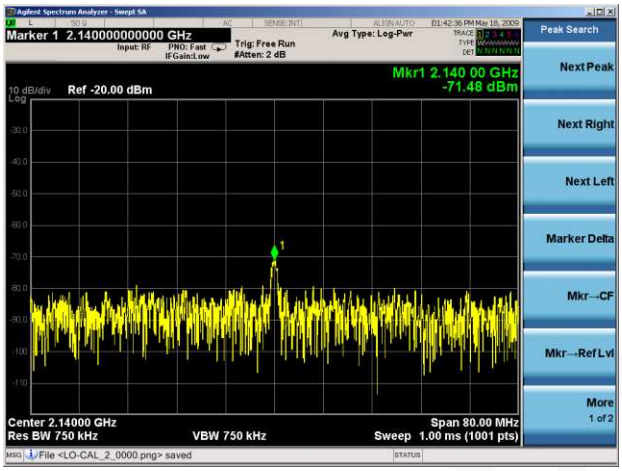


Figure 69 Transmit output after calibration

In this case the LO cancellation has been improved to -71dBm as shown in this figure. The optimum values were:

I = 0
Q = -0.125

6.2 Transmit I/Q Balance Calibration

This procedure assumes the TX LO calibration procedure in section 6.1 has been completed. The purpose of this calibration is to optimize I/Q balance for optimum transmit EVM performance. Typically, this is done by applying a 1 MHz CW tone from a digital I/O card through the digital interface at J5. The 1 MHz CW tone could also be applied at J3 from a differential I/Q analog signal generator.

Initially, the user should observe a spectrum at the tuned frequency that is similar to the figure below.

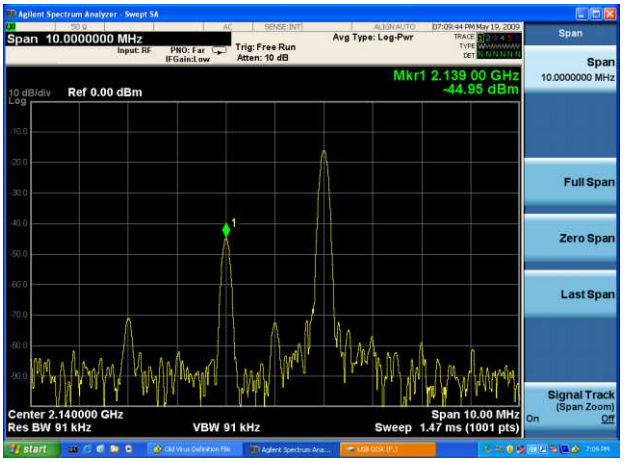


Figure 70 Initial -1 MHz Image Spectrum

The wanted signal can be seen at 1MHz offset from the selected RF frequency (2140MHz), In this case at a level of approx -16dBm.

The unwanted (lower) sideband can be seen at -1MHz offset, with no correction is at a level of -45dBm (29dBc)

Note – the 3rd order product at LO-3*1MHz can be seen also.

The image or sideband rejection performance of the system depends upon the phase and gain match of the I and Q paths. This includes the test equipment, cables and of course the LMS6002D transmit path. The closer in length the cables between the signal generator and the test board are the better.

The phase match also depends on the accuracy of the sin/cosine split on the LO of the IQ modulator (inside the LMS6002D), the bulk of the phase correction is for this parameter – hence, amplitude mismatch will vary little with frequency, however phase mismatch may be quite different for each band.

The result of the phase angle calibration can be seen below.

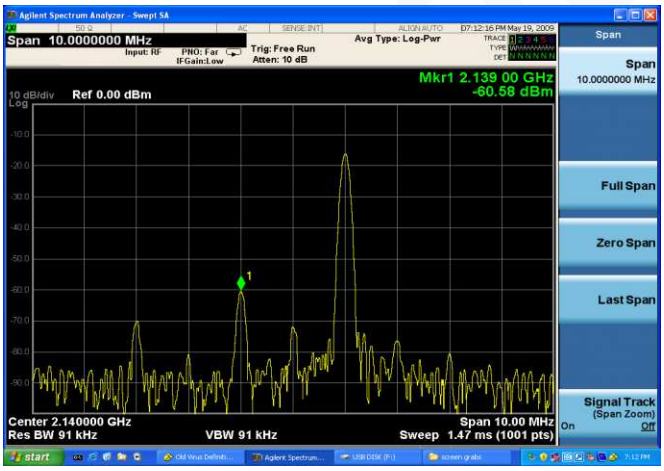


Figure 71 Phase angle calibration

The result of the phase angle calibration is seen.

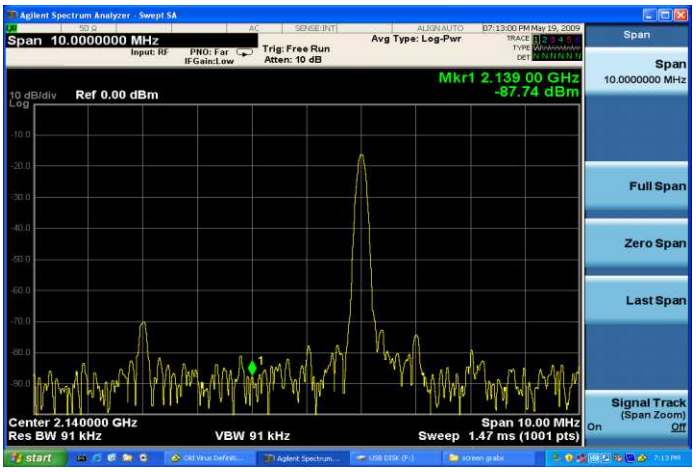
The unwanted sideband has been reduced to -60dBm (-44dBc).

The optimum value found in this case was 4.1 deg.

The result of the amplitude balance calibration is seen.

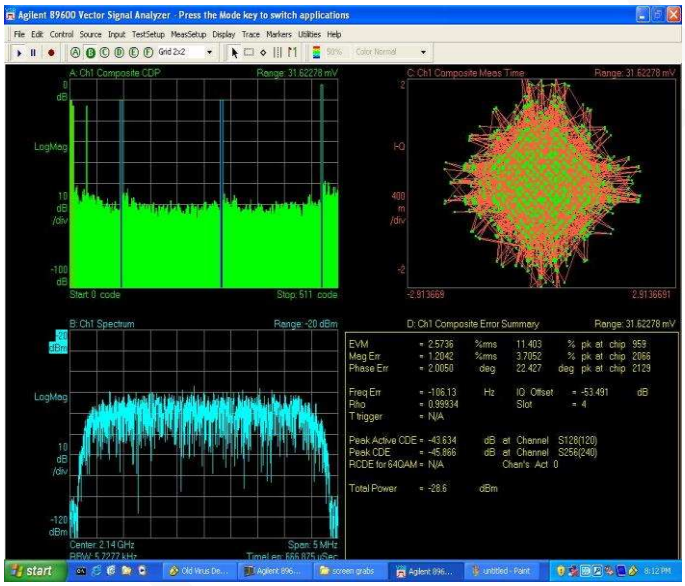
The unwanted sideband has been reduced to <-80dBm (-64dBc).

The optimum value found in this case was 0.11 dB.



If necessary repeat the phase and amplitude adjustments until the optimum values are found and an EVM ≤ 4% is measured as shown below. The transmit I/Q balance calibration is valid on the flat part of the LPF bandwidth. As you approach the LPF corner frequency the lower sideband cancellation will begin to degrade. For example, with the 1 MHz tone used in this calibration the EVM will degrade as the filter bandwidth decreases below 1.92 MHz.

Figure 72 Amplitude balance calibration



Using the VSA analysis software.

WCDMA TM2 codes can be seen in top left.

Spectrum, bottom left

Composite constellation, top right.

Signal statistics, Bottom right.
EVM 2.5%
Peak CDE -45 dB

Figure 73 Transmit EVM performance after calibration

Note: The EVM is dependent on a number of parameters being set up correctly. Phase noise performance of the LO is dominant factor in the above measurement.

6.3 Receiver DC Calibration

The receiver has a number of self-calibration routines which are designed to cancel out DC offsets from the LPF's and the VGA's. In addition it has I and Q LO cancellation DACs which can cancel out the DC caused by the LO leakage in the mixers.

It is similar to calibration in the transmit path where the low LO levels are easy to measure with the spectrum analyser but low DC levels are more difficult to measure.

In most cases the baseband (BB) processor is capable of adjusting the DC calibration (and also the IQ phase and amplitude match) based on measurements of the uplink signal. It is only necessary to ensure the calibration is good enough so the ADC is not at full scale.

However for testing without the BB the following procedure has been devised. This method uses the I and Q samples from the oscilloscope. The Agilent VSA software is used to sample the oscilloscope and display the spectrum. The oscilloscope used for this procedure must be supported by the Agilent VSA software. The spectrum analyser cannot be used because it cannot display DC.

1. Set the receiver up as in section 5.3.
2. Resetting DC Calibration.
   In 'Rx FE' Tab, set RXVGA1 I and Q DC Offsets to middle value 0.

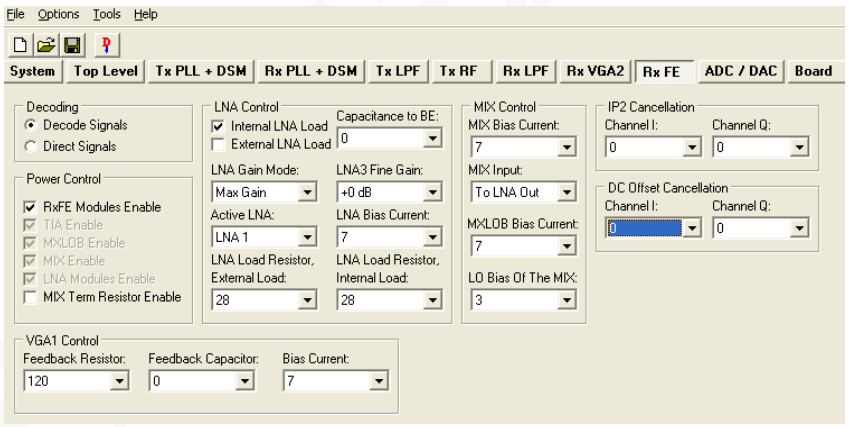


Figure 74 Rx FE page

3. In ‘Rx LPF’ Tab, press “Reset Calibration”.

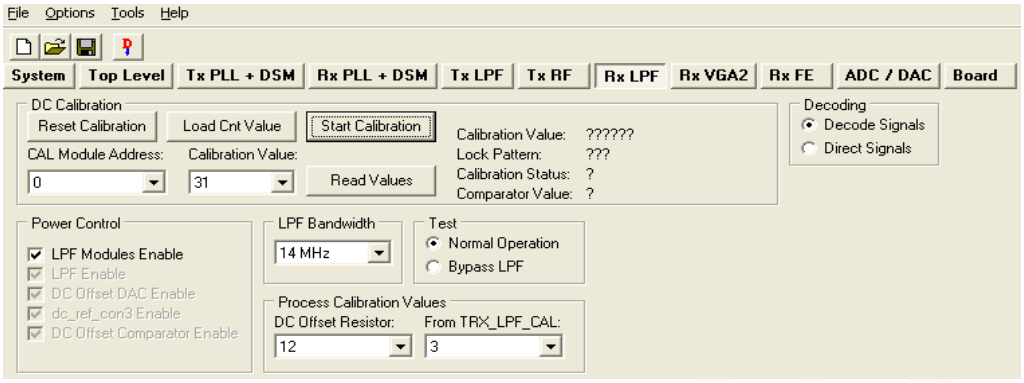


Figure 75 Rx LPF tab

4. In ‘Rx VGA2’ Tab, Press “Reset Calibration”.

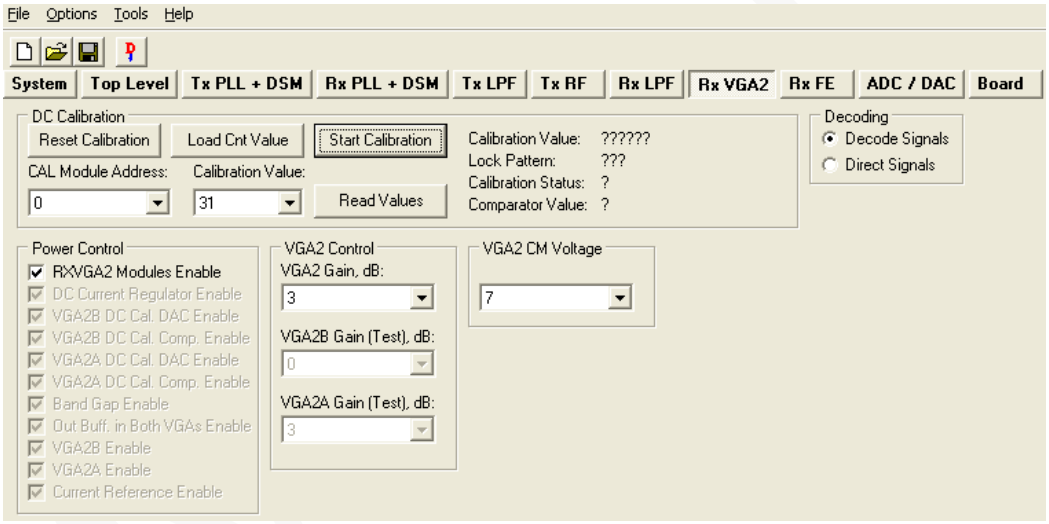


Figure 76 Rx VGA2 Tab

DC Leakage after Calibration Reset.
DC offset very large – would prevent automatic DC calibration.

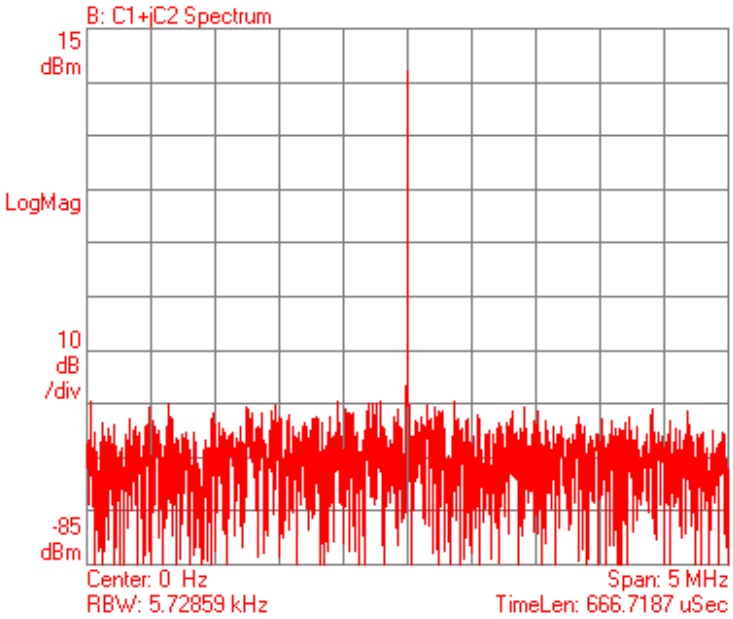


Figure 77 Receiver LO leakage

5. RXVGA1 Offset Optimisation
   In 'RX FE' tab, slightly adjust the RXVGA1 DC offset values to reduce the DC offset.

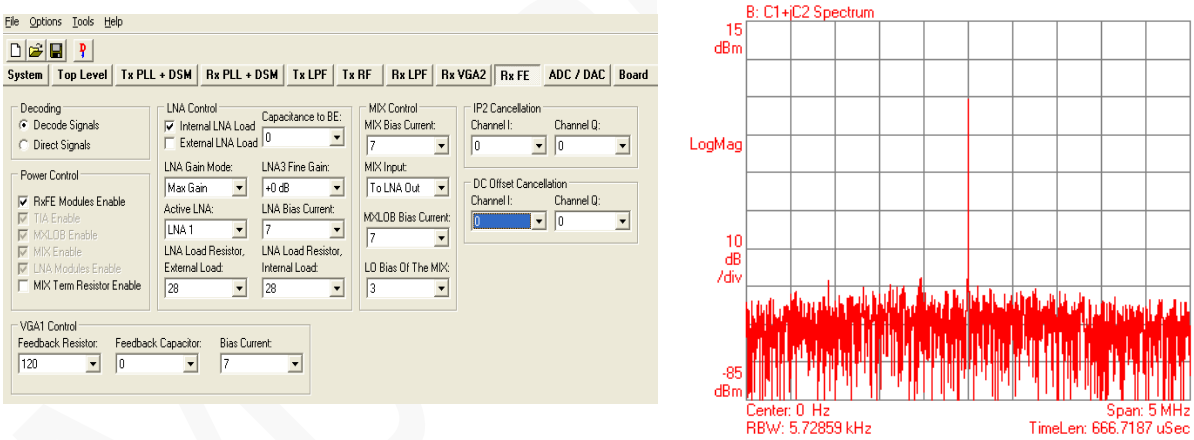


Figure 78 Rx VGA1 DC Offset Adjust in RX FE Tab

6. Automatic DC Calibration

   If RX VGA1 DC Offset is small enough, automatic DC calibration can be used in System Interface, select receiver automatic calibration.

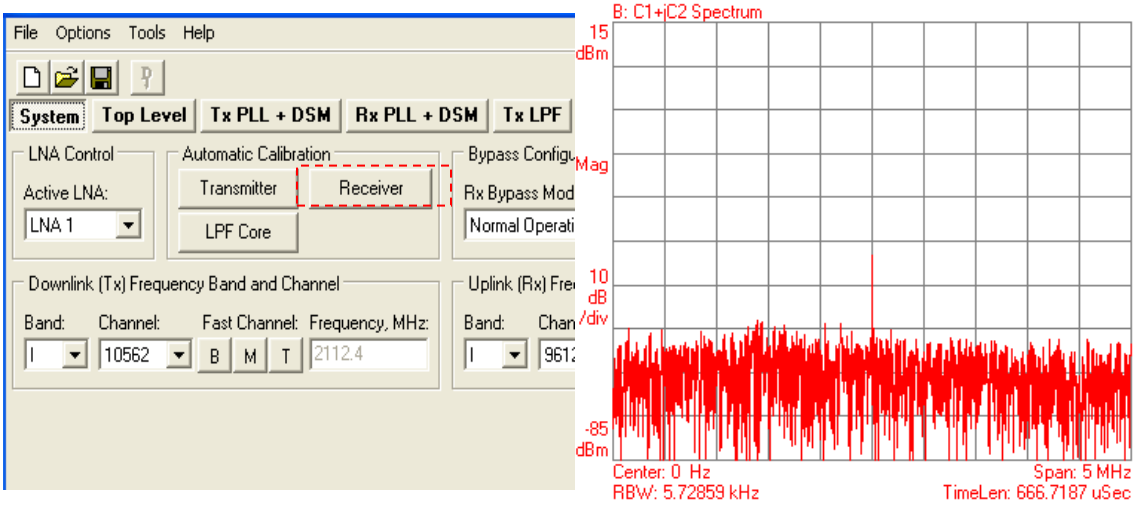


Figure 79 Rx automatic DC calibration result

6.4 Calibration Process Summary

There are several similarities between receive and transmit DC calibration process but one fundamental difference. During the transmit calibration process no signal can be applied to the input of the transmitter. An automated DC calibration is performed to ensure the BB stages contribute no DC offset to the LO leakage calibration. Finally, an LO leakage calibration is performed to minimise LO leakage. The transmit input must be zero so that the automated DC calibration can find the correct minimum DC point. This DC calibration process provides optimum transmitter performance.

In the receiver a similar DC calibration process is applied but in reverse order. When no signal is applied at the input of the receiver, the resulting DC offsets at the receiver outputs are due to LO leakage (multiplied by the RX gain) and the DC offsets in the LPFs and VGAs. The first step is to calibrate the LO leakage contribution and minimise the DC offset due to LO leakage. After the DC offset due to LO leakage has been removed then the automated DC offset calibration routines can be run. These DC offset calibration routines will remove the DC offset contribution from the LPFs and VGAs. This calibration process will result in minimum DC offset in the receiver and optimum sensitivity and dynamic range.

7

Appendix A – Saving and Retrieving SPI Test Setups

The LMS6002D chip set up can be stored in a *.prj file and used in the future. The Save Project feature of the software tool allows all the SPI settings to be saved for future use.

7.1 Saving a Setup

To save the SPI setup being used, press the File button on the toolbar. Select “Save Project” as shown below.

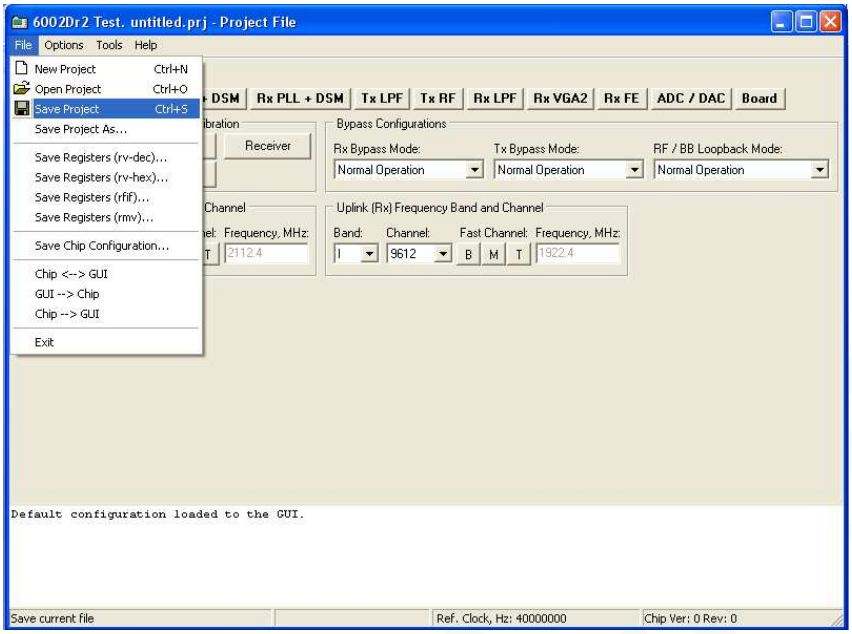


Figure 80 Save Project feature

7.2 Loading *.prj Files

A *.prj file can be loaded using the standard windows procedure as shown below.

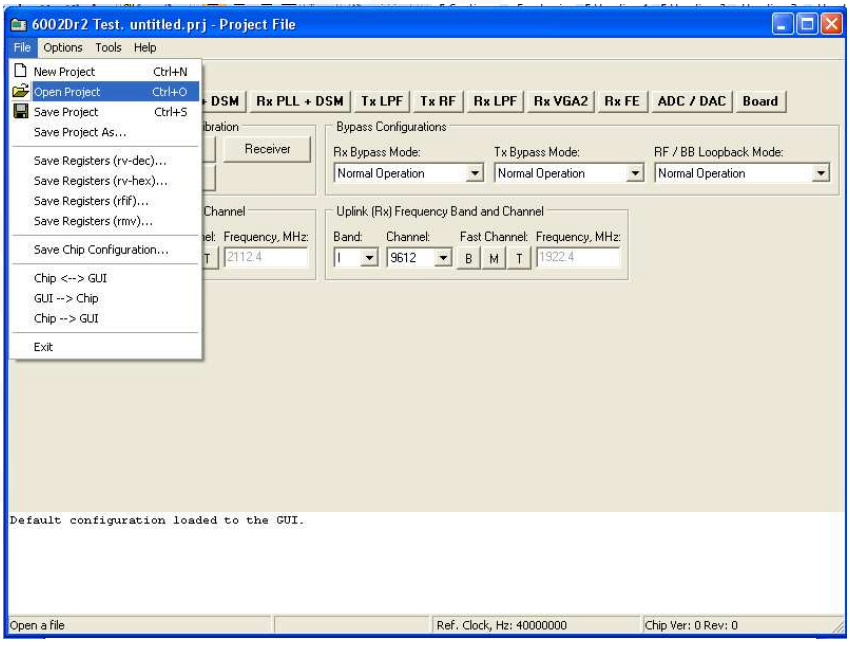


Figure 81 Open project

Select File – Open Project – then select the project that was previously saved from the window file box.

When loading files the software GUI tool can be setup to either load variables into the tool, but not download them to the chip or to download the variable into the tool and auto download them.

Auto Download is enabled by the Options menu as shown below.

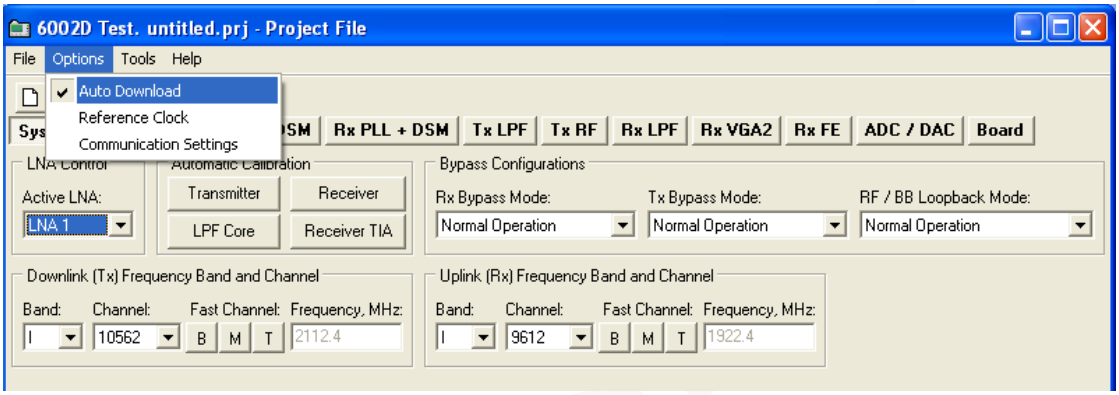


Figure 82 Auto Download feature

If Auto Download is not enabled then the whole SPI map can be sent to the chip by using the download button  as shown below.

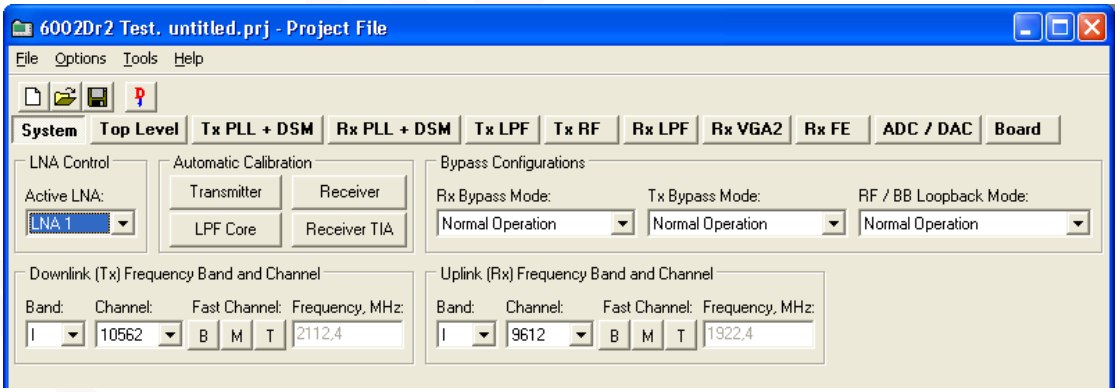


Figure 83 Download Button for Previously Saved Setup

Note : The Ref clock frequency is not strictly part of the SPI information, it is used to calculate the divider ratios for the PLLs. When you start the software for the first time the default clock frequency is 40MHz. You need to change this to the TCXO frequency which typically is 30.72

MHz. If you use a different TCXO frequency you need to change the reference clock (Tools->Reference Clock).

8

Appendix B – PC and USB Controller Communication

USB microcontroller emulates COM port and in system it will be seen as virtual COM port .To control LMS6002 chip you need to write and read the commands and data using standard COM port driver.

8.1 COM Port Settings

The software must open COM port using those settings:

Setting	Describtion
Port	Determine to what port USB controller is connected
Baud Rate	Baud Rate Baud rate defines SPI bus clock frequency: 9600 baud means 4Mhz SPI clock 14400 baud means 2Mhz SPI clock 19200 baud means 1MHz SPI clock 38400 baud means 500kHz SPI clock 57600 baud means 250kHz SPI clock 115200 baud means 125kHz SPI clock
Data	8 bit
Parity	None
Stop	1 bit
Flow Control	None

Table 10 COM Port Settings

8.2 Communication testing

To test communication between USB microcontroller and PC application you can to send the test command and check if microcontroller sends response.

Command to Microcontroller	Microcontroller response
0x54	0x0A 0x0D 0x4F 0x4B 0x0A 0x0D
0x74	0x0A 0x0D 0x4F 0x4B 0x0A 0x0D

Table 11 Communication testing commands

8.3 Controlling Reset line of LMS6002

It is possible to activate and deactivate Reset line of LMS6002 chip.

Command to Microcontroller	Microcontroller response
0x11	Sets Reset line to '0' (Active, low voltage)
0x12	Sets Reset line to '1' (Inactive, high voltage)

Table 12 Reset line control commands

8.4 Read data from LMS6002

To read data from LMS6002 chip you need to send command 0x20 to USB microcontroller and one or more addresses you want to read from. Address length is 8 bit and the structure is as follows (in binary notation):

MSB							LSB
Read code	SPI module address			Register in SPI module address			
0	A6	A5	A4	A3	A2	A1	A0

Table 13 The address length

SPI module and register addresses are described in “SPI Register Map” document.

Example:
Let’s say we want to read register address 0x4 from Top SPI module (address is 0x0). So, we need to send command sequence to USB microcontroller:

0x20 0x04

After that microcontroller will respond by 0x22 (if the chip is LMS6002Dr2).

If you want to read more than one register from SPI modules, you need to write command 0x20 and then register addresses you want to read.

Example:
Let's say we want to read register address 0x4, 0x5 and 0x6 from TxPLL SPI module (address is 0x1). So, we need to send command sequence to USB microcontroller:

0x20 0x14 0x15 0x16

After that microcontroller will respond by 0x88 0xB1 0x1C (if the chip is LMS6002Dr2 and chip is just after reset).

8.5 Write data to LMS6002

To write data to LMS6002 chip you need to send command 0x30 and one or more address – data pairs to USB microcontroller. Address structure is the same as described in 4.4 Read data from LMS6002.

Example:
Let's say we want to write data 0x19 to register address 0x4 to RxPLL SPI module (address is 0x2). So, we need to send command sequence to USB microcontroller:

0x30 0x24 0x19

Example:
Let's say we want to write data 0x88, 0xB1 and 0x1C to register addresses 0x4, 0x5 and 0x6 for RxPLL SPI module (address is 0x2) respectively. So, we need to send command sequence to USB microcontroller:

0x30 0x24 0x88 0x25 0xB1 0x26 0x1C

There is no response from USB microcontroller when data are written to the LMS6002.

9

Appendix C - Test System Connections

9.1 Basic Setup

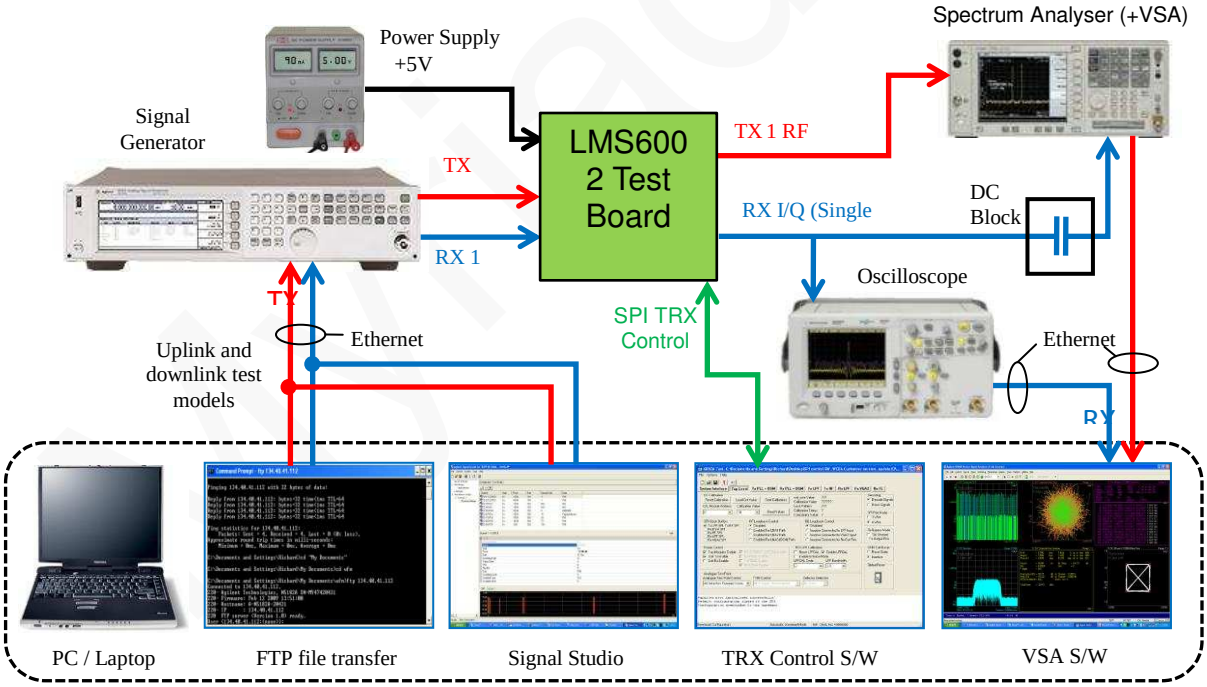


Figure 84 Test system connections for receive and transmit Testing

9.2 Transmitter Test System Connections

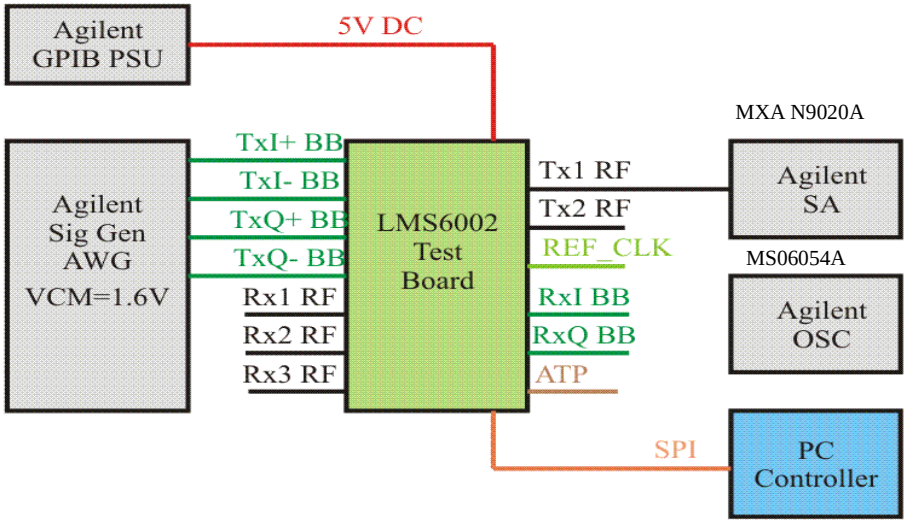


Figure 85 Transmitter test setup

9.3 Receive Test System Connections

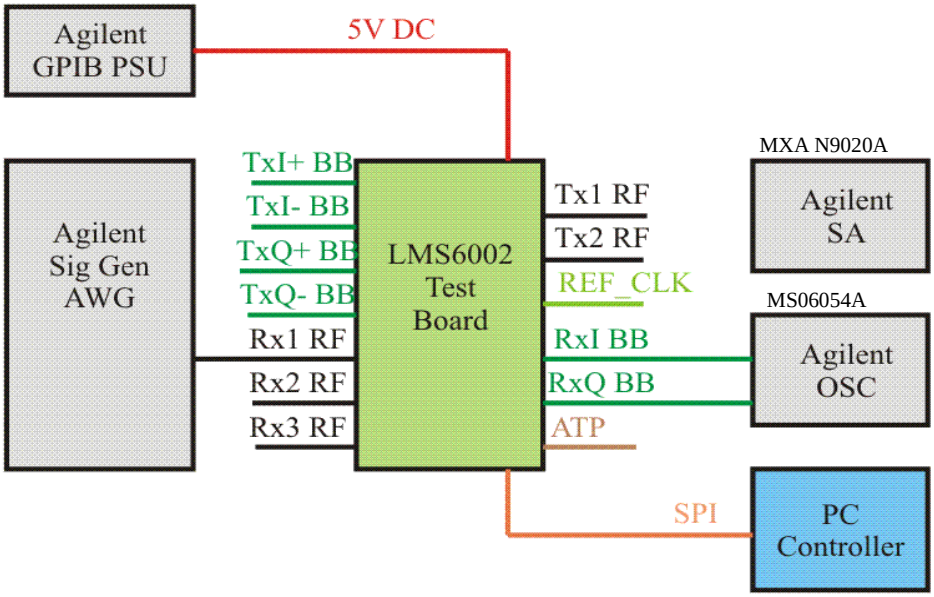


Figure 86 Receiver test setup

10

Appendix D – Signal Generator Setup

This manual uses the Agilent N5182A MXG signal generator with an arbitrary waveform generator and the differential I/Q outputs option (1EL). Other signal generators can be used. However, some issues may arise if the options available for IQ amplitude and phase manipulation which come with the MXG are not supported.

10.1 Agilent MXG Setup

The front panel of the MXG is as follows:

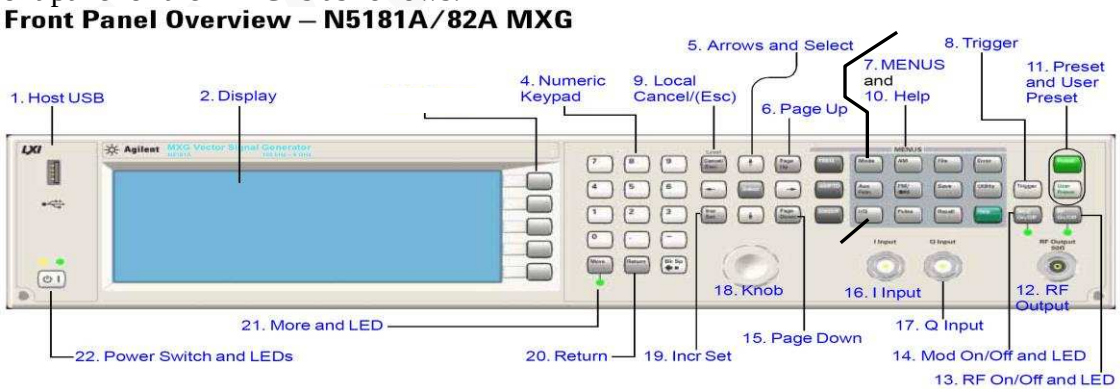


Figure 87 Agilent N5181A/82A MXG Front Panel

Step 1 – Apply 0.6V common mode offset on IQ outputs

LMS6002D Analog inputs require a 0.6V common mode offset voltage with a 300 mVp-p voltage swing for optimum performance.

To apply common m ode offset voltage:

2. Press 'IQ' button (24)
3. Press 'IQ offsets (on/off)' softkey (3. softkey 4)
4. Press 'external output adjustments' softkey (3. softkey 4)
5. Press 'Common Mode I/Q offset' softkey (3. softkey 2)
6. type 0.6 on number pad (4), press 'V' softkey (3. softkey 1)
7. 0.6V should appear on the display next to the 'Common Mode I/Q offset' softkey
8. Press return
   i. Check text next to 'I/Q Adjustments' softkey (3. softkey 1) highlights 'off/on'
   ii. If not press 'I/Q Adjustments' softkey (3. softkey 1), highlighted section should alternate between on and off when pressed.
   iii. press return
   iv. Check text next to 'I/Q' softkey (3. softkey 1) highlights 'off/on'
   v. If not press 'I/Q' softkey (3. softkey 1), highlighted section should alternate between on and off when pressed.

There should now be a 0.6V common mode voltage on the differential IQ connections on the signal generator. This can be verified by measuring the DC level of each of the 4 differential I/Q lines with a multimeter.

Note: Very small DC offset levels in the transmit IQ path can result in LO breakthrough levels changing in the transmit chain. To eliminate or minimize this effect the following practices should be followed:

- IQ cables should be equal length.
- Once I/Q gain and phase calibration is completed, connections should not be modified.
- Cables and connections should not be moved once I/Q gain and phase calibration is completed.

In practice the LMS6002D chip will be soldered to a PCB and connected to a baseband processor so this is purely a test issue.

Step 2 – Turn on the arbitrary waveform generator

The arbitrary waveform generator will run test vectors which are downloaded to it via either Agilents 'Signal Studio' program or test vectors which can be generated independently via 'Matlab' or C.

Development kit has a number of test vector files which are used for test and calibration of the LMS6002D as follows:

- DC.wfm - DC tone for TX CW testing (clock 52MHz).
- onetone1.wfm - single tone at 1MHz offset for sideband suppression calibration/test (clock 52MHz).
- twotone.wfm - two tone signal for linearity testing for MXG and LMS6002D use MXG IQ scaling factor of 30% (clock 52MHz).
- wcdma31.wfm - TM2 WCDMA signal - use MXG IQ scaling factor of 30% (clock=15.36MHz).
- EDGE3.wfm - GSM EDGE modulated test signal - (clock=13MHz).

To download files to the signal generator follow process described in 9.2 section.

To apply the correct file

1. Press 'Mode' button (23)
2. Press 'Dual Arb' softkey (3. softkey 1)
3. Press 'Select waveform' softkey (3. softkey 2)
4. Use up/down arrows (5) or spin knob (18) to select wanted waveform from list.
5. Press 'Select waveform' softkey (3. softkey 1)
6. Name of selected waveform should now be present in display window
7. Soft key list should have moved up one level back to 'Arb'
8. Now change the Arb clock frequency
9. Press 'Arb setup' softkey (3. softkey 3)
10. Press 'Arb sample clock' softkey (3. softkey 1)
11. Type in required frequency on number pad eg for 13MHz type '13' and press 'MHz' softkey (3. softkey 2)
12. Sample clock frequency should now be displayed on the screen.
13. Now scale waveform data if necessary
14. Go to 'Arb' softkey menu
    a. Either press 'return' button from 'Arb setup' menu or
    b. Press 'Mode' button then 'Dual Arb softkey (3. softkey 1)
15. Press 'More' button (21)
16. Press 'Waveform Utilities' softkey (3. softkey 2)
17. Use up/down arrows (5) or spin wheel to highlight wanted waveform from list.
18. Press 'scale waveform data' softkey (3. softkey 2)

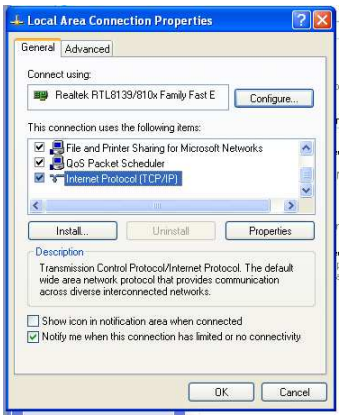
19. Type in required scaling factor e.g.25%, type ’25’ on number pad and press ‘%’ softkey (3. softkey 1).
    Note – even if text next to ‘scaling’ softkey already states 25% (for example) this does not mean it has been applied to the waveform, still follow process.
20. Press ‘Apply to waveform’ softkey (3. softkey 4)
21. Progress bar will show on screen, soft menu will return to level up (Arb utilities).
22. Now return to main ‘Arb’ Menu
    a. Press ‘return’ button twice or
    b. Press ‘Mode’ button then ‘Dual Arb softkey (3. softkey 1)
23. Check Arb in enabled
    a.‘Arb on/off’ softkey (3. softkey 1) text should have on highlighted ‘Off / On’
    b. If not press ‘Arb on/off’ softkey (3. softkey 1) to toggle between on and off.
24. Modulation can be also toggled on and off by the ‘Mod on/off’ button (just above the RF o/p connector). This must also be on – green LED must be illuminated.
    a. Press ‘Mod on/off’ button to toggle modulation on and off.
    Note – Mod on/off button turns modulation on to RF output and IQ output simultaneously. RF does not need to be on for IQ outputs to work

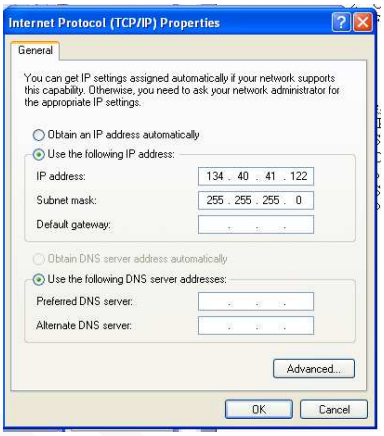
10.2 Downloading *.wfm Files to the Signal Generator

The following process should allow you to download files to the Agilent signal generator. The same process works for MXG and ESG.

This can be done via a network, however these instructions assume a direct connection between a PC running windows XP and the signal generator.

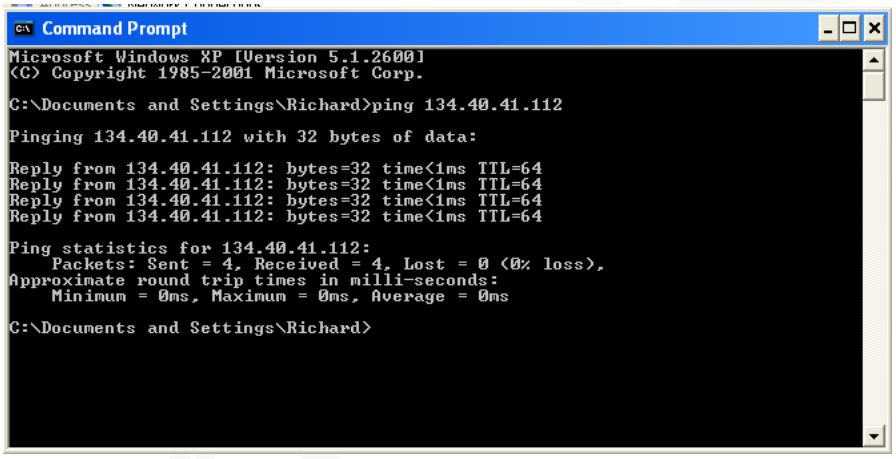
- Connect a cable between PC network port and signal generator LAN port.
- Check LEDs are illuminated on both ends to indicate HW is connected.
- Find IP address of Signal generator
  - Press ‘Utility’ button
  - Press ‘I/O config’ softkey (3. softkey 1)
  - Press ‘LAN setup’ softkey (3. softkey 2)
  - IP address should now be displayed on screen
  - e.g.
    IP Address : 134.40.41.112
    Subnet Mask : 255.255.255.0
- On PC open the ‘Local Area Connection Properties’ box
  - Select Internet Protocol (TCP/IP)
  - Press ‘Properties button
  - Select ‘Use the following IP address’ tick box
  - Set IP address to one close to sig gen, in this case: 134.40.41.122





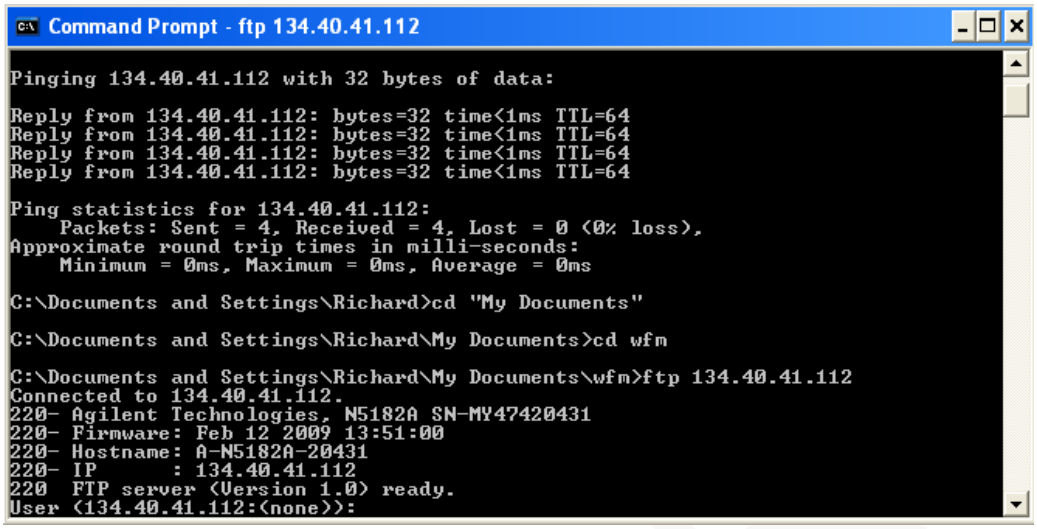
- Set subnet mask to same as sig gen, in this case 255.255.255.0
- Press ok on both open dialog boxes.

- Open a Command Prompt window
  - Start
  - All programs
  - Accessories
  - Command Prompt
- To check connection to signal generator attempt to 'ping' it
  - Type 'ping 134.40.41.112' (or use your sig gen IP address)
- A successful ping result should be returned as shown below.

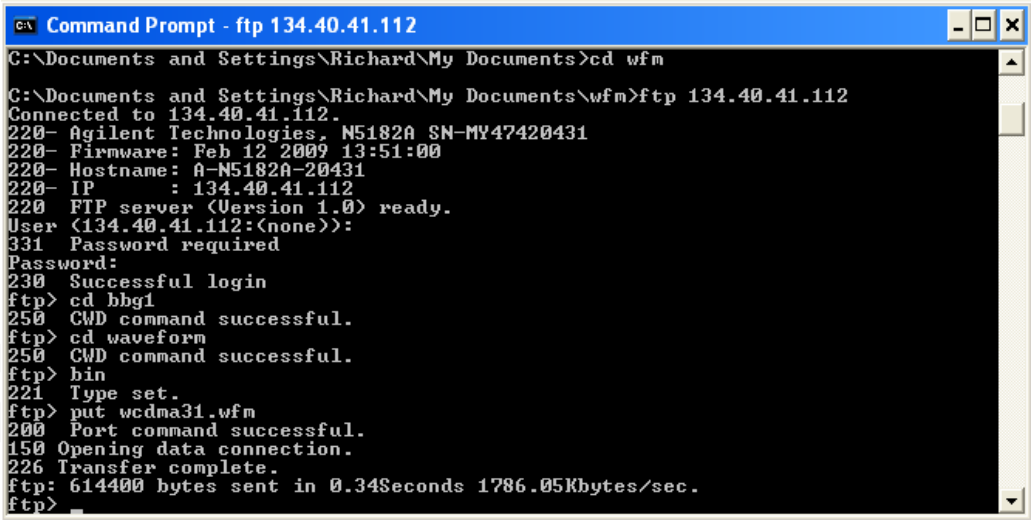


To send wfm files to signal generator the following procedure should be followed.

- Ensure wfm files are in a known directory e.g. 'C:\Documents and Settings\User\My Documents\wfm'.
- In 'Command Prompt' window set directory to the one where the wfm files are located.
- Use FTP to send files to sig gen
- Type 'ftp 134.40.41.112'



- If you are correctly connected the above should be returned.
- Press ‘return’ twice (for user name and password – none needed)
- Type ‘cd bbg1’
- Type ‘cd waveform’
- Type ‘bin’
- Type ‘put wcdma31.wfm’
- Applied command copies files to sig gen – repeat ‘put’ command for all files needed.



- To exit the ftp program type “bye”.
- To close ‘Command Prompt’ window type exit.
- The wfm files should now be visible in the list of Arb files.