

Marvell Xelerated X11 Family of Network Processors

with integrated Ethernet MACs



PRODUCT OVERVIEW

Based on the highly efficient Dataflow Architecture, the Marvell® Xelerated® X11 brings high function, low cost network processors (NPUs) to Metro Ethernet and Unified Fiber Access systems. With 24 embedded Ethernet MACs for GE or FE coupled with packaged Metro Ethernet data plane software, it provides the efficiency and feature density of fixed-function Ethernet switches while enabling feature differentiation and enhancements through programmability.

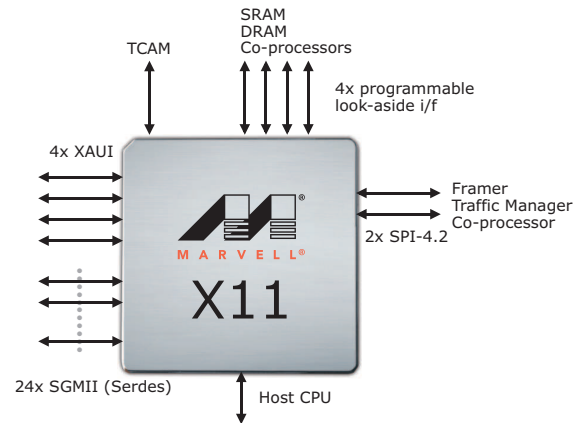
The X11 family of NPUs comes with internal TCAM and SRAM memories as well as high bandwidth to external memories for large-size forwarding and flexible classification tables.

The X11 NPU family is designed for wirespeed 20Gbps duplex Ethernet or 10G duplex Sonet/SDH line cards using a single chip.

PRODUCT OPTIONS

	Packet Processing	SPI-4.2 i/f	GE i/f	10GE i/f
X11-d240t	40 Gbps 60 Mpps	2	24	4

The X11 NPU supports 40 Gbps and a range of 10GE and GE interfaces.



The X11 NPU integrates 10GE and GE Ethernet MACs and comes with integrated memory. It can also use external memories for scaling tables in TCAM, SRAM and DRAM. Support for SPI-4.2 enables high-speed connection to third party traffic managers, custom fabrics and to Sonet/SDH framer.

ARCHITECTURE ADVANTAGES

All Marvell network processors are based on the same pipelined, programmable Dataflow Architecture. The architecture is Wirespeed by Design, cutting out time-consuming performance optimization required in competing products. The Dataflow Architecture set new industry benchmarks in terms of number of processor cores enabling rich service density with wirespeed guarantees. For system vendors, this translates to greater support for existing metro standards as well as headroom to add future features, significantly extending product life-times.

The Programmable Pipeline is a linear array of PISC (Packet Instruction Set Computer) processor cores, forming a packet processing unit through which all packets flow. A PISC is a network optimized processor core which operates on packets as they flow through the pipeline. In addition, the programmable pipeline features Engine Access Points (EAP) performing the function of I/O processors, interconnecting the pipeline with several powerful on-chip engines. These engines execute key tasks such as classification, metering, statistics counting and load balancing. Access to external DRAM, SRAM or TCAM is also performed by EAPs, enabling many and flexible lookups per packet.

The Dataflow Architecture eliminates contention for internal resources, which guarantees that packets can advance to the next processor of the pipeline (or stage in the EAP FIFO) each clock cycle, resulting in fully synchronous processing and deterministic operation.

TARGET SYSTEMS

- Carrier Ethernet Switch-Routers (CESR)
- Metro Aggregation and Transport Systems
- OLT and Point-to-point Ethernet Fiber Access Switches

PROGRAMMING AND SOFTWARE

Programming the device is simple. The intuitive sequential single threaded model is identical to the model used for programming standard general-purpose CPUs. There are no synchronization issues or complex inter-processor communication challenges as found in multicore architectures. The network processors share data structures in ANSI C with the control plane, eliminating the hassle of data types conversion.

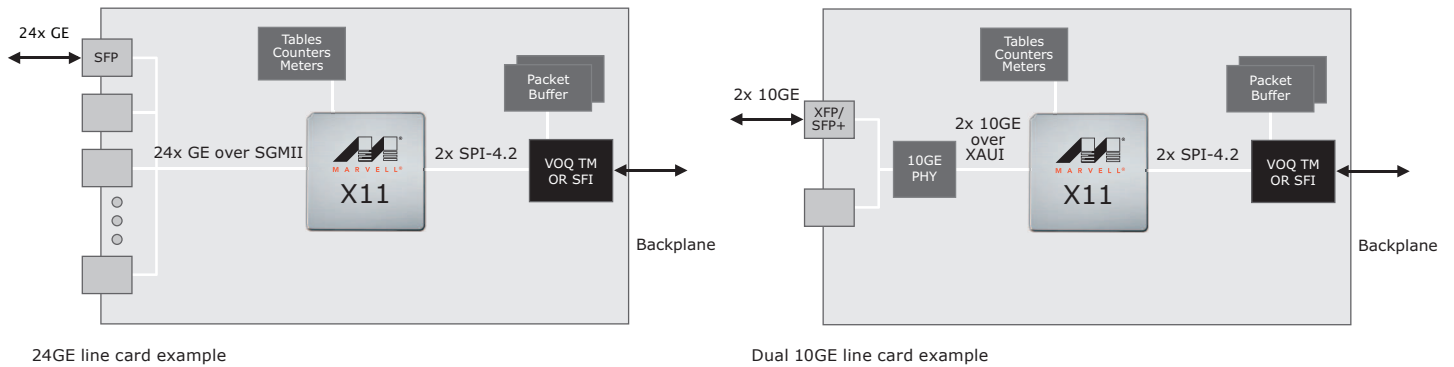
Marvell offers a full featured Metro Ethernet data plane software package for the X11 family of processors. This software can be used as a basis for customization to system vendor specific requirements.

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▶ KEY FEATURES AND BENEFITS

SPECIAL FEATURES	BENEFITS
Processing and Switching Performance	
<ul style="list-style-type: none"> 40 Gbps and 60 Mpps of wirespeed programmable packet processing 	<ul style="list-style-type: none"> Guaranteed wirespeed forwarding for a full carrier feature set at 40 Gbps
Classification and Lookup	
<ul style="list-style-type: none"> Internal TCAM and SRAM engines External programmable TCAM, SRAM and DRAM Look-aside engines Hash engine Memory protection and in-service maintenance Programmable statistics 	<ul style="list-style-type: none"> High number of classifications per packet, cost-effective for small tables Scalable number of counters and meters per packet Effective search lookup in MAC tables, flexible load balancing Carrier-grade availability Flexible and future adjustable session type metering and counting
Interfaces	
<ul style="list-style-type: none"> Triple-speed GE ports supporting SGMII 100/1000BASE-X fiber interfaces 10GE ports supporting XAUI with proprietary framing or preamble SPI-4.2 interfaces for framers and traffic managers 	<ul style="list-style-type: none"> No need for external GE MAC No need for external opto phy for GE configurations No need for external 10G MAC. Use of proprietary XAUI fabric formats Easy integration to custom or third party fabrics
OAM	
<ul style="list-style-type: none"> 802.1ag and Y.1731 link and performance monitoring Programmable Dataflow OAM tasks 	<ul style="list-style-type: none"> Continuity checks issued, received and checked by forwarding plane, enabling CPU offload Deterministic OAM processing and flexible session definitions, state tracking and reporting
Technology	
<ul style="list-style-type: none"> 130 nm CMOS technology 	

▶ SOLUTION EXAMPLES



THE MARVELL ADVANTAGE: Marvell chipsets come with complete reference designs which include board layout designs, software, manufacturing diagnostic tools, documentation, and other items to assist customers with product evaluation and production. Marvell's worldwide field application engineers collaborate closely with end customers to develop and deliver new leading-edge products for quick time-to-market. Marvell utilizes world-leading semiconductor foundry and packaging services to reliably deliver high-volume and low-cost total solutions.

ABOUT MARVELL: Marvell is a leader in storage, communications, and consumer silicon solutions. Marvell's diverse product portfolio includes switching, transceiver, communications controller, processor, wireless, power management, and storage solutions that power the entire communications infrastructure, including enterprise, metro, home, storage, and digital entertainment solutions. For more information, visit our Web site at www.marvell.com.



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