

# BUK761R8-30C

N-channel TrenchMOS standard level FET

Rev. 02 — 20 August 2007

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package, using NXP Ultra High-Performance (UHP) automotive TrenchMOS technology.

### 1.2 Features

- 175 °C rated
- Standard level compatible
- Q101 compliant
- TrenchMOS technology

### 1.3 Applications

- 12 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference

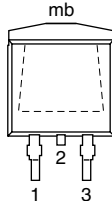
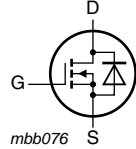
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a>	[1][2] -	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	333	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	1.5	1.8	mΩ
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$	-	-	1.7	J

[1] Refer to document 9397 750 12572 for further information.

[2] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning**

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	G	gate	 <p style="text-align: center;">SOT404 (D2PAK)</p>	 <p style="text-align: center;">mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK761R8-30C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

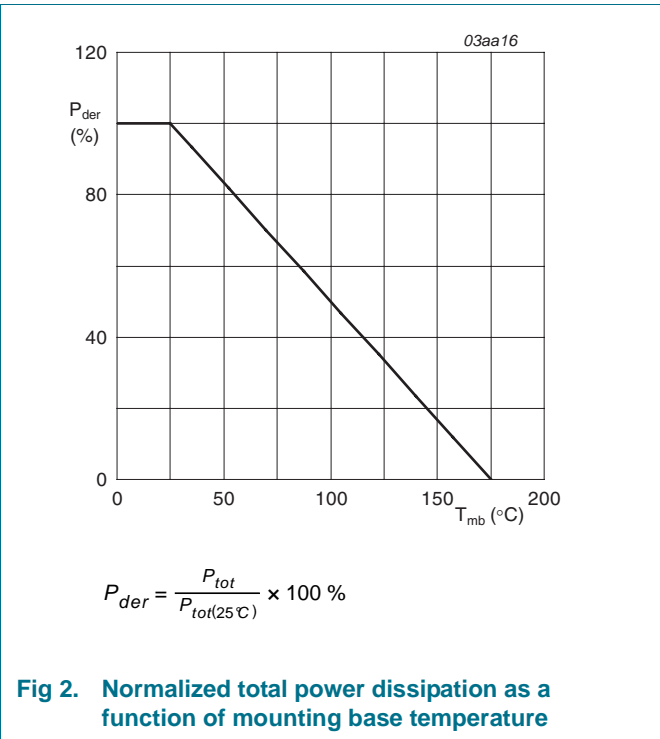
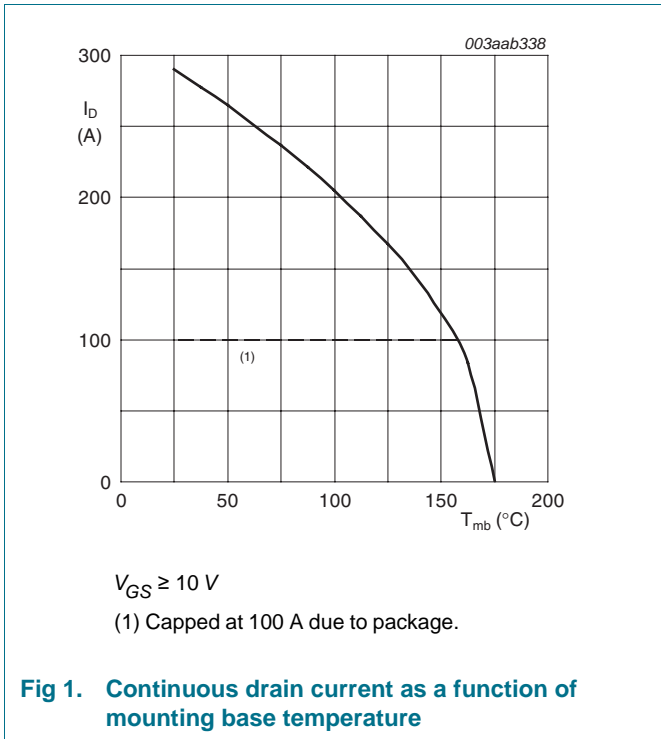
## 4. Limiting values

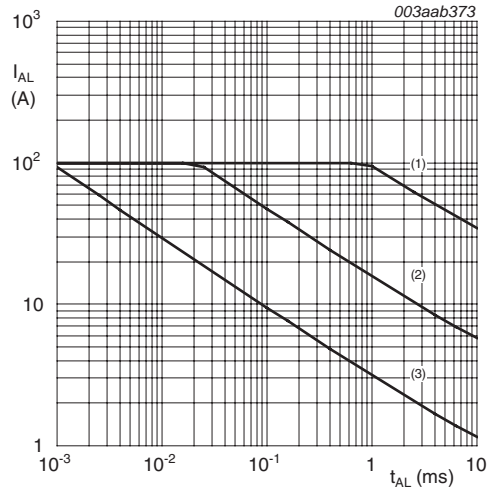
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage		-	30	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	30	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$T_{mb} = 100\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a> <a href="#">[1][2]</a>	-	100	A	
		$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a> <a href="#">[1][2]</a>	-	100	A	
		$T_{mb} = 25\text{ }^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">4</a> <a href="#">[1][3]</a>	-	312	A	
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 4</a>	-	1249	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	333	W	
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$	
$T_j$	junction temperature		-55	175	$^\circ\text{C}$	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^\circ\text{C}$	-	1.7	J	
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 3</a>	<a href="#">[4][5]</a> <a href="#">[6][7]</a>	-	J	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ }^\circ\text{C}$	<a href="#">[1][3]</a>	-	312	A
		$T_{mb} = 25\text{ }^\circ\text{C}$	<a href="#">[1][2]</a>	-	100	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ }^\circ\text{C}$	-	1249	A	

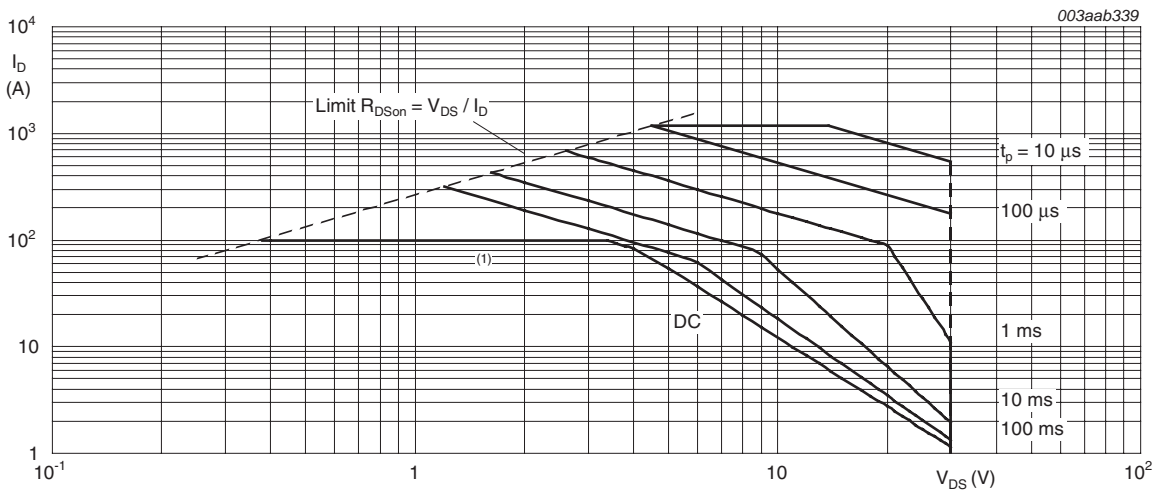
- [1] Refer to document 9397 750 12572 for further information.
- [2] Continuous current is limited by package.
- [3] Current is limited by chip power dissipation rating.
- [4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.
- [7] Refer to application note AN10273 for further information.





- (1) Single-pulse;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .
- (2) Single-pulse;  $T_{mb} = 150\text{ }^{\circ}\text{C}$ .
- (3) Repetitive.

**Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time**



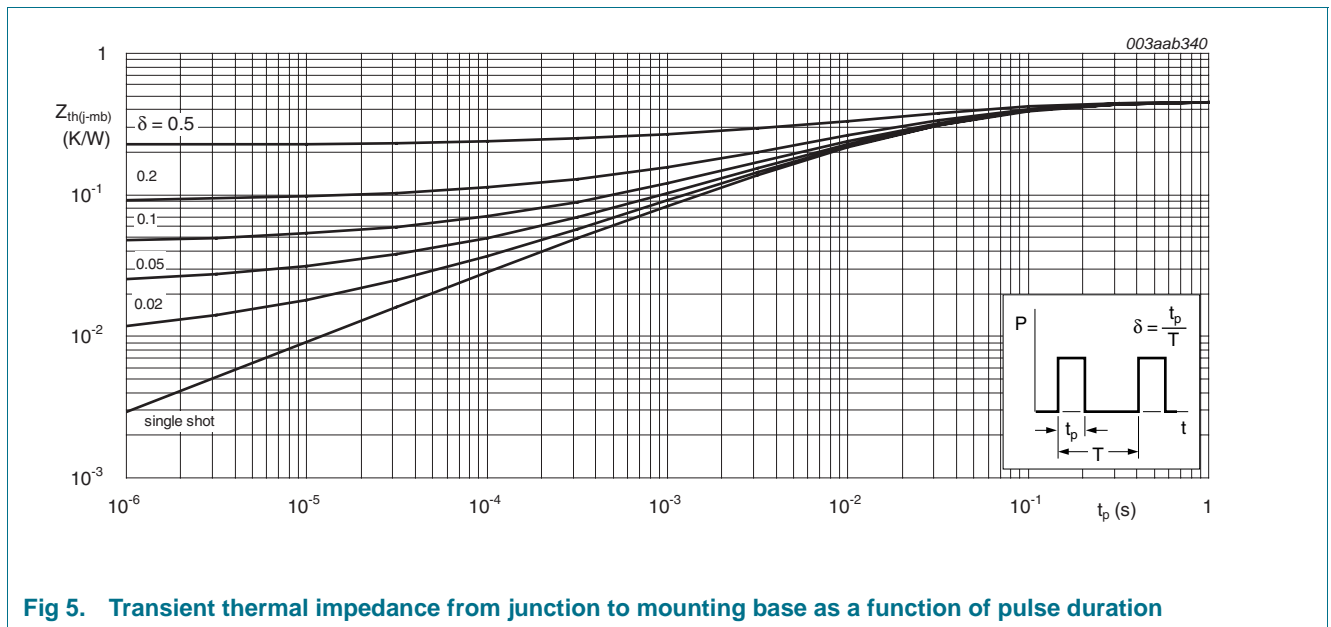
- $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{DM}$  is single pulse
- (1) Capped at 100 A due to package.

**Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; minimum footprint	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	-	0.45	K/W



**Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 6. Characteristics**

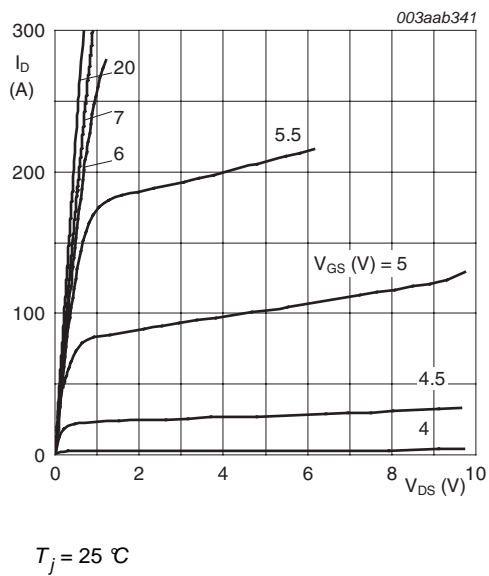
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	-	-	4.4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> and <a href="#">10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> and <a href="#">10</a>	2	3	4	V

**Table 6. Characteristics ...continued**

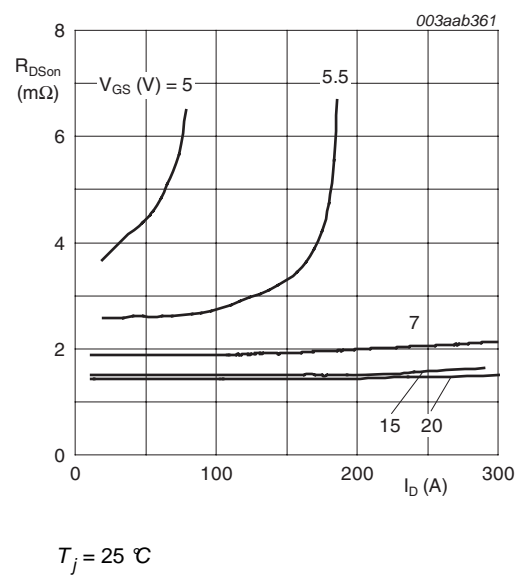
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
		V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 20 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>DS</sub> = 0 V; V <sub>GS</sub> = -20 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	-	3.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	1.5	1.8	mΩ
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 16</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V	-	73	-	ns
Q <sub>r</sub>	recovered charge	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V	-	48	-	nC
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 10 V; see <a href="#">Figure 14</a>	-	150	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 10 V; see <a href="#">Figure 14</a>	-	36	-	nC
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 10 V; see <a href="#">Figure 14</a>	-	52	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; see <a href="#">Figure 14</a>	-	5	-	V
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 15</a>	-	7762	10349	pF
C <sub>oss</sub>	output capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 15</a>	-	1807	2168	pF
C <sub>rss</sub>	reverse transfer capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 15</a>	-	996	1365	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 25 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω	-	52	-	ns
t <sub>r</sub>	rise time	V <sub>DS</sub> = 25 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω	-	110	-	ns
t <sub>d(off)</sub>	turn-off delay time	V <sub>DS</sub> = 25 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω	-	186	-	ns

**Table 6. Characteristics ...continued**

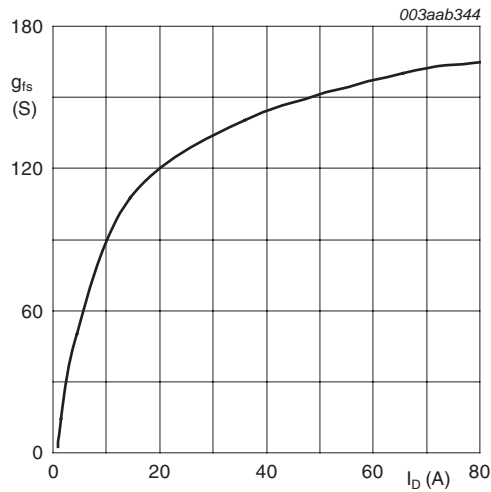
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_f$	fall time	$V_{DS} = 25\text{ V}; R_L = 1.2\ \Omega;$ $V_{GS} = 10\text{ V}; R_{G(ext)} = 10\ \Omega$	-	134	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to center of die	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH



**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**

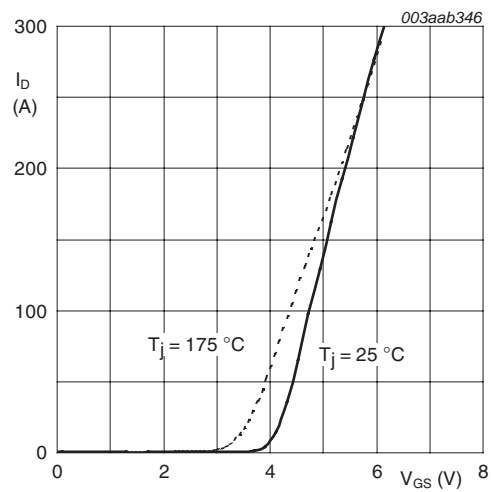


**Fig 7. Drain-source on-state resistance as a function of drain current; typical values**



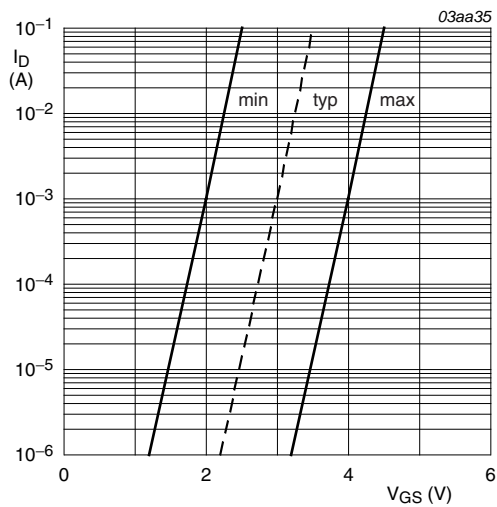
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

**Fig 8. Forward transconductance as a function of drain current; typical values**



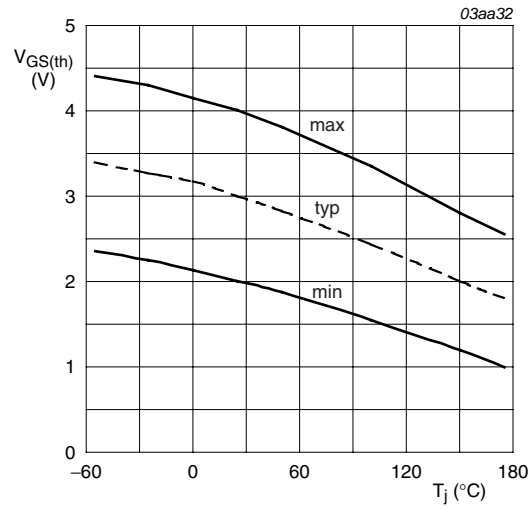
$V_{DS} = 25\text{ V}$

**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



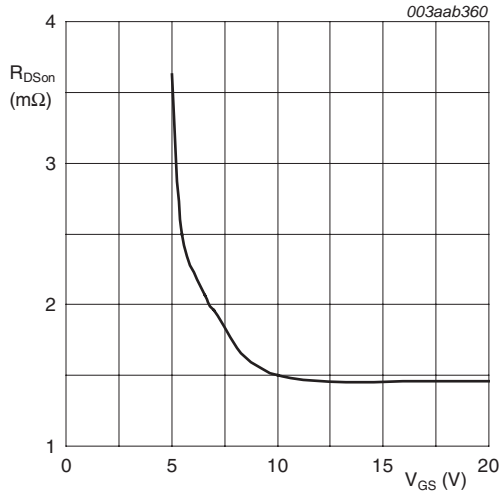
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**



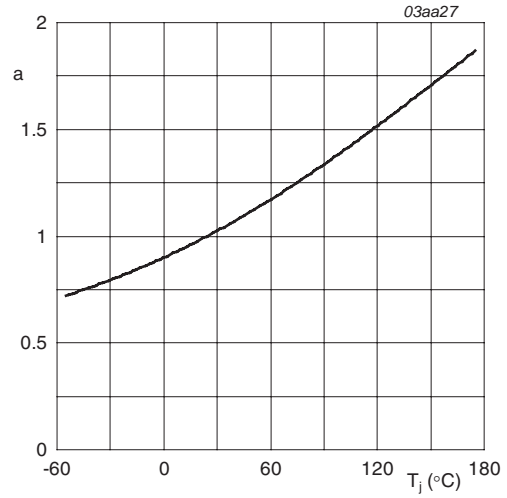
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



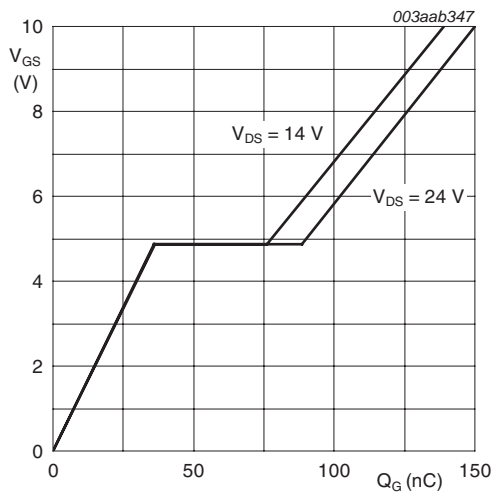
$T_j = 25\text{ °C}; I_D = 25\text{ A}$

**Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values**



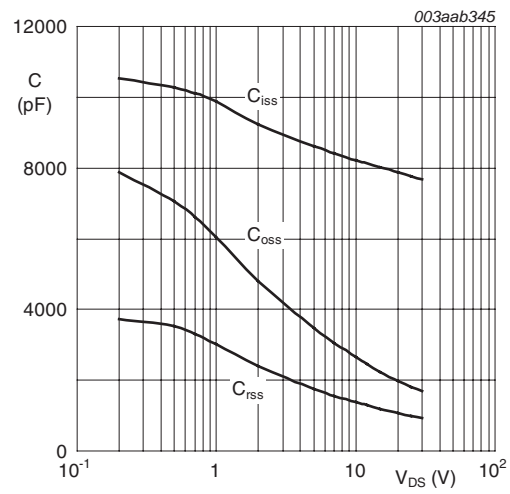
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**



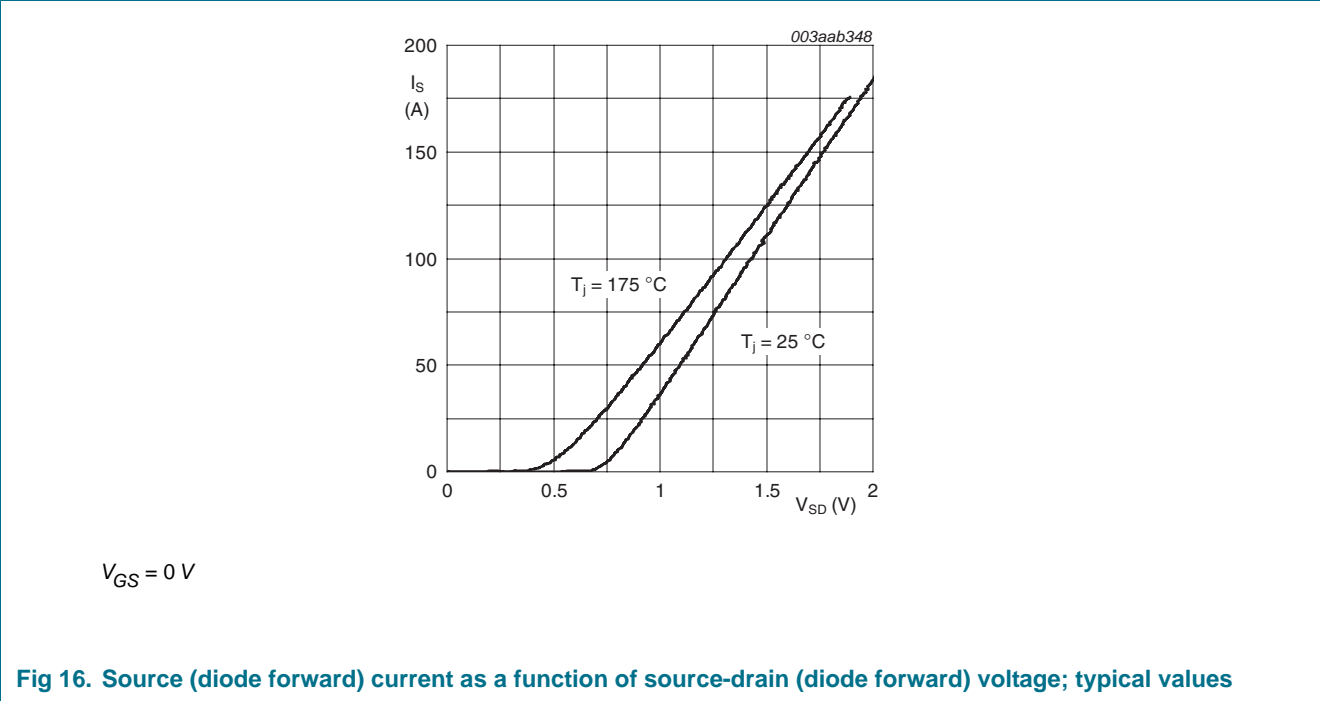
$T_j = 25\text{ °C}; I_D = 25\text{ A}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

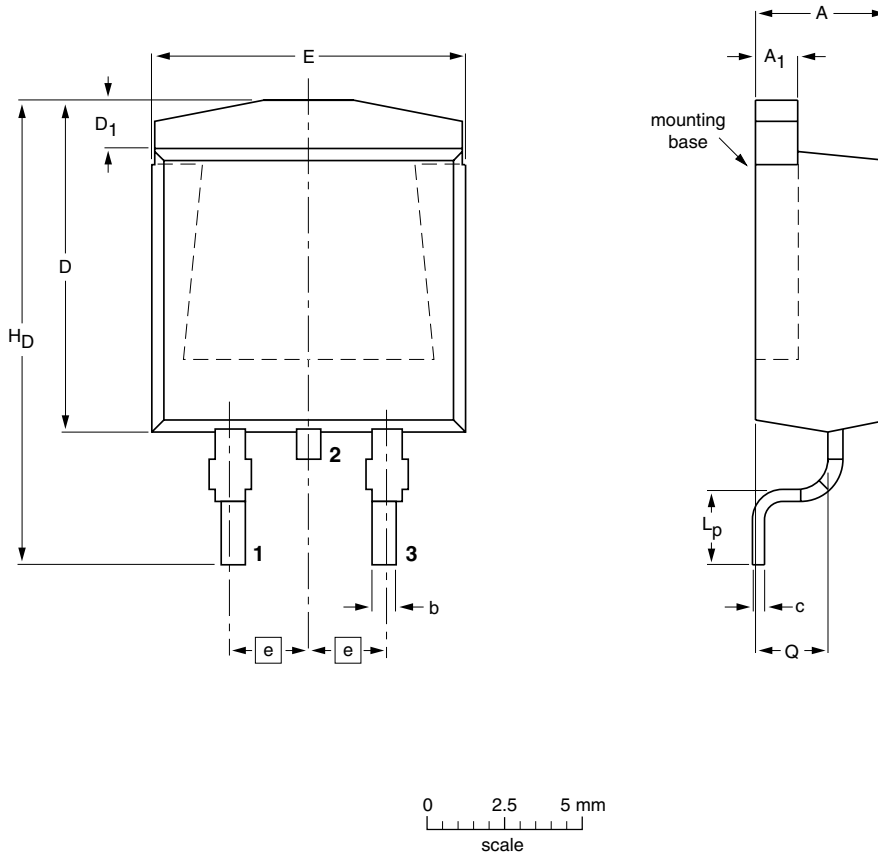
**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404**



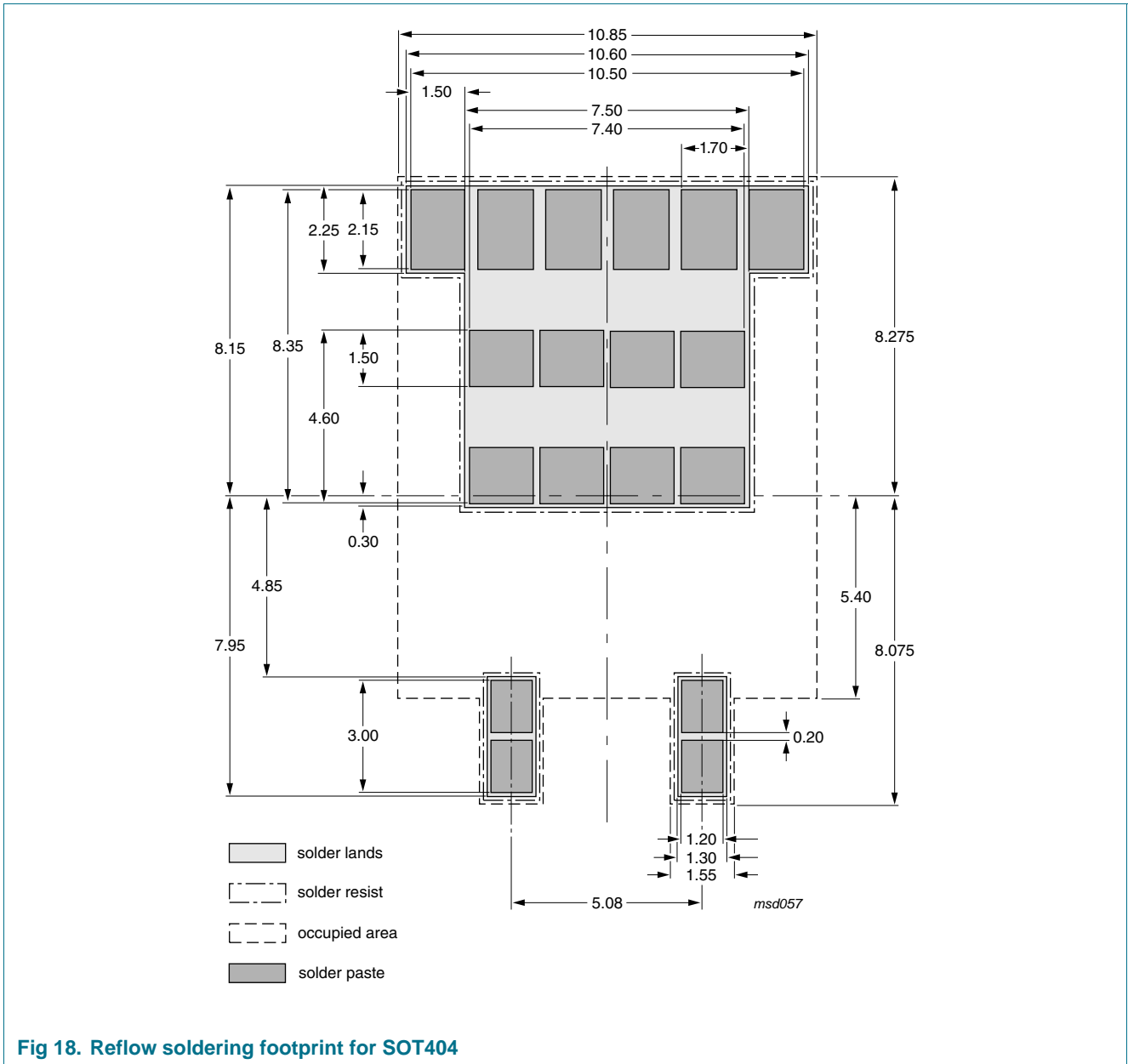
**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub>	b	c	D <sub>max.</sub>	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50	1.40	0.85	0.64	11	1.60	10.30	2.54	2.90	15.80	2.60
	4.10	1.27	0.60	0.46		1.20	9.70		2.10	14.80	2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

**Fig 17. Package outline SOT404 (D2PAK)**

## 8. Soldering



## 9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK761R8-30C_2	20070820	Product data sheet	-	BUK761R8-30C_1
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>		
BUK761R8-30C_1	20060725	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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