

## DIGITAL LOCK FOR AUTOMOTIVE IGNITIONS

January 2003

### FEATURES:

- 5040 Four-Digit Combinations (for a 10 digit Keypad)
- Combinations are Hard-Wire Programmed
- Sense Input Enables Operation
- Save Memory Feature for Valet Parking
- Convenience Delay Controlled by External Capacitor
- Static or Momentary Lock Control Output
- Save Memory and Lock Status Outputs
- +5V to +18V Operation (Vss - VDD)
- LS7220 (DIP), LS7220-S (SOIC) - See Figure 1

### DESCRIPTION:

The LS7220 is a MOS digital lock circuit. When wired to a ten-digit keypad, the circuit will recognize one four-digit combination out of a possible 5040 combinations.

The LS7220 is configured with the features required for an Automotive Ignition Anti-Theft Digital Lock (See Figure 5). These features include Sense input which enables the IC, Save Memory for Valet Parking, Convenience Delay to maintain Unlock condition for short term interruptions of the Sense input and Save Status and Lock Status outputs which can be used for direct drive of LED indicators.

### OPERATING DESCRIPTION: (Refer to Figures 2, 3, 4 and 5.)

When the Sense input goes high, the LS7220 is enabled. The Lock Status output turns on and Save Status and LOCK outputs remain off. When the programmed four-digit combination is entered from the keypad, in proper sequence, LOCK turns on and Lock Status turns off. If the Sense input is interrupted for a period of time greater than the Convenience Delay, the operating sequence must start over. If the Sense input is interrupted for a period of time less than the Convenience Delay, the operation of the LS7220 is unaffected. A momentary high at the Save input sets the Save Memory and causes the LS7220 to save an Unlock condition (Sequential Memory is set) for any time duration interruption of the Sense input (i.e., valet parking). The Save Status output turns on when Save Memory is set. The Lock input is used to reset the Save Memory and return the LS7220 to normal operation.

**NOTE:** Using a 3 x 4 keypad, the \* key can be connected to the Lock input and the # key to the Save input. Lock Status and Save Status outputs can be used to drive red and green LED indicators, respectively.

### INPUT/OUTPUT DESCRIPTION: (Refer to Figure 4)

#### SENSE INPUT (Pin 1)

A high at this input causes CONVENIENCE DELAY to transition high and enables recognition of the SELECTED KEYS when they are inputted in proper sequence. Control logic for LOCK, LOCK STATUS and SAVE STATUS outputs is also enabled. A low at this input keeps all outputs off and resets the Sequential Memory if Save Memory is not set.

**VDD** (Pin 9) Supply voltage negative terminal.

**Vss** (Pin 14) Supply voltage positive terminal.

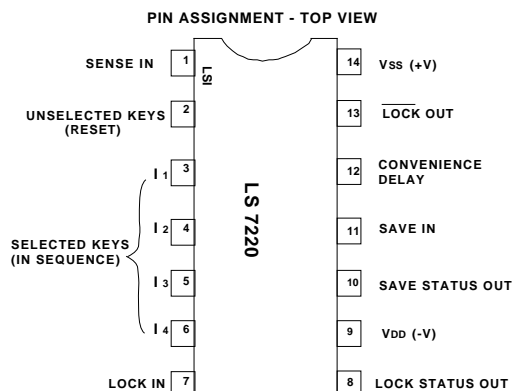


FIGURE 1.

#### UNSELECTED KEYS (RESET) INPUT (Pin 2)

A high at this input resets the Sequential Detector for the SELECTED KEYS inputs. This input must be wired to all digit keys which are not part of the Four-Digit Combination.

#### SELECTED KEYS INPUTS (Pins 3, 4, 5, 6)

When these inputs are brought high in correct sequence, (i.e., I1, I2, I3, I4) the Sequential Memory is set if SENSE input is high. LOCK output turns on and LOCK STATUS output turns off when the Sequential Memory is set.

#### LOCK INPUT (Pin 7)

A high at this input resets the Save Memory. The SAVE STATUS output turns off when this occurs.

#### LOCK STATUS OUTPUT (Pin 8)

This output is the complement of LOCK output when the SENSE input is high. See NOTE.

#### SAVE STATUS OUTPUT (Pin 10)

This output turns on when Save Memory is set and SENSE input is high. See NOTE.

#### SAVE INPUT (Pin 11)

A high at this input sets the Save Memory. If Save Memory is set and Sequential Memory is set, the Save Memory will prevent the Sequential Memory from being reset as a result of a change at the SENSE input. (See SAVE STATUS OUTPUT.)

#### CONVENIENCE DELAY I/O (Pin 12)

An external capacitor placed on this pin will delay the effect of changes at the SENSE Input from affecting the outputs and the condition of the Sequential Detector and Sequential Memory. (See Figure 2)

#### LOCK OUTPUT (Pin 13)

This output turns on when the Sequential Memory is set and SENSE input is high. See NOTE.

**NOTE:** Outputs are off when SENSE input is low.

**ABSOLUTE MAXIMUM RATINGS:**

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	VSS - VDD	+20	V
Any Input Voltage	VIN	VSS - 20 to VSS + 0.5	V
Operating Temperature	TA	-25 to +85	°C
Storage Temperature	TSTG	-65 to +150	°C

**TRANSIENT CHARACTERISTICS:** (See Figure 3)  
(TA = -25°C to +85°C, VSS = +5V to +18V)

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
SENSE High Delay to Outputs Enabled	TSE	-	1	µs	No external capacitor, Pin 12
SENSE Low Delay to Outputs Disabled	TSD	-	10	µs	No external capacitor, Pin 12
Input Pulse Widths (except SENSE)	TPW	25	-	µs	-
Valid Combination Entry to <u>LOCK</u> Output Enabled	TCE	-	10	µs	SENSE High

**DC ELECTRICAL CHARACTERISTICS:**

(All voltages referenced to VDD; TA = -25°C to +85°C unless otherwise specified.)

**Vss voltages = 5V, 9V, 12V, 15V, 18V**

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
Supply Voltage	VSS	+5	+18	V	-
Supply Current	ISS	-	20, 30, 40, 50, 70	µA	Vss voltages
<b>*INPUT VOLTAGES:</b>					
SENSE Low	VIL	0	2, 3, 4, 6, 8.5	V	Vss voltages
SENSE High	VIH	3.5, 5.5, 6.5, 9, 11.5	Vss	V	Vss voltages
CONVENIENCE DELAY Low	VIL	-	0.3Vss	-	Typical
CONVENIENCE DELAY High	VIH	0.7Vss	-	-	Typical
All Other Inputs:					
Low	VIL	0	Vss - 3	V	-
High	VIH	Vss - 1	Vss	V	-

**\*NOTE 1:** All inputs have pull down resistors to VDD. Typical input sink current is 12µA with input at Vss (Vss - VDD = +12V)**OUTPUT CURRENT:**

*** <u>LOCK</u> STATUS Source Current Vo = +1.7V	Io	0.4, 2.5, 5, 9, 14	1.3, 6, 12, 20, **30	mA	Vss voltages
*** <u>SAVE</u> STATUS Source Current Vo = +1.7V	Io	0.8, 5, 10, 18, 28	2.6, 12, 24, **30, **30	mA	Vss voltages
CONVENIENCE DELAY	Io	0.1, 0.5, 0.7, 1, 1.2	0.5, 1.1, 1.6, 2.1, 2.4	mA	Vss voltages
<u>LOCK</u>	Io	1.3, 6.5, 9.1, 13, 15.6	6.5, 14.7, 21, 27.3, **30	mA	Vss voltages
Inupt Capacitance	CIN	-	10	pF	-

**\*\*NOTE 2:** Limit current to 30mA maximum**\*\*\*NOTE 3:** LOCK STATUS and SAVE STATUS output currents are balanced to achieve equal brightness for red and green LEDs

FIGURE 2. CONVENIENCE DELAY TIME vs POWER SUPPLY  
(with External Capacitor C, Pin 12)

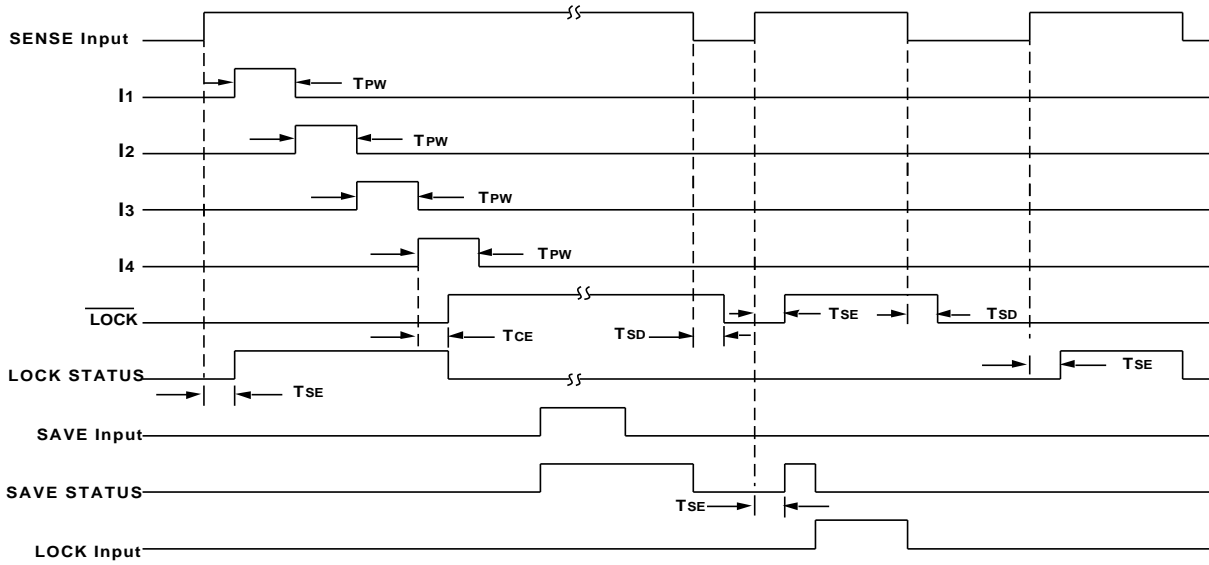
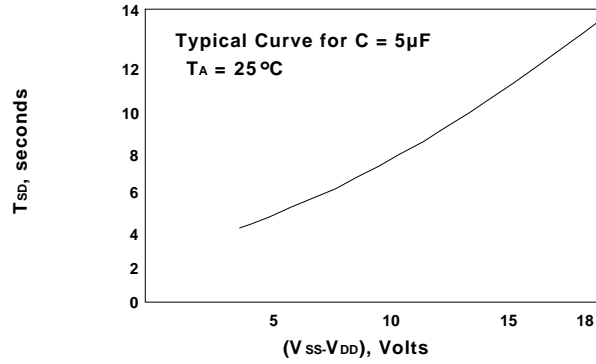


FIGURE 3. LS7220 TIMING DIAGRAM

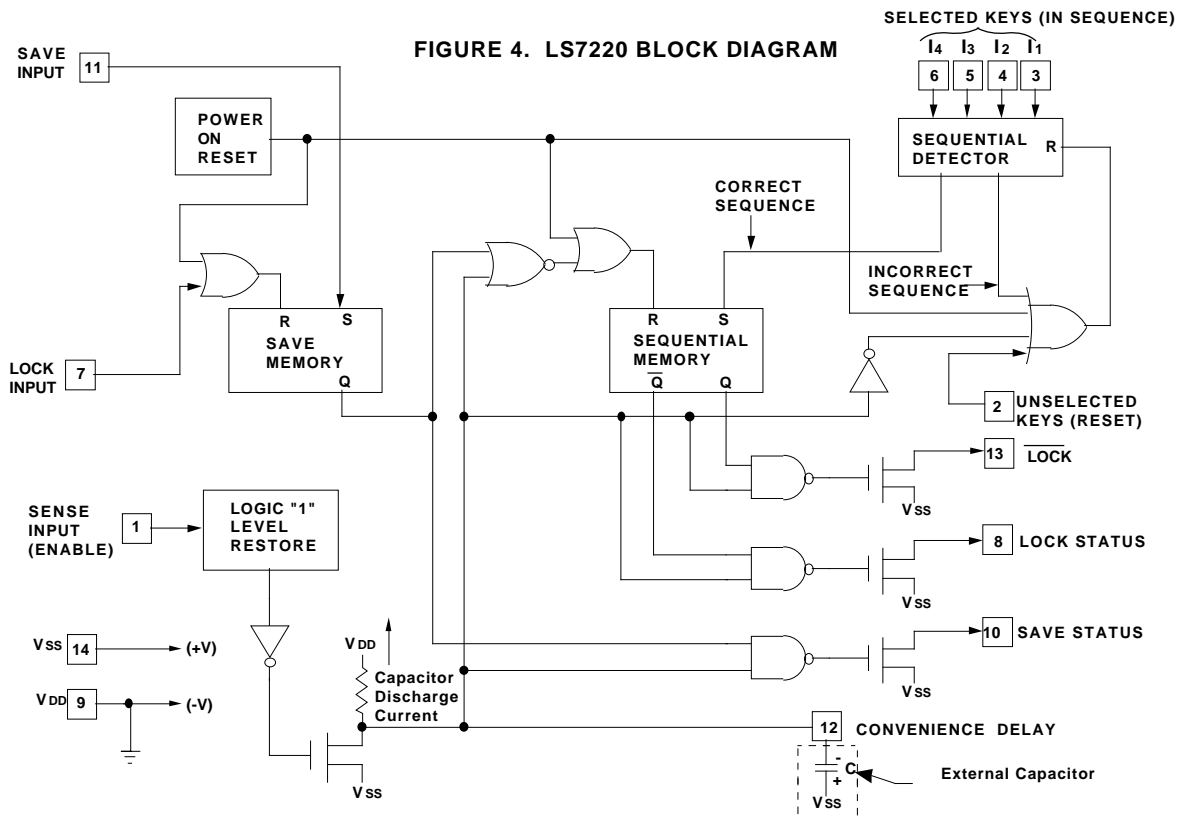
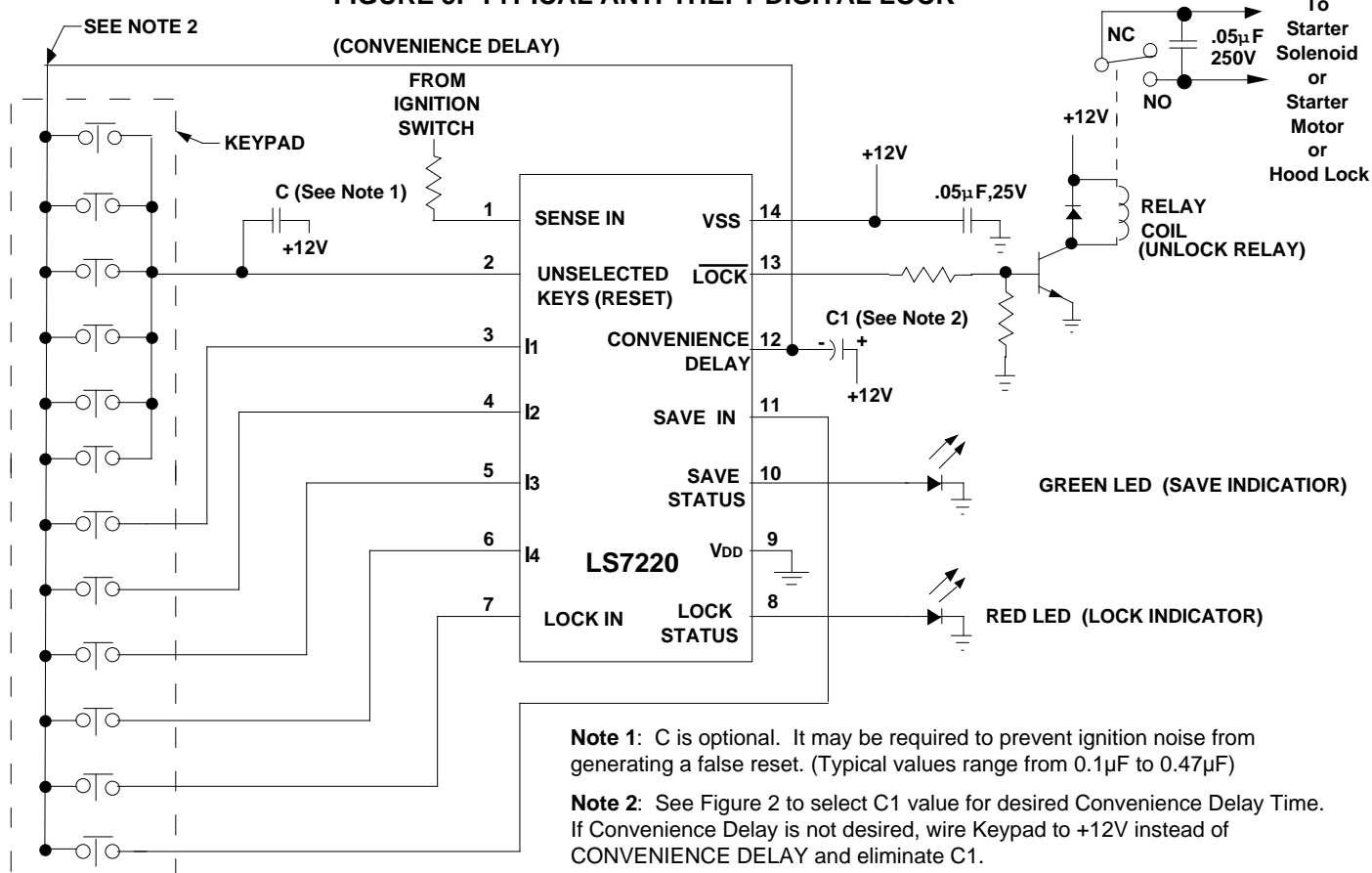


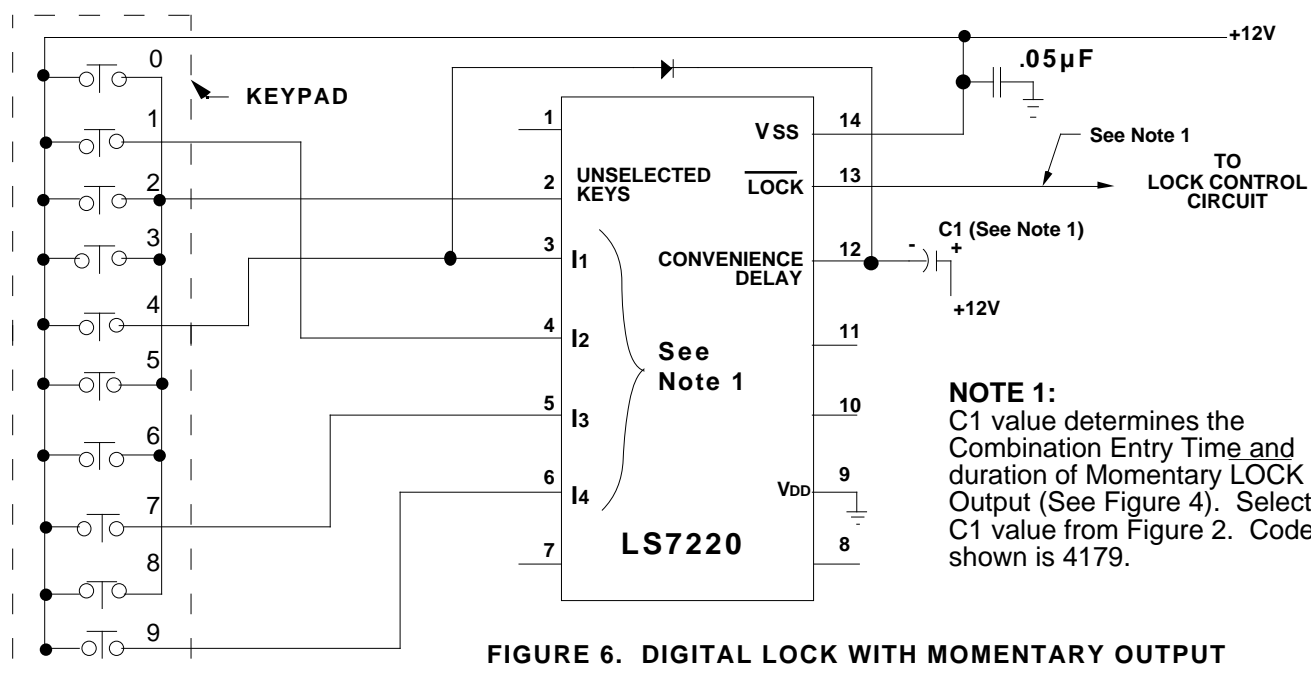
FIGURE 4. LS7220 BLOCK DIAGRAM

**FIGURE 5. TYPICAL ANTI-THEFT DIGITAL LOCK**



A typical automotive anti-theft digital lock circuit is shown in Figure 5. When the Ignition Switch is turned on the SENSE input (Pin 1) goes high and the circuit is ready to accept the unlocking input sequence at I1, I2, I3 and I4 (Pins 3, 4, 5 and 6, respectively). If the keys associated with these inputs are depressed exactly in sequence, the LOCK output (Pin 13) turns ON and the Unlock Relay is energized. This state is indicated by the OFF condition of the LOCK STATUS output (Pin 8) which turns the red LED OFF (indicates unlock condition). If the keys are depressed in any sequence other than as described above, the internal sequential detector resets and the entire sequence must be repeated (See Figure 4).

In order to save the ON condition of the LOCK output before the ignition switch is turned Off (i.e., when the SENSE input becomes low) the key associated with the SAVE input (Pin 11) has to be depressed. The "SAVE" status is indicated by a high at the SAVE STATUS output (Pin 10), which turns the green LED On. If the ignition switch is turned Off when the green LED is On, all the output status are preserved in the internal memory, so that when the ignition switch is turned on again there is no need to go through the input sequence again. This feature could be used for valet parking and garage service. Status saving may be cancelled by depressing the LOCK input key followed by turning the ignition switch Off for a time greater than the CONVENIENCE DELAY (See Figure 2). This also turns OFF the LOCK output.



**FIGURE 6. DIGITAL LOCK WITH MOMENTARY OUTPUT**