LSI/CSI

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# LS8397

# STEPPER MOTOR CONTROLLER

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**FEATURES:**

- Controls Bipolar and Unipolar Motors
- **L297** operation with ***added functions*:**
- ***Selectable torque ripple compensated phase drive***
- ***Selectable automated switching between stepping and holding torques***
- ***Supply current < 400uA***
- Half and full step modes
- Normal/wave drive
- Direction control
- Reset input
- Step control input
- Enable input
- PWM chopper circuit for current control
- Two over current sensor comparators with external references input
- All inputs and outputs TTL/CMOS compatible (TTL for 5V operation)
- 4.75V to 7V Operation ($V_{DD}$ – $V_{SS}$).
- **LS8397** (DIP), **LS8397-S** (SOIC), **LS8397-TS** (TSSOP)

**– See Figure 1 –**

**PIN ASSIGNMENT**
**TOP VIEW**

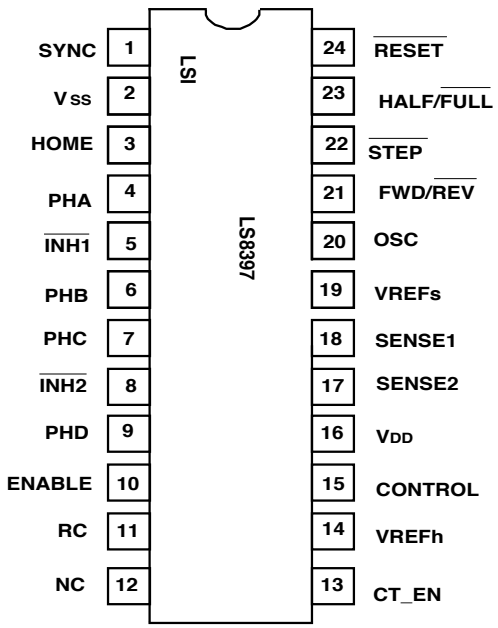



**FIGURE 1**

**DESCRIPTION:**

The **LS8397** Stepper Motor Controller generates four phase drive signal outputs for controlling two phase Bipolar and four phase Unipolar motors. The outputs are used to drive two H-bridges for the two motor windings in the Bipolar motor or the four driver transistors for the two center- tapped windings in the Unipolar motor. The motor can be driven in full step mode either in normal drive (two-phase-on) or wave drive (one-phase-on) and half step mode. The **LS8397** provides two inhibit outputs which are used to control the driver stages of each of the motor phases. The circuit uses STEP, FRD/REV and HALF/FULL inputs in a translator to generate controls for the output stages.

A dual PWM chopper circuit using an on-chip oscillator, latches and voltage comparators are used to regulate the current in the motor windings. For each pair of phase driver outputs (PHA, PHB, and PHC, PHD) each pulse of the common internal oscillator sets the latch and enables the output. If the current in the motor winding causes the voltage across a sense resistor to exceed the reference voltage, VREFs, at the comparator inputs, the latch is reset disabling the output until the next oscillator pulse.

Input for a separate reference voltage VREFh is also provided for reducing holding torque when the motor is not turning. When holding torque mode is enabled with a resistor-capacitor pair connected to the RC Pin, the sense comparator input reference switches between VREFs and VREFh depending on whether the motor is turning or not. The separate sense reference voltages allow for conserving power when the motor is not turning. Holding torque mode can be disabled by connecting the RC Pin to $V_{SS}$.

In the half-step stepping sequence, the phase drives alternate between one-phase-on and two-phase-on in successive steps at full power thus generating substantial ripple on the output torque. An input, CT_EN is provided for selecting an operational mode in which the torque ripple is corrected. In this mode the sense input reference voltage is switched to 100% and 70.7% of the applied voltages at the VREFs and VREFh inputs in successive one-phase-on and two-phase-on conditions, respectively. The CONTROL input determines whether the chopper acts on the phase driver outputs or the inhibit outputs. When the phase lines are chopped, the non-active phase line of each pair (PHA, PHB or PHC, PHD) is activated rather than deactivating the active line to reduce dissipation in the load sensing resistor Rs. Refer to Figure 5B for Bipolar motors. If PHA is high and PHB is low, current flows through Q1, motor winding, Q4 and sense resistor Rs. When chopping occurs, PHB is brought high and circulating current flows through Q1 and D3 and not through Rs resulting in less power dissipation in Rs. Current decay is slow using this method. When the Control input is brought low, chopping occurs by bringing INH1 low. In this case circulating current flows through D2, motor winding and D3 and through the power supply to ground causing the current to decay rapidly. For Unipolar motors, only inhibit chopping is used. Refer to Figure 6. When INH1 is brought low the current flowing in either half of the center tapped motor winding recirculates through the diode across it.

**INPUT/OUTPUT DESCRIPTION:**

**OSC Input**

An RC input with the resistor connected to $V_{DD}$ and the capacitor connected to ground determines the oscillator chopper rate. When connected as an oscillator, the oscillator output appears as a negative-going pulse at the Sync pin. If the oscillating pin is tied to ground, the Sync pin becomes an input.
Osc frequency, fosc = 1/0.69RC

**SYNC**
As an output the sync can be used to drive sync pins of other **LS8397**s. This eliminates the need for RC components for any other **LS8397** controllers used in the system. As an input the sync can be driven by the **LS8397** that has the RC oscillator components or by any other system external clock.

**PHA/PHB/PHC/PHD**
Phase drive output signals for power stages. In a Bipolar motor PHA and PHB are used for one H-bridge while PHC and PHD are used for the other.

**$\overline{\text{INH1}}$/$\overline{\text{INH2}}$ Outputs**
These outputs are active low inhibit controls for motor drive outputs. $\overline{\text{INH1}}$ controls driver stage using PHA and PHB signals while $\overline{\text{INH2}}$ control driver stage using PHC and PHD signals. When the Control input is low, these outputs are chopped using the internal oscillator for current regulating.

**CONTROL Input**
When high, the phase outputs, PHA, PHB, PHC and PHD are chopped. When low, $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ are chopped. Normally, inhibit outputs are chopped. Phase chopping might be used with a Bipolar motor that does not store much energy to prevent fast current decay and a low useful torque.

**ENABLE Input**
When Enable input is low, $\overline{\text{INH1}}$, $\overline{\text{INH2}}$, PHA, PHB, PHC and PHD are brought low.

**HOME Output**
An open drain output that indicates when the **LS8397** is in its initial state with PHA, PHB, PHC, PHD = logic states 0101 respectively. Refer to Figure 4. In the active state the open drain device is off.

**$\overline{\text{STEP}}$ Input**
An active low pulse on this input causes the motor to advance one step. The step occurs on the rising edge of the step signal.

**FRD/$\overline{\text{REV}}$ Input**
A logic 1 on this input causes the motor to advance through the stepping sequence of Fig. 4. A logic 0 on this input cause the motor to reverse the sequence.

**$\overline{\text{RESET}}$ Input**
An active low on this input cause the motor to be restored to the home position (0101).

**HALF/$\overline{\text{FULL}}$ Input**
When high, half-step operation is selected. When low, full-step operation is selected. The one-phase-on full step is selected by selecting full when the stepping sequence is at an even state. The two-phase-on full step operation is selected when the stepping sequence is at an odd state. Refer to Figure 4.

**SENSE1/ SENSE2 Inputs**
Inputs for load current sense voltages from power stages using PHA and PHB drive signals or PHC and PHD drive signals, respectively.

When holding-torque mode is enabled, the motor torque is switched to stepping torque at a step command followed by holding torque after a programmable delay. The stepping torque is controlled by the reference voltage VREFs input and the holding torque is controlled by the voltage at the VREFh input. The delay is controlled by a resistor-capacitor pair connected to the RC pin.

When the holding-torque mode is disabled, the motor torque remains in the stepping torque mode all the time controlled by the VREFs voltage.

**RC Input/Output**
A resistor-capacitor pair connected to this pin starts a time-out delay at every step command. At the start of the delay, the reference voltage at the VREFs pin is switched in for the SENSE comparators to produce higher stepping torque. At the end of the time-out, the reference voltage at the VREFh pin is switched in for the SENSE comparators to produce the lower holding torque, reducing power dissipation while the motor is stationary.

The delay is given by Tds = 1.4RC

If tied low, holding torque mode is disabled and stepping torque is produced in both dynamic and static states by using the VREFs reference voltage.

**VREFs Input**
Input for the SENSE comparator reference voltage for producing stepping torque.

**VREFh Input**
Input for the SENSE comparator reference voltage for producing holding torque.

**CT_EN Input**
Input for selecting/deselecting compensated torque-ripple mode. The step sequence in the half-step mode alternates between one-phase-on and two-phase-on states resulting in torque ripple during the stepping sequence. In the compensated-torque mode, the ripple is eliminated by equalizing the torques for the alternate states. This is done by alternately switching the SENSE reference voltages between 100% and 70.7% in alternate cycles.

The CT_EN input is relevant only in the half-step mode, since the alternating one-step-on and two-step-on sequence does not exist in the full-step mode.

This input has an internal pull-up.

**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_S$ | Supply Voltage | 10 | V |
| $V_I$ | Input Signals | 7 | V |
| $T_{STG}$, $T_J$ | Storage and Junction Temperatures | -40 to +150 | °C |

**ELECTRICAL CHARACTERISTICS:** (Refer to Block Diagram, Figure 2, and Timing Diagram, Figure 3)
$T_A$ = +25°C, $V_{DD}$ = +5V unless otherwise specified.

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|---|---|---|---|---|---|---|
| (**Pin 15**) | | | | | | |
| Supply Voltage | $V_{DD}$ | 4.75 | - | 7 | V | - |
| Quiescent Supply Current | $I_{DD}$ | - | 300 | 400 | uA | Outputs floating |
| (**Pins 13, 14, 21, 22, 23 and 24**) | | | | | | |
| Input Voltage Low | $V_{IL}$ | - | - | 0.75 | V | - |
| Input Voltage High | $V_{IH}$ | 2 | - | - | V | - |
| (**Pins 14, 21, 22, 23, 29**) | | | | | | |
| Input Current | $I_{IH}$, $I_{IL}$ | - | - | 50 | nA | $V_I = V_{IL}$ or $V_{IH}$ |
| Input Current (**Pin 13**) | $I_{IL}$ | - | - | 50 | nA | $V_I$ = 0 |
| | $I_{IH}$ | - | - | 50 | nA | $V_I = V_{DD}$ |
| (**Pin 10**) | | | | | | |
| Enable Input Voltage Low | $V_{ENL}$ | - | - | 1.3 | V | - |
| Enable Input Voltage High | $V_{ENH}$ | 2 | - | - | V | - |
| Enable Input Current | $I_{EN}$ | - | - | 50 | nA | $V_{EN} = V_{ENL}$ |
| Enable Input Current | $I_{EN}$ | - | - | 50 | nA | $V_{EN} = V_{ENH}$ |
| (**Pins 4, 6, 7, 9**) | | | | | | |
| Phase Output Voltage Low | $V_{OL}$ | - | - | 0.5 | V | $I_O$ = -10mA |
| Phase Output Voltage High | $V_{OH}$ | 4.0 | - | - | V | $I_O$ = 5mA |
| (**Pins 5, 8**) | | | | | | |
| Inhibit Output Voltage Low | $V_{InhL}$ | - | - | 0.5 | V | $I_O$ = -10mA |
| Inhibit Output Voltage High | $V_{InhH}$ | 4.0 | - | - | V | $I_O$ = 5mA |
| Leakage Current (**Pin 3**) | $I_{Leak}$ | - | - | 1 | uA | $V_{CE}$ = 7V |
| Saturation Voltage (**Pin 3**) | $V_{Sat}$ | - | - | 0.4 | V | I = 5mA |
| (**Pins 13, 14, 15**) | | | | | | |
| Comparators Offset Voltage | $V_{Off}$ | - | 5 | - | mV | $V_{REF}$ = 1V |
| Comparator Bias Current | $I_O$ | 100 | - | 10 | uA | - |
| (**Pins 18, 19**) | | | | | | |
| Input Reference Voltages | VREFs, VREFh | 0 | - | 3 | V | - |
| Input Currents | IREFs, IREFh | - | - | 8 | uA | VREFs, VREFh = 3V |
| (**Pin 11**) | | | | | | |
| RC Input Low | $V_{RCL}$ | 0 | - | 2.5 | V | - |
| RC Input High | $V_{RCH}$ | 3.5 | - | - | V | - |
| External resistor at RC | R | 10 | - | No Limit | kΩ | - |
| $\overline{\text{Step}}$ Pulse Width | $t_{stp}$ | 0.5 | - | - | us | - |
| Set up time | $t_S$ | 1 | - | - | us | - |
| Hold time | $t_H$ | 4 | - | - | us | - |
| Reset time | $t_R$ | 1 | - | - | us | - |
| Reset to Step delay | $t_{RStp}$ | 1 | - | - | us | - |
| (**Pin 20**) **Oscillator:** | | | | | | |
| Sawtooth Low | $V_{SOL}$ | - | 2.1 | - | V | - |
| Sawtooth High | $V_{SOH}$ | - | 3.65 | - | V | - |

| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Condition |
|---|---|---|---|---|---|---|
| Oscillator Frequency | $f_{OSC}$ | - | 30 | - | kHz | R = 22kΩ, C = 3.3nF |
| **SYNC** (**Pin1**) | | | | | | |
| Sync Output Voltage Low | $V_{SyncL}$ | - | - | 0.8 | V | $I_O$ = -5mA |
| Sync Output Voltage High | $V_{SyncH}$ | 3.0 | - | - | V | $I_O$ = 5mA |
| Sync Input Pulse Width | $T_{SPW}$ | - | 3.3 | - | V | R = 22kΩ, C = 3.3nF |
| Sync Input Switching Point | $T_{SSP}$ | - | 2.0 | - | us | Pin 16 ≤ 1.0V |
| Sync Input Pulse Width | $I_{IS}$ | - | -425 | - | uA | Pin 16 ≤ 1.0V, $V_{IN} = V_{DD}$ |

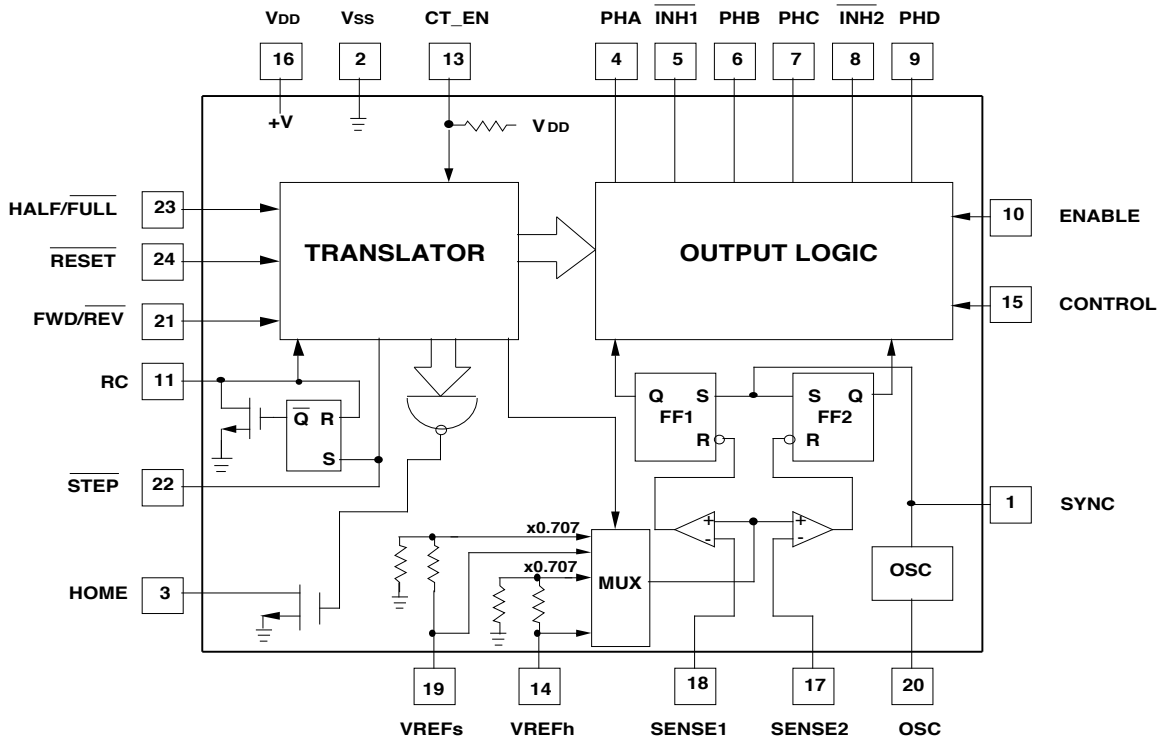



**FIGURE 2. LS8397 BLOCK DIAGRAM**

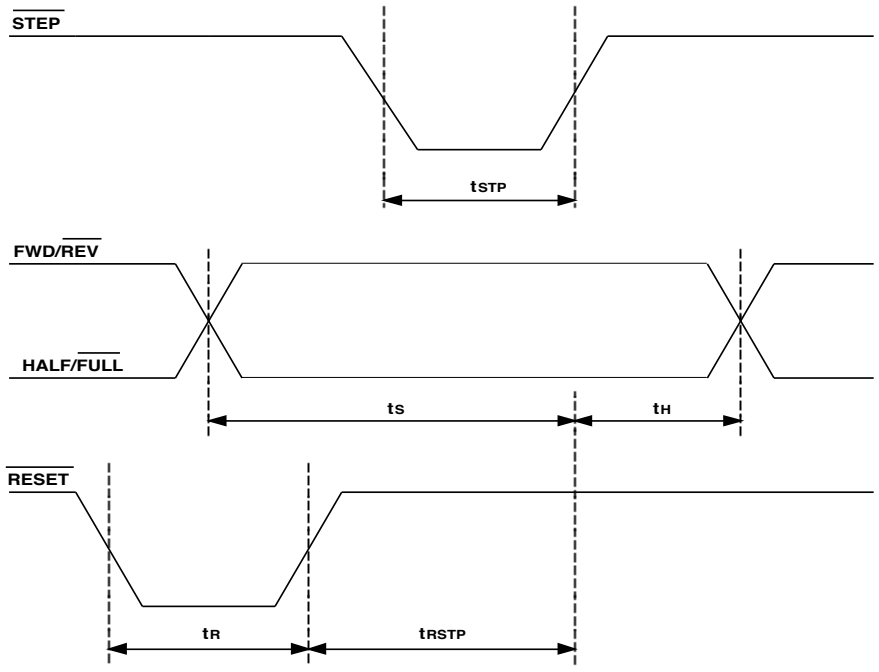
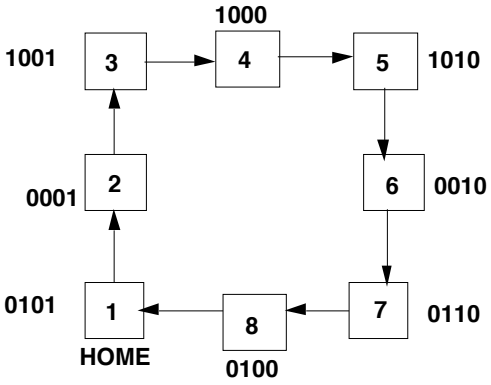



**FIGURE 3. Input Timing Diagram**



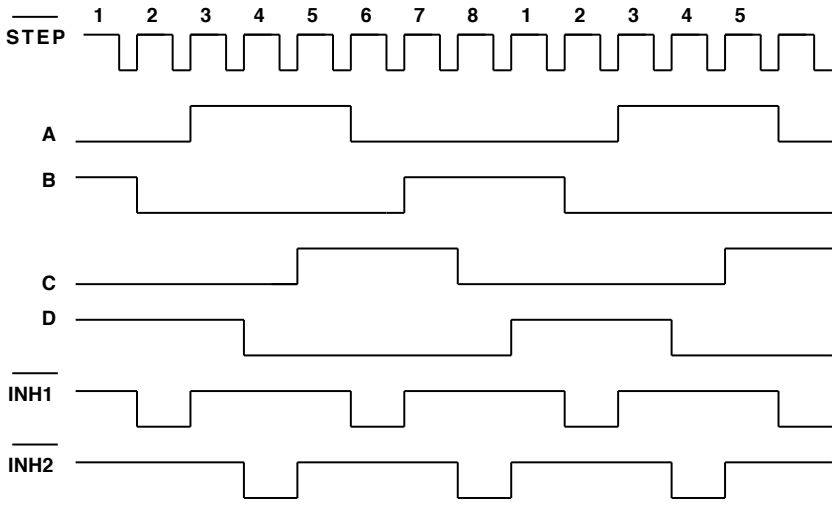
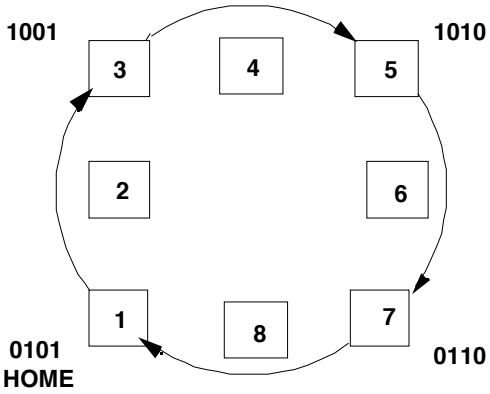




**FIGURE 4A. HALF-STEP MODE**



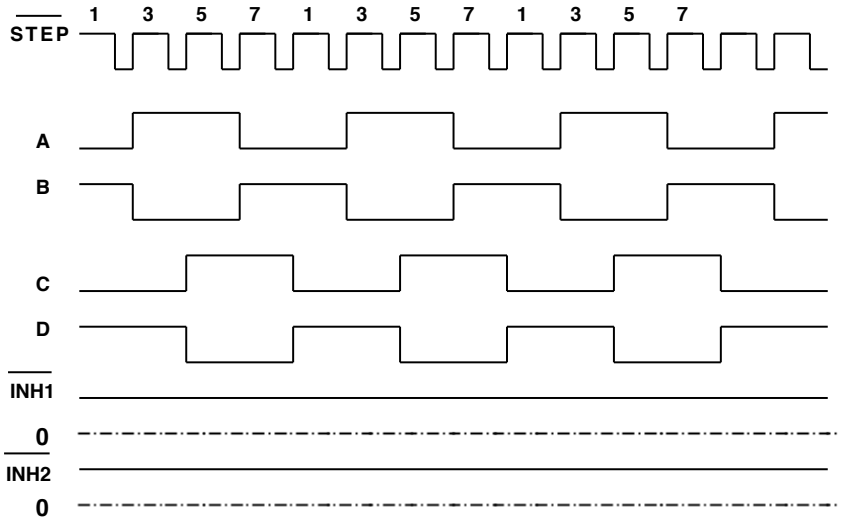
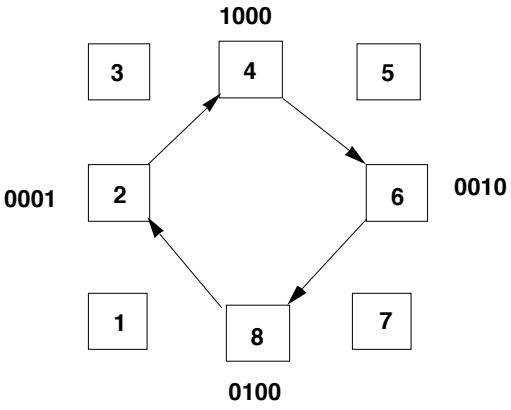




**FIGURE 4B. NORMAL DRIVE MODE (TWO-PHASE-ON)**



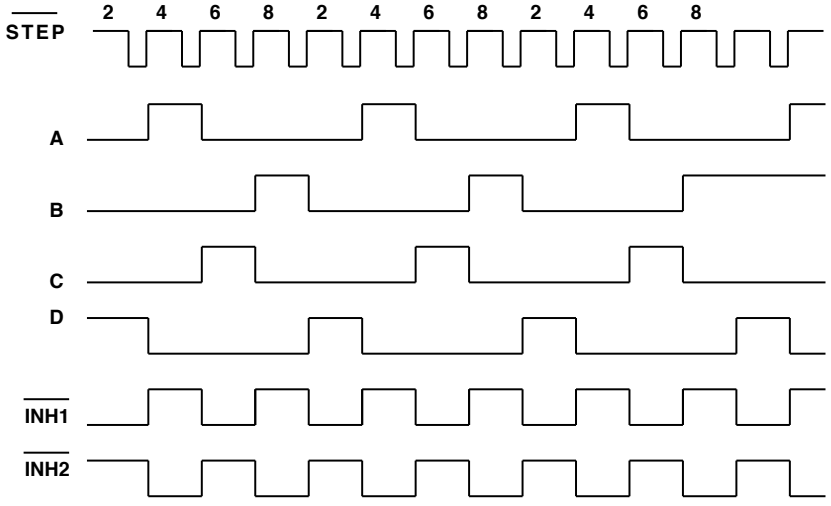
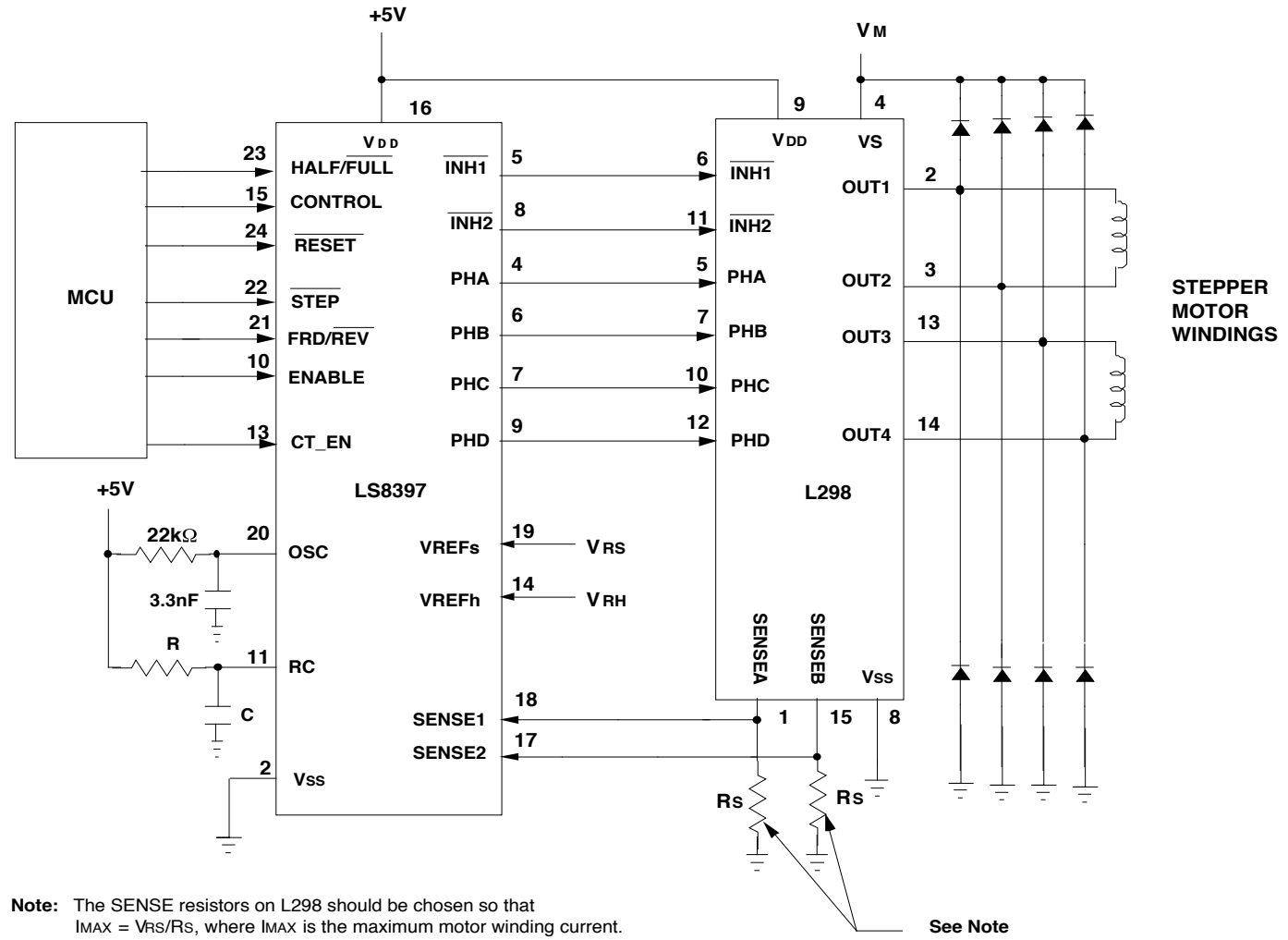




**FIGURE 4C. WAVE DRIVE MODE (ONE-PHASE-ON)**

**FIGURE 4. MOTOR DRIVING SEQUENCES**

The **LS8397** generates phase sequences for half-step mode, normal drive mode and wave drive mode. Advancing occurs on the positive edge of the STEP input signal. HOME is defined as PHA, PHB, PHC, PHD being 0101, respectively. The State Diagrams showing the phase output polarities for all states are shown above for clockwise rotation. For counter clockwise rotation, the sequences are reversed. RESET restores the phases to 0101 and State 1.




**Note:** The SENSE resistors on L298 should be chosen so that $I_{MAX} = V_{RS}/R_S$, where $I_{MAX}$ is the maximum motor winding current.

**FIGURE 5A. Typical Application Schematic for a Two-Phase Bipolar Motor Using a Single Motor Driver IC**

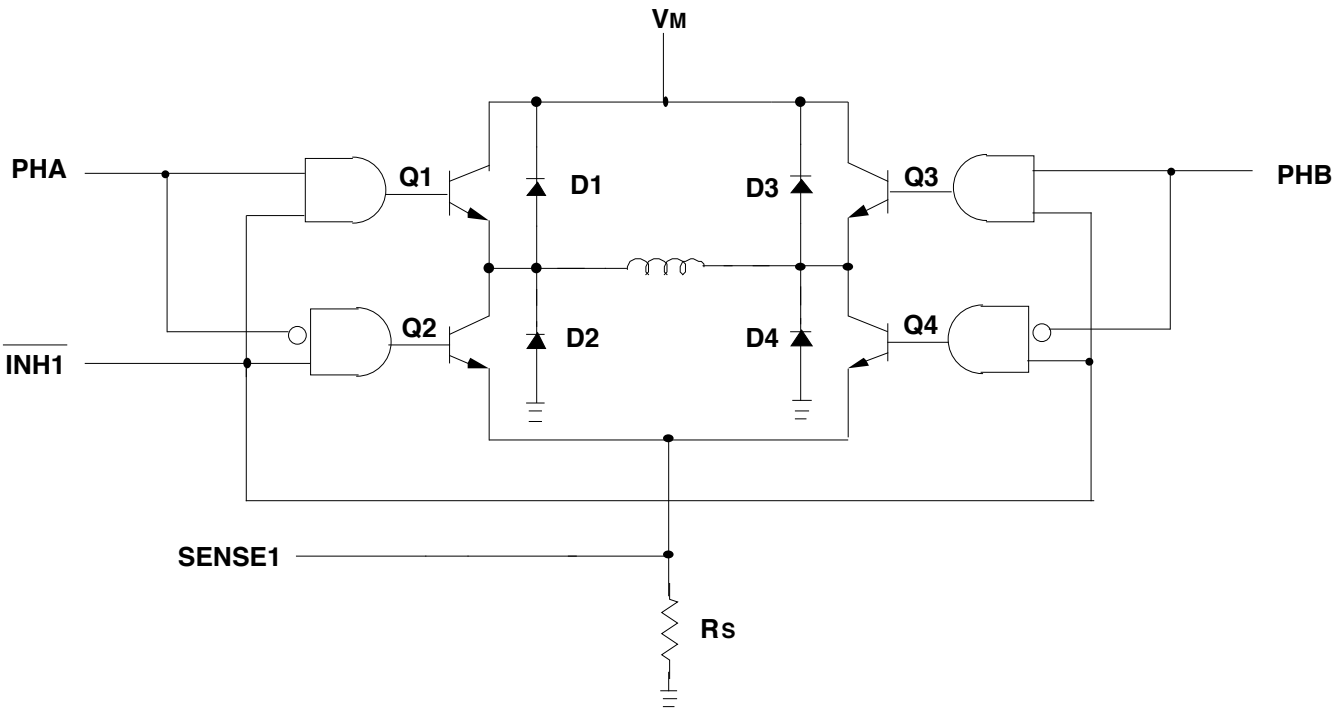
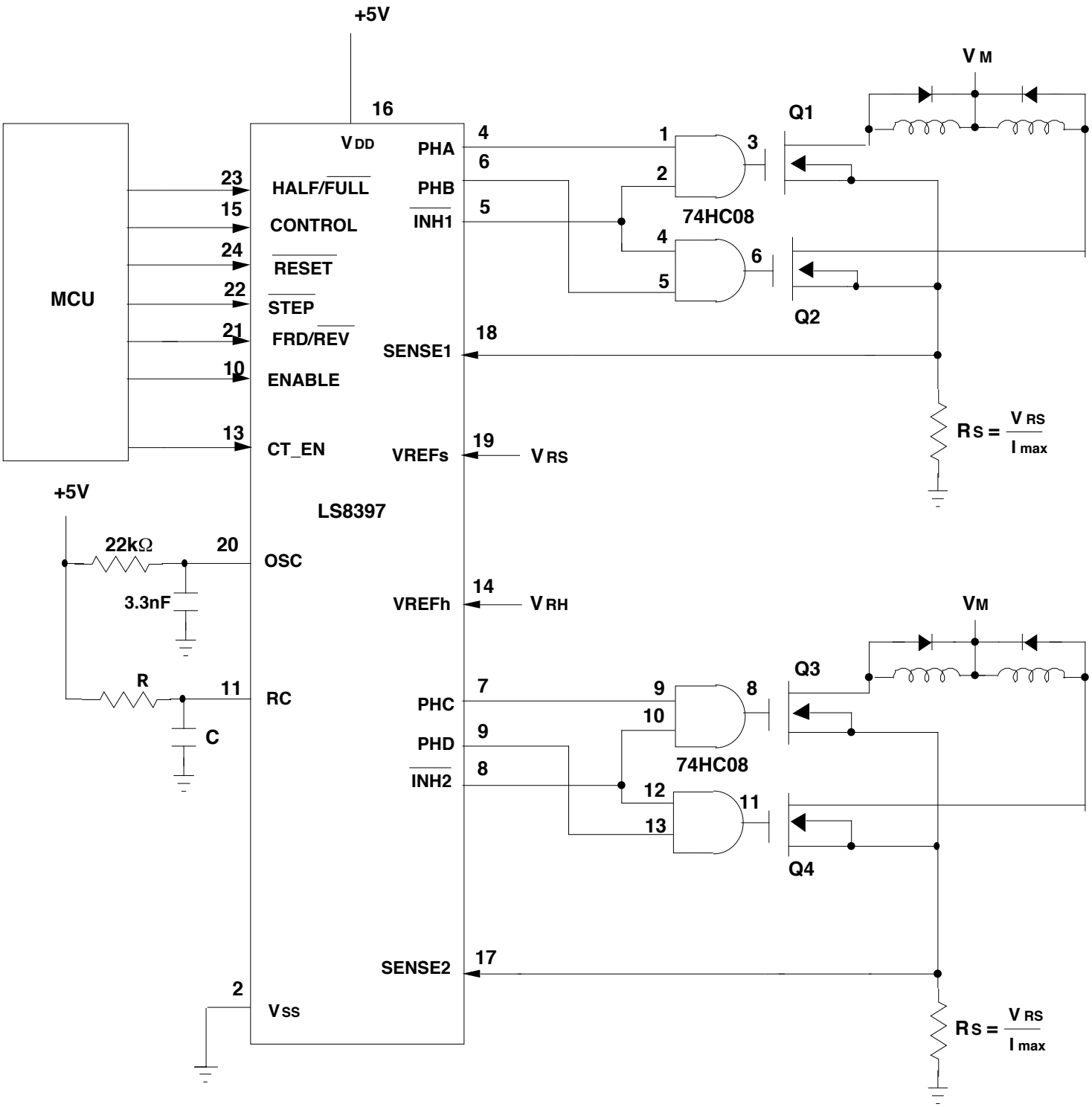



**FIGURE 5B. One half of L298 Drive Stage**




**NOTE: Q1, Q2, Q3, Q4 are MOSFET Power Transistors suitable for 5V Gate Drive**
**Typical P/Ns = IRLZ44N and IRF3708**

**FIGURE 6. TYPICAL APPLICATION SCHEMATIC FOR A FOUR-PHASE UNIPOLAR MOTOR USING DISCRETE MOSFET TRANSISTORS**

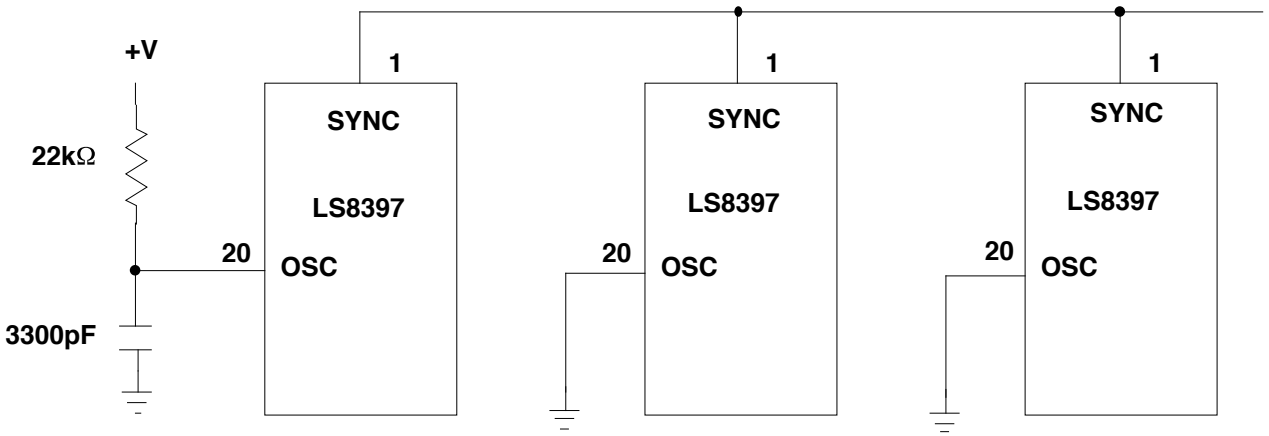



**FIGURE 7. Synchronizing Multiple LS8397s**