CADEKA
Amplify the Human Experience

SPT7734

8-BIT, 40 MSPS,175 mW A/D CONVERTER

FEATURES

- Monolithic 40 MSPS Converter
- 175 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum
- Selectable +3 V or +5 V Logic I/O

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Digital Communications

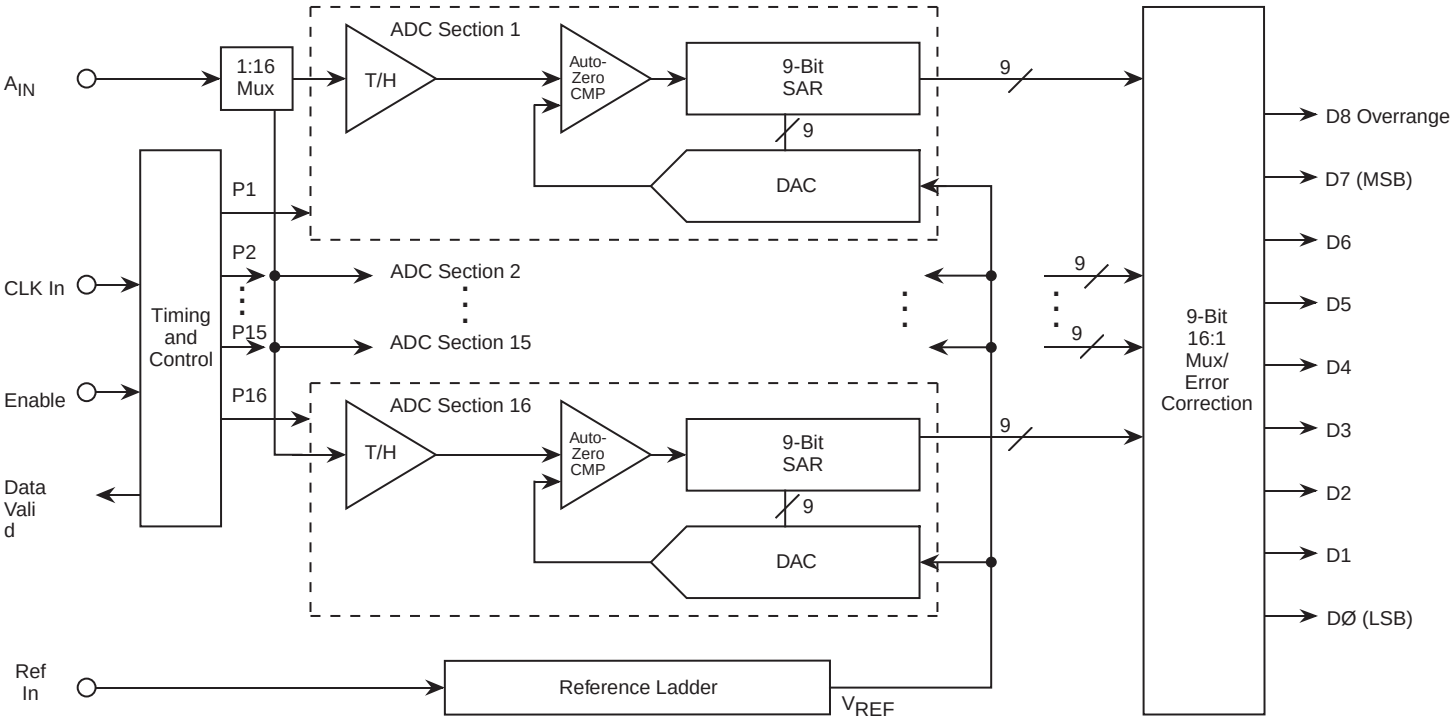
GENERAL DESCRIPTION

The SPT7734 is a 8-bit monolithic, low cost, ultralow power analog-to-digital converter capable of minimum word rates of 40 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7734's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 175 mW typical at 40 MSPS with a power supply of +5.0 V. The digital outputs are +3 V or +5 V, and are user selectable. The SPT7734 has incorporated proprietary circuit design and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7734 is available in 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.5 V to AV_{DD} +0.5 V
V_{REF} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
AV_{DD} - DV_{DD} ..... ±100 mV
AGND - DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to +70 °C
Junction Temperature ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MAX}$ to T_{MAX}, $AV_{DD}=DV_{DD}=+5.0$ V, $V_{IN}=0$ to 4 V, $f_S=40$ MSPS, $V_{RHS}=4.0$ V, $V_{RLS}=0.0$ V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7734 MIN	SPT7734 TYP	SPT7734 MAX	UNITS
Resolution			8			Bits
DC Accuracy						
Integral Nonlinearity		IV		±1.0		LSB
Differential Nonlinearity		IV		±0.5		LSB
No Missing Codes		VI		Guaranteed		
Analog Input						
Input Voltage Range		VI	V_{RLS}		V_{RHS}	V
Input Resistance		IV	50			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V	250			MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		VI	300	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		VI	40			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		4.0		ns
Aperture Jitter Time		V		30		ps(p-p)
Dynamic Performance						
Effective Number of Bits						
f_{IN}=3.58 MHz		VI	7.3	7.8		Bits
f_{IN}=10.3 MHz		VI	7.2	7.7		Bits

ELECTRICAL SPECIFICATIONS

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7734 MIN	SPT7734 TYP	SPT7734 MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=3.58 MHz		VI	46	49		dB
f_{IN}=10.3 MHz		VI	45	48		dB
Harmonic Distortion	9 Distortion bins from					
f_{IN}=3.58 MHz	1024 pt FFT	VI	53	57		dB
f_{IN}=10.3 MHz		VI	53	56		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=3.58 MHz		VI	46	49		dB
f_{IN}=10.3 MHz		VI	45	48		dB
Spurious Free Dynamic Range	f_{IN}=1.0 MHz	V		63		dB
Differential Phase		V		±0.3		Degree
Differential Gain		V		±0.3		%
Intermodulation Distortion				TBD		dB
Inputs						
Logic 1 Voltage		VI	2.0			V
Logic 0 Voltage		VI			0.8	V
Maximum Input Current Low		VI	-10		+10	µA
Maximum Input Current High		VI	-10		+10	µA
Input Capacitance		V		+5		pF
Digital Outputs						
Logic 1 Voltage	I_{OH} = 0.5 mA	VI	3.5			V
Logic 0 Voltage	I_{OL} = 1.6 mA	VI			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages OV_{DD}		IV	3.0		5.0	V
DV_{DD}		IV	4.75	5.0	5.25	V
AV_{DD}		IV	4.75	5.0	5.25	V
Currents AI_{DD}		VI		17	22	mA
DI_{DD}		VI		18	23	mA
Power Dissipation		VI		175	225	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

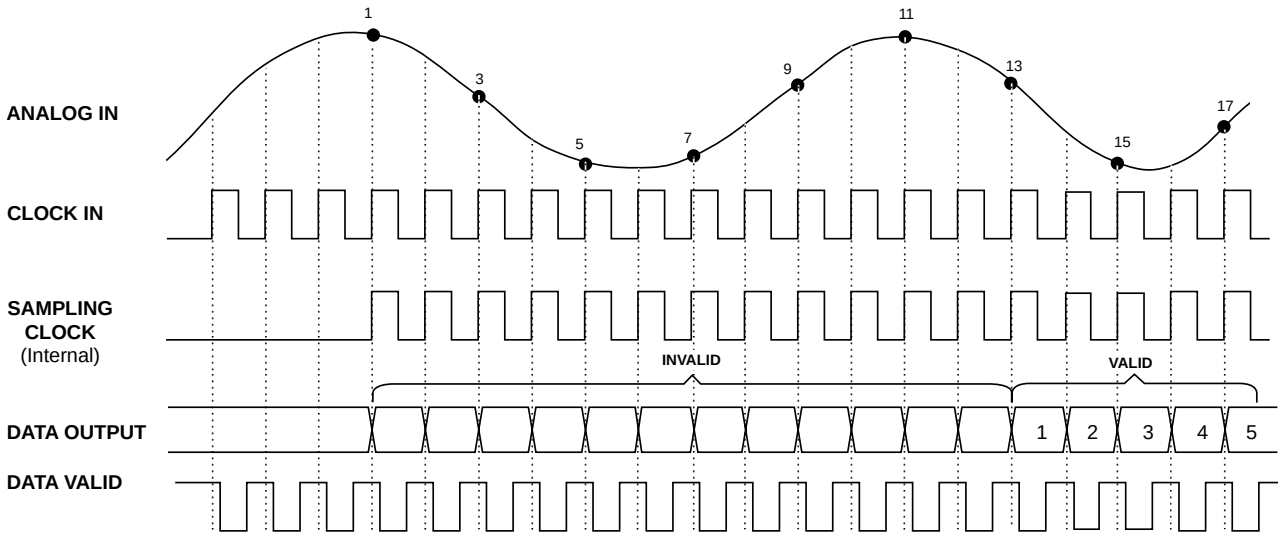


Figure 1B: Timing Diagram 2

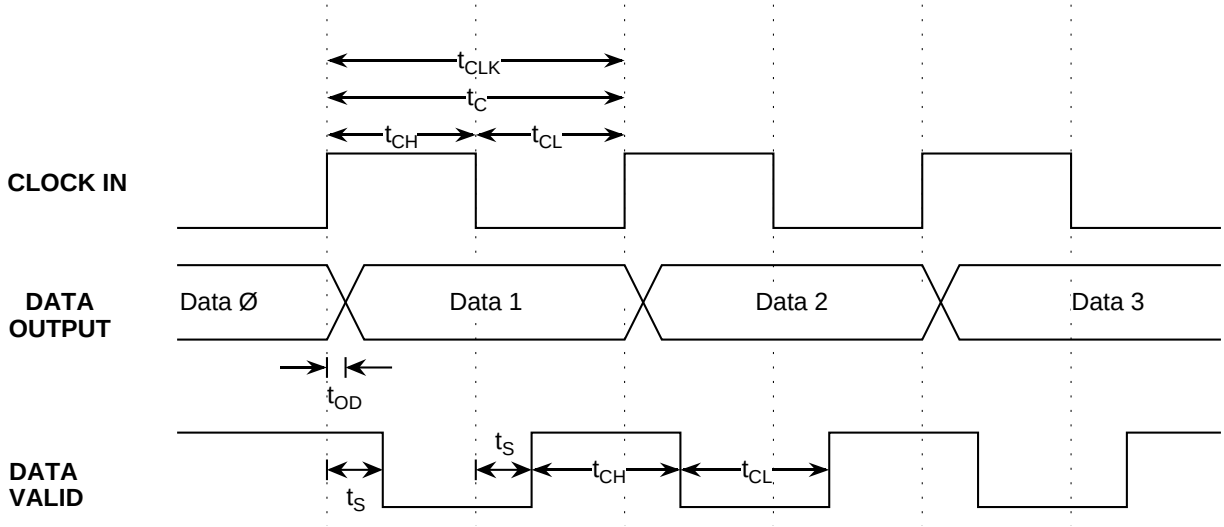


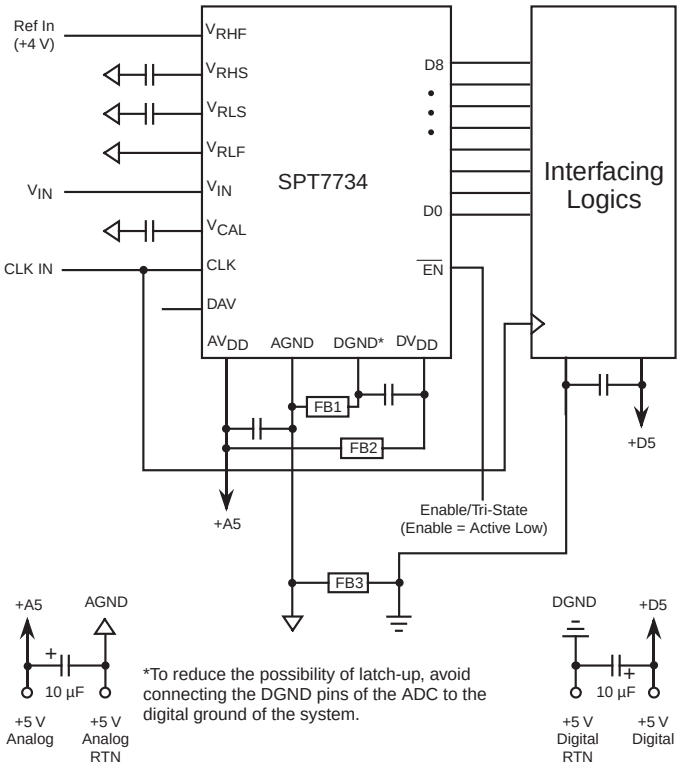
Table I - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_C	t_{CLK}			ns
Clock Period	t_{CLK}	25			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Clock to Output Delay (15 pF Load)	t_{OD}		17		ns
Clock to DAV	t_S		10		ns

TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 1 shows the typical interface requirements when using the SPT7734 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



NOTES: 1) FB3 is to be located as closely to the device as possible.
2) There should be no additional connections to the right of FB1 and FB2.
3) All capacitors are 0.1 µF surface-mount unless otherwise specified.
4) FB1, FB2 and FB3 are 10 µH inductors or ferrite beads.

POWER SUPPLIES AND GROUNDING

CADEKA suggests that both the digital and the analog supply voltages on the SPT7734 be derived from a single analog supply as shown in figure 1. A separate digital supply should be used for all interface circuitry. CADEKA suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains 16 identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 9-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Table II - Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	9-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

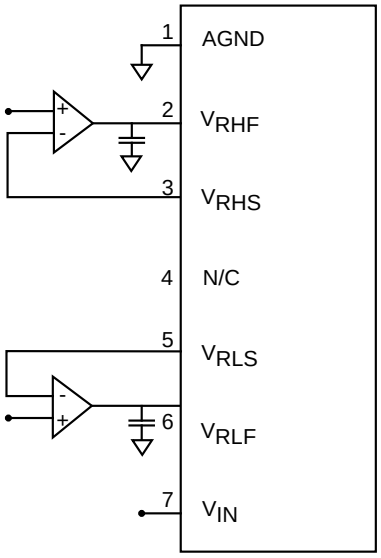
- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7734 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

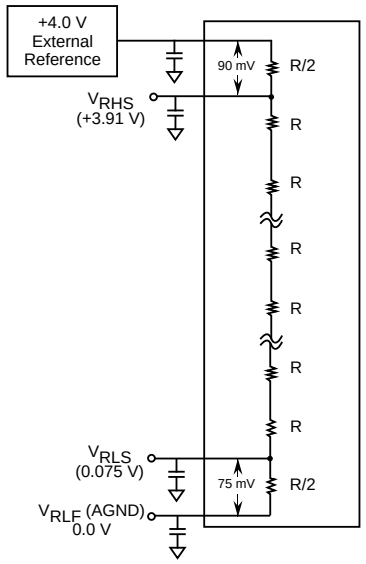
Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 2, offset and gain errors of less than ±2 LSB can be obtained.

Figure 2 - Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 3 - Simplified Reference Ladder Drive Circuit Without Force/Sense Circuit



R=30 Ω (typ)
All capacitors are 0.01 µF

In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 3. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 3 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS}$ = 2.25 % of ($V_{RHF} - V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF}$ = 1.9 % of ($V_{RHF} - V_{RLF}$) (typical).

Figure 3 shows an example of expected voltage drops for a specific case. Vref of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7734's extremely low input capacitance of only 5 pF and very high input resistance in excess of 50 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 4.

CALIBRATION

The SPT7734 uses an auto calibration scheme to ensure 8-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 8-bit accuracy during device operation. This process is completely transparent to the user.

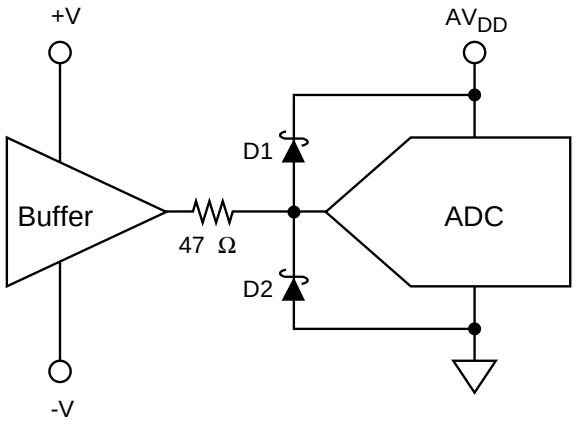
Upon power-up, the SPT7734 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 8-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec (for a 40 MHz clock). Once calibrated, the SPT7734 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7734 to remain in calibration.

INPUT PROTECTION

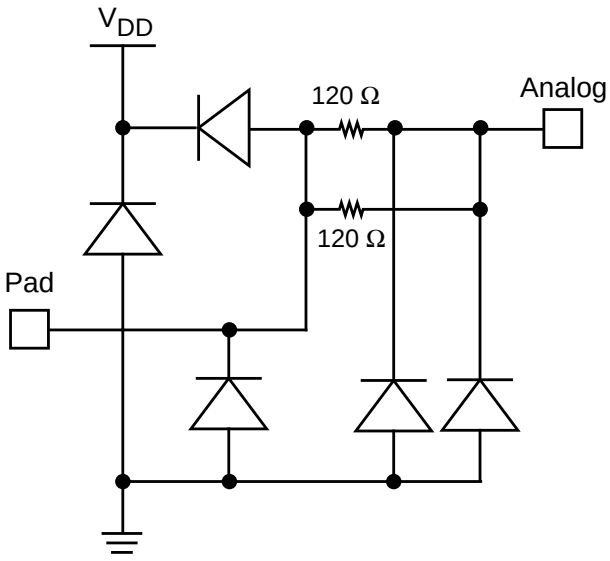
All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 4 - Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

Figure 5 - On-Chip Protection Circuit



CLOCK INPUT

The SPT7734 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance.

DIGITAL OUTPUTS

The digital outputs (D0-D8) are driven by a separate supply (OV_{DD}) ranging from +3 V to +5 V. This feature makes it possible to drive the SPT7734's TTL/CMOS-compatible outputs with the user's logic system supply. The format of the output data (D0-D7) is straight binary. (See table III.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table III - Output Data Information

ANALOG INPUT	OVERRANGE D8	OUTPUT CODE D7-D0
+F.S. + 1/2 LSB	1	1111 1111
+F.S. -1/2 LSB	O	1111 111Ø
+1/2 F.S.	O	ØØØØ ØØØØ
+1/2 LSB	O	OOOO OOOØ
0.0 V	O	OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

DO NOT CONNECT PINS (DNC)

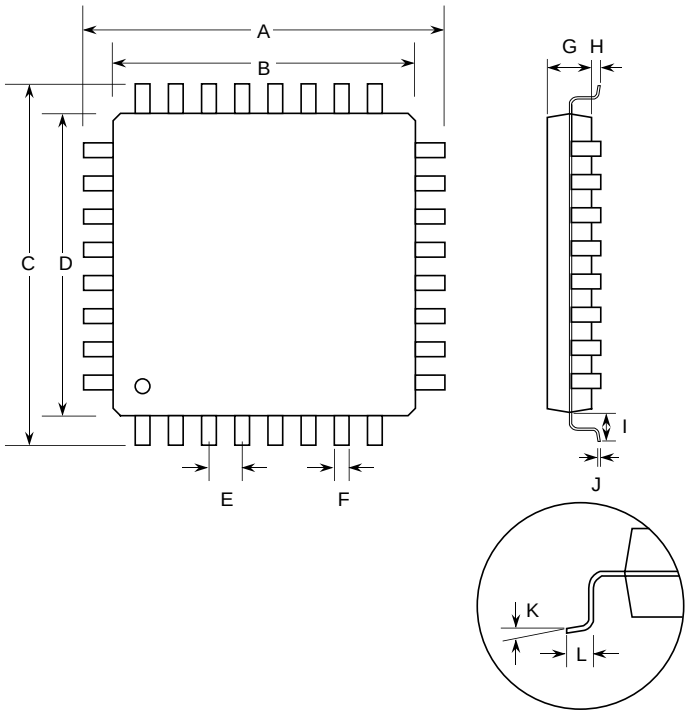
There are two pins designated as Do Not Connect (DNC). These pins must be left floating for proper operation of the device.

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D8) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D8 will switch to logic 1. All other data outputs (D0 to D7) will remain at logic 1 as long as D8 remains at logic 1. This feature makes it possible to include the SPT7734 into higher resolution systems.

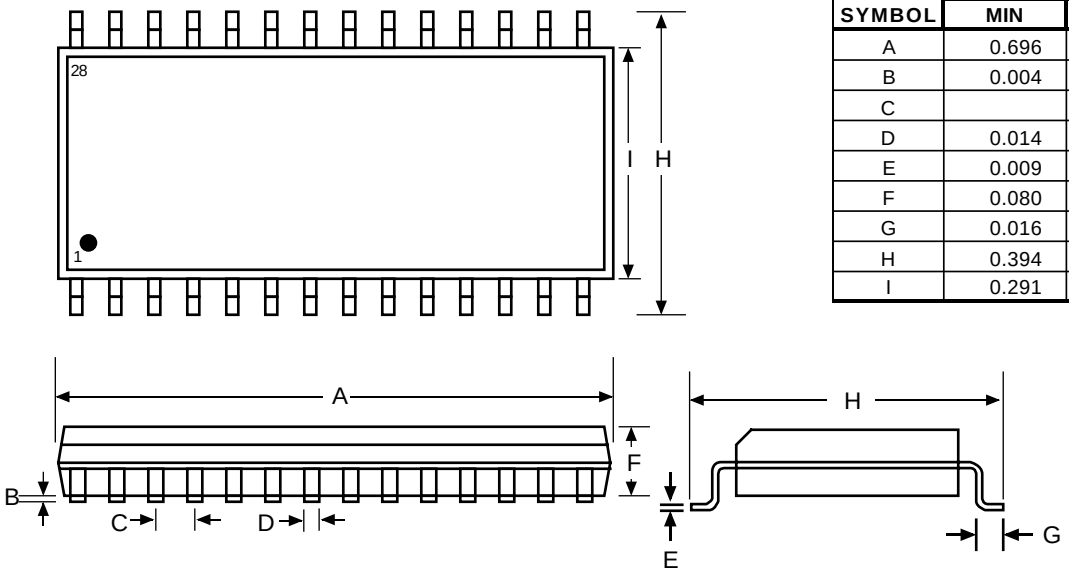
PACKAGE OUTLINES

32-Lead TQFP



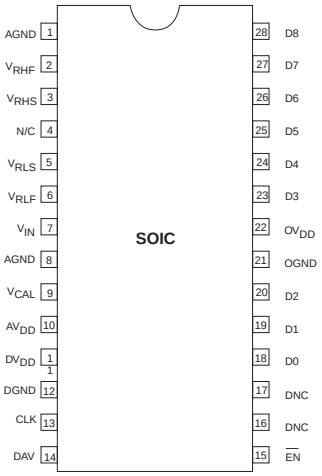
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.347	0.355	8.90	9.10
B	0.269	0.277	6.90	7.10
C	0.347	0.355	8.90	9.10
D	0.269	0.277	6.90	7.10
E	0.027	0.035	0.68	0.89
F	0.012	0.018	0.30	0.45
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.039 typ		1.00 typ	
J	0.004	0.008	0.09	0.20
K	0°	7°	0°	7°
L	0.018	0.029	0.45	0.75

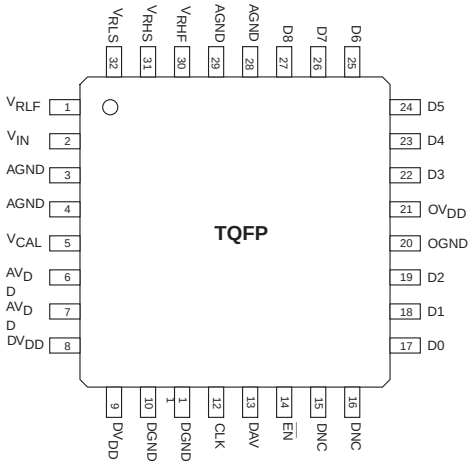
28-Lead SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.696	0.712	17.68	18.08
B	0.004	0.012	0.10	0.30
C		.050 typ	0.00	1.27
D	0.014	0.019	0.36	0.48
E	0.009	0.012	0.23	0.30
F	0.080	0.100	2.03	2.54
G	0.016	0.050	0.41	1.27
H	0.394	0.419	10.01	10.64
I	0.291	0.299	7.39	7.59

PIN ASSIGNMENTS





PIN FUNCTIONS

Name	Function
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-7	Tri-State Data Output, (DØ=LSB)
D8	Tri-State Output Overrange
DAV	Data Valid Output
OV_{DD}	Digital Output Supply
OGND	Digital Output Ground
DNC	Do Not Connect

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7734SCS	0 to +70 °C	28L SOIC
SPT7734SCT	0 to +70 °C	32L TQFP