SPT7722

8-Bit, 250 MSPS A/D Converter with Demuxed Outputs

Features

- TTL/CMOS/PECL input logic compatible
- High conversion rate: 250 MSPS
- Single +5V power supply
- Very low power dissipation: 425mW
- 350 MHz full power bandwidth
- Power-down mode: 24mW
- +3.0V/+5.0V (LVCMOS) digital output logic compatibility
- Single/demuxed output ports selectable
- Improved replacement for AD9054

Applications

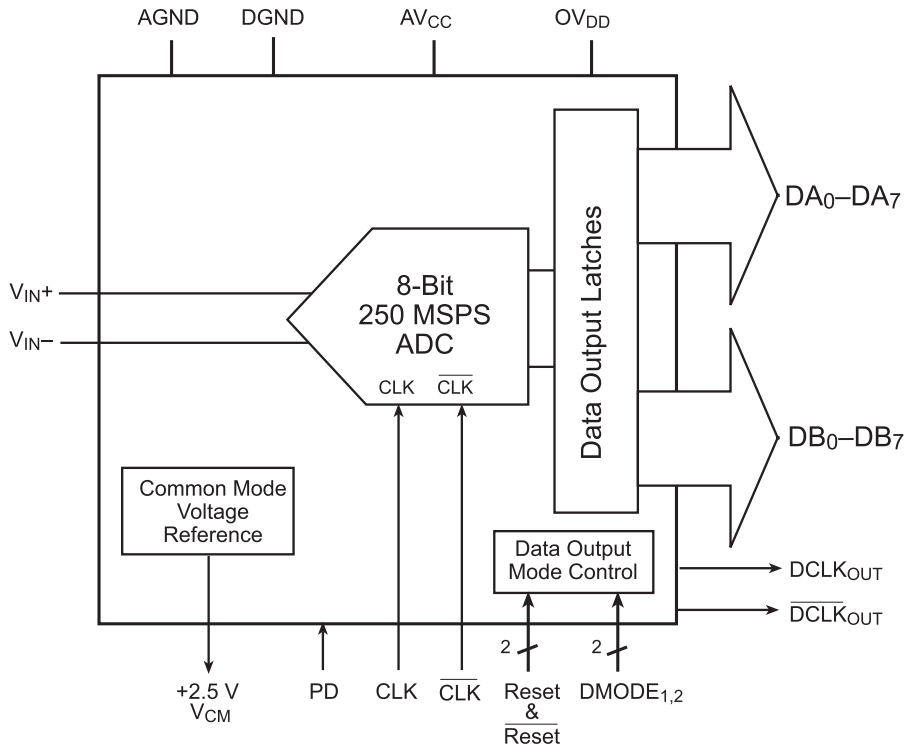
- RGB video processing
- Digital communications
- High-speed instrumentation
- Digital Sampling Oscilloscopes (DSO)
- Projection display systems

Description

The SPT7722 is a high-speed, 8-bit analog-to-digital converter implemented in an advanced BiCMOS process. It is a performance-enhanced version of the SPT7721, offering better linearity and dynamic performance. An advanced folding and interpolating architecture provides both a high conversion rate and very low power dissipation of only 425mW. The analog inputs can be operated in either single-ended or differential input mode. A 2.5V common mode reference is provided on chip for the single-ended input mode to minimize external components.

The SPT7722 digital outputs are demuxed (double-wide) with both dual-channel and single-channel selectable output modes. Demuxed mode supports either parallel aligned or interleaved data output. The output logic is both +3.0V and +5.0V compatible. The SPT7722 is available in a 44-lead TQFP surface mount package over the industrial temperature range of -40°C to +85°C.

Block Diagram



Absolute Maximum Ratings (beyond which damage may occur)[1] 25°C

Parameter	Min.	Max.	Unit
Supply Voltages			
AV_{CC}		+6	V
OV_{DD}		+6	V
Input Voltages			
Analog Inputs	-0.5	V_{CC} +0.5	V
Digital Inputs	-0.5	V_{CC} +0.5	V
Temperature			
Operating Temperature	-40	+85	°C
Storage Temperature	-65	+125	°C

Note:
1. Operation at any absolute maximum rating is not implied.
See Electrical Specifications table for proper nominal applied conditions in typical applications.

Electrical Specifications

($T_A = T_{Min}$ to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
Resolution				8		bits
DC Performance (fIN = 1kHz)						
Differential Linearity Error (DLE)	+25°C	VI	-0.68	±0.4	0.68	LSB
	-40°C to +85°C	IV	-0.95	±0.7	0.95	LSB
Integral Linearity Error (ILE)	+25°C	VI		±1.2	±1.90	LSB
	-40°C to +85°C	IV		±1.4	±2.15	LSB
No Missing Codes @250 MSPS		VI		Guaranteed		
Analog Input						
Input Voltage Range	with respect to V_{IN}-	V		±512		mV_{pp}
Input Common Mode (V_{CM})		IV	2.0	2.5	3.0	V
Input Bias Current	+25°C	V		13		µA
Input Resistance	+25°C	V		50		kΩ
Input Capacitance	+25°C	V		5		pF
Input Bandwidth	+25°C (–3 dB of FS)	V		350		MHz
Gain Error	+25°C	VI	-7.5		+3.5	%FS
Offset Error	+25°C	VI	-5		+5	LSB
Offset Power Supply Rejection Ratio	AV_{CC} = 5V ±0.25V	V		<1		LSB
Timing Characteristics						
Conversion Rate		IV	25	250		MSPS
Output Delay (Clock-to-Data) (t_{pd1})	-40°C to +85°C	IV	7.0	8	9.4	ns
Output Delay Tempco		V		16		ps/°C
Aperture Delay Time (t_{ap})		V		0.3		ns
Aperture Jitter Time		V		2.0		ps-RMS

NOTE: All electrical characteristics are subject to the following condition:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific devices testing actually performed during production and quality assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Electrical Specifications

(T_A = T_{Min} to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
Pipeline Delay (Latency)						
Single Channel Mode		V		2.5		Cycle
Demuxed Interleaved Mode		V		2.5		Cycle
Demuxed Parallel Mode						
Channel B		V		2.5		Cycle
Channel A		V		3.5		Cycle
CLK to $DCLK_{OUT}$ Delay Time						
Single Channel Mode (t_{pd2})		IV	5.0	5.18	5.3	ns
Dual Channel Mode (t_{pd3})		IV	5.6	5.73	5.9	ns
Output Delay (Clock to DClock)		V		18.1		ps/°C
Dynamic Performance						
Effective Number of Bits (ENOB)						
f_{IN} = 70MHz	+25°C	VI	6.4	7.0		Bits
f_{IN} = 70MHz	-40°C to +85°C	IV	6.25	6.8		Bits
Signal-to-Noise Ratio (SNR)						
f_{IN} = 70MHz	+25°C	VI	44.3	46.1		dB
f_{IN} = 70MHz	-40°C to +85°C	IV	42.6	45.4		dB
Total Harmonic Distortion (THD)						
f_{IN} = 70MHz	+25°C	VI		-47	-41.5	dB
f_{IN} = 70MHz	-40°C to +85°C	IV		-45.5	-40.3	dB
Signal-to-Noise & Distortion (SINAD)						
f_{IN} = 70MHz	+25°C	VI	40.2	43.7		dB
f_{IN} = 70MHz	-40°C to +85°C	IV	39.3	42.8		dB
Power Supply Requirements						
AV_{CC} Voltage (Analog Supply)		IV	4.75	5.0	5.25	V
OV_{DD} Voltage (Digital Supply)		IV	2.75		5.25	V
AV_{CC} Current		VI		85	110	mA
AV_{CC} Current Powerdown	+25°C	VI		4.8	5.5	mA
OV_{DD} Current	OV_{DD} = 3.0V, 10pF load					
Single Mode		V		35		mA
Parallel Mode		V		55		mA
Interleave Mode		V		55		mA
Power Dissipation		VI		425	550	mW
Common Mode Reference Output						
Voltage		VI	2.44	2.5	2.56	V
Voltage Tempco		V		84		ppm/°C
Output Impedance	I_{OUT} = ±50 µA	V		1.07		kΩ
Power Supply Rejection Ratio		V		47.5		mV/V

NOTE: All electrical characteristics are subject to the following condition:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific devices testing actually performed during production and quality assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Electrical Specifications

($T_A = T_{Min}$ to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

Parameter	Conditions	Test Level	Min.	Typ.	Max.	Unit
Clock and Reset Inputs	**(Diff & Single-Ended)**					
Diff Signal Amplitude (V_{DIFF})		IV	400			mV_{pp}
Diff High Input Voltage (V_{IHD})		IV	1.4		AV_{CC}	V
Diff Low Input Voltage (V_{ILD})		IV	0		3.9	V
Diff Common Mode Input (V_{CMD})		IV	1.2		4.1	V
SE High Input Voltage (V_{IH})		IV	1.8			V
SE Low Input Voltage (V_{IL})		IV	0		1.2	V
Input Current High (I_{IH})	V_{ID} = 1.5V	VI	–100	43	+100	µA
Input Current Low (I_{IL})	V_{ID} = 1.5V	VI	–100	43	+100	µA
Power Down & Mode Control Inputs	**(Single-Ended)**					
High Input Voltage		IV	2.0		AV_{CC}	V
Low Input Voltage		IV	0		1.0	V
Max Input Current Low		VI	–100	0.5	+100	µA
Max Input Current High <4.0V		VI	–100	50	+100	µA
Digital Outputs						
Logic “1” Voltage	I_{OH} = -0.5mA	VI	OV_{DD}-0.2			V
Logic “0” Voltage	I_{OL} = +1.6mA	VI			0.2	V
T_R/T_F Data	10pF load					
	OV_{DD} = 3V	V		3.3/3.0		ns
	OV_{DD} = 5V	V		2.3/1.9		ns
T_R/T_F DCLK	10pF load					
	OV_{DD} = 3V	V		1.2/1.0		ns
	OV_{DD} = 5V	V		0.7/0.6		ns

NOTE: All electrical characteristics are subject to the following condition:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific devices testing actually performed during production and quality assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

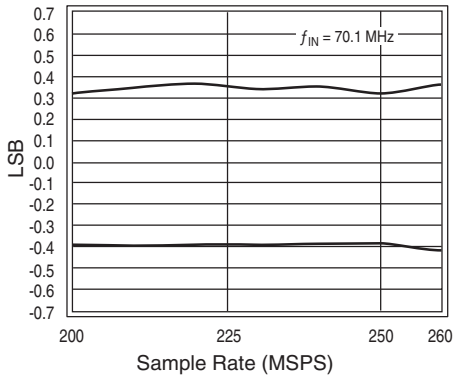
TEST LEVEL CODES:

Level	Test Procedure
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C and sample tested at the specified temperatures.
II	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specific temperature range.

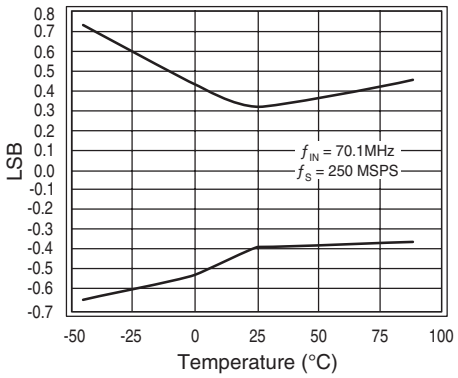
Typical Operating Characteristics

($T_A = T_{Min}$ to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

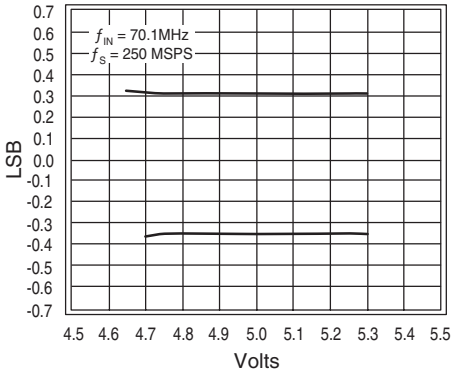
DLE vs. Sample Rate



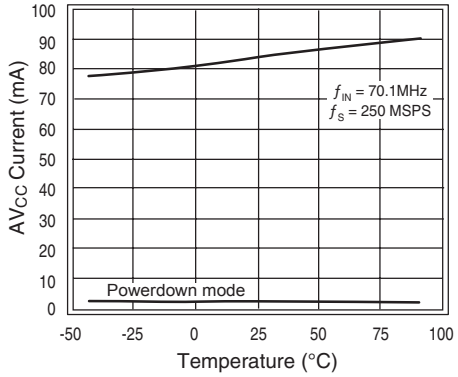
DLE vs. Temperature



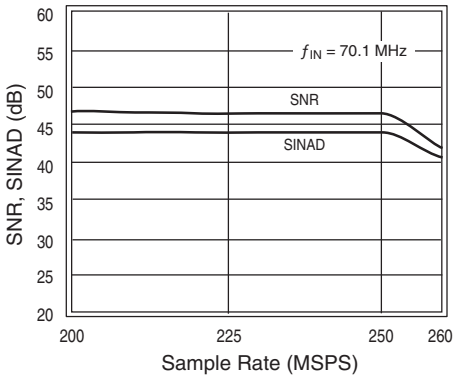
DLE vs. AV_{CC}



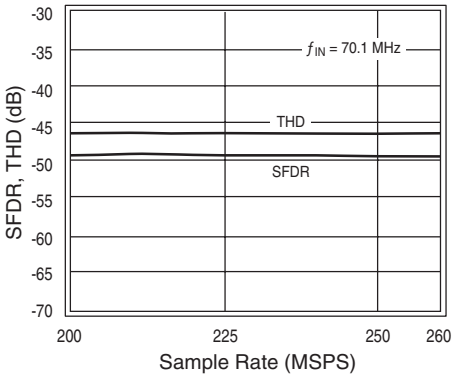
AV_{CC} Current vs. Temperature



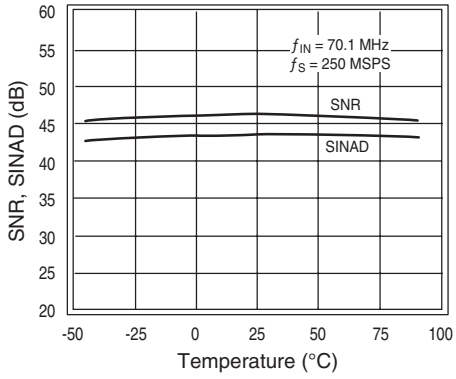
SNR, SINAD vs. Sample Rate



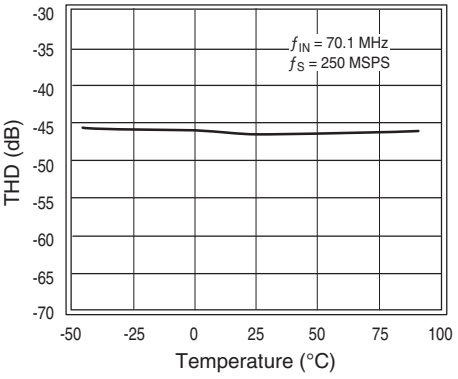
SFDR, THD vs. Sample Rate



SNR, SINAD vs. Temperature



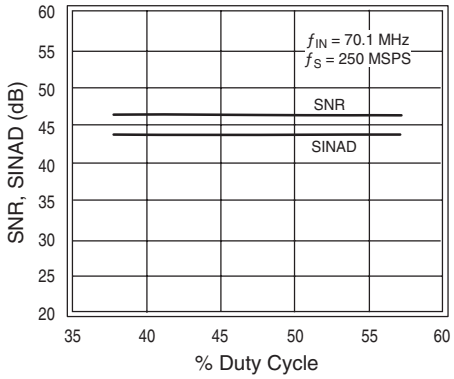
THD vs. Temperature



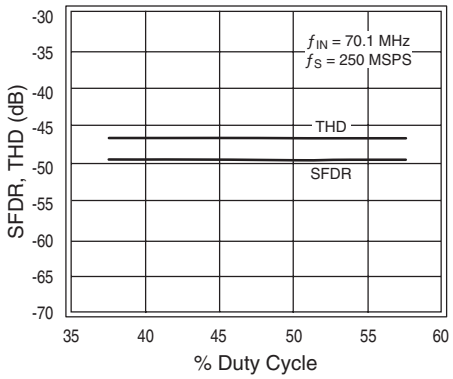
Typical Operating Characteristics

($T_A = T_{Min}$ to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

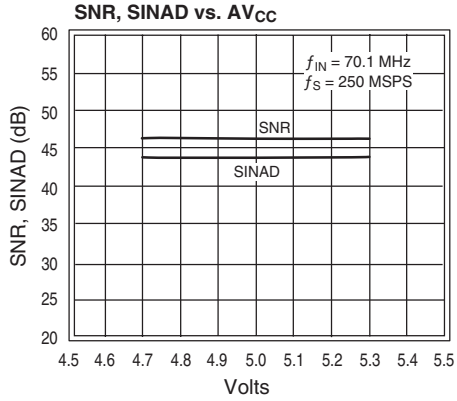
SNR, SINAD vs. Duty Cycle



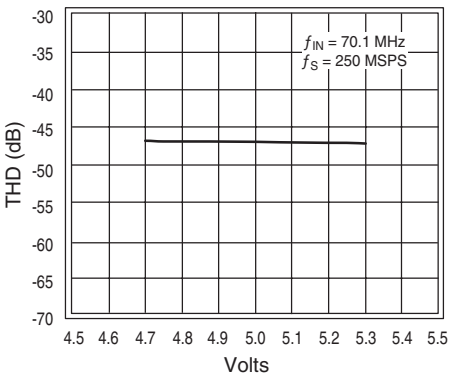
SFDR, THD vs. Duty Cycle



SNR, SINAD vs. AV_{CC}



THD vs. AV_{CC}



Theory of Operation

The SPT7722 is a three-step subranger. It consists of two THAs in series at the input, followed by three ADC blocks. The first block is a three-bit folder with over/under range detection. The second block consists of two single-bit folding interpolator stages. There are pipelining THAs between each ADC block.

The analog decode functions are the input buffer, input THAs, three-bit folder, folding interpolators, and pipelining THAs. The input buffer enables the part to withstand rail-to-rail input signals without latchup or excessive currents and also performs single-ended to differential conversion. All of the THAs have the same basic architecture. Each has a differential pair buffer followed by switched emitter followers driving the hold capacitors. The input THA also has hold mode feed-through cancellation devices.

The three MSBs of the ADC are generated in the first three-bit folder block, the output of which drives a differential reference ladder which also sets the full-scale input range. Differential pairs at the ladder taps generate midscale, quarter and three-quarter scale, overrange, and underrange. Every other differential pair collector is cross-coupled to generate the eighth scale zero crossings. The middle ADC block generates two bits from the folded signals of the previous stages after pipeline THAs. Its outputs drive more pipeline THAs to push the decoding of the three LSBs to the next half clock cycle. The three LSBs are generated in interpolators that are latched one full clock cycle after the MSBs.

The digital decode consists of comparators, exclusive of cells for gray to binary decoding, and/or cells used for mostly over/under range logic. There is a total of 2.5 clock cycles latency before the output bank selection. In order to reduce sparkle codes and maintain sample rate, no more than three bits at a time are decoded in any half clock cycle.

The output data mode is controlled by the state of the demux mode inputs. There are three output modes:

- All data on bank A with clock rate limited to one-half maximum
- Interleaved mode with data alternately on banks A and B on alternate clock cycles
- Parallel mode with bank A delayed one cycle to be synchronous with bank B every other clock cycle

If necessary, the input clock is divided by two. The divided clock selects the correct output bank. The user can synchronize with the divided clock to select the desired output bank via the differential RESET input.

The output logic family is CMOS with output OV_{DD} supply adjustable from 2.7V to 5.25V. There are also differential clock output pins that can be used to latch the output data in single bank mode or to indicate the current output bank in demux mode.

Finally, a power-down mode is available, which causes the outputs to become tri-state, and overall power is reduced to about 24mW. There is a 2V reference to supply common mode for single-ended inputs that is not shut down in power-down mode.

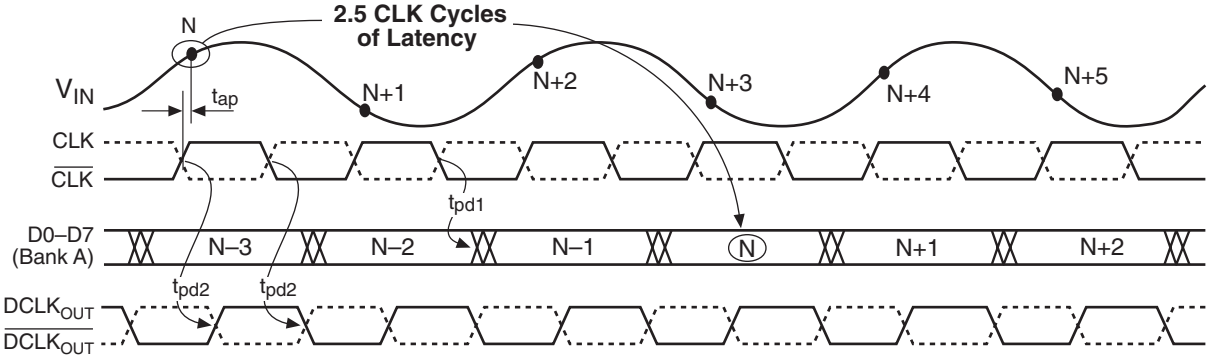


Figure 1. Single Mode Timing Diagram

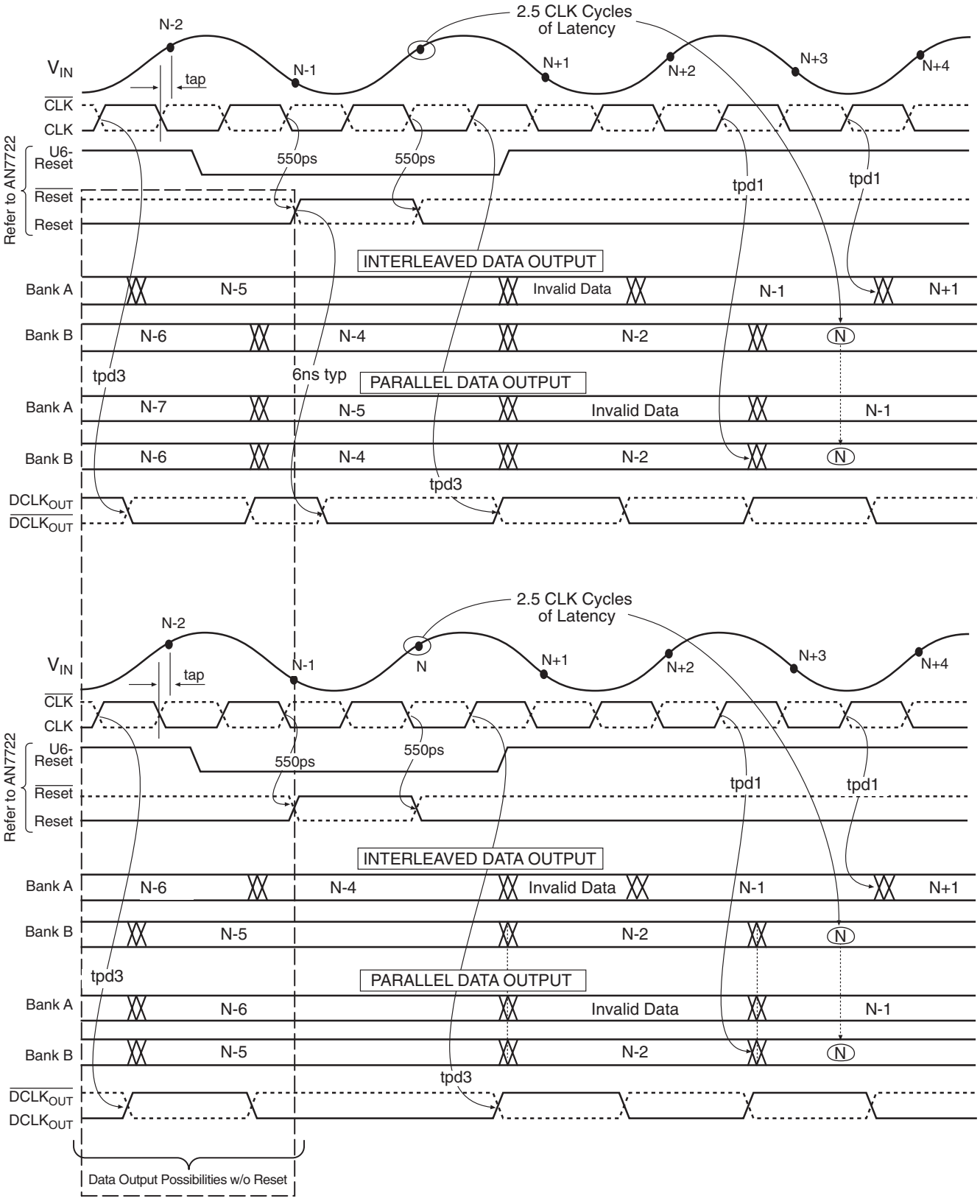
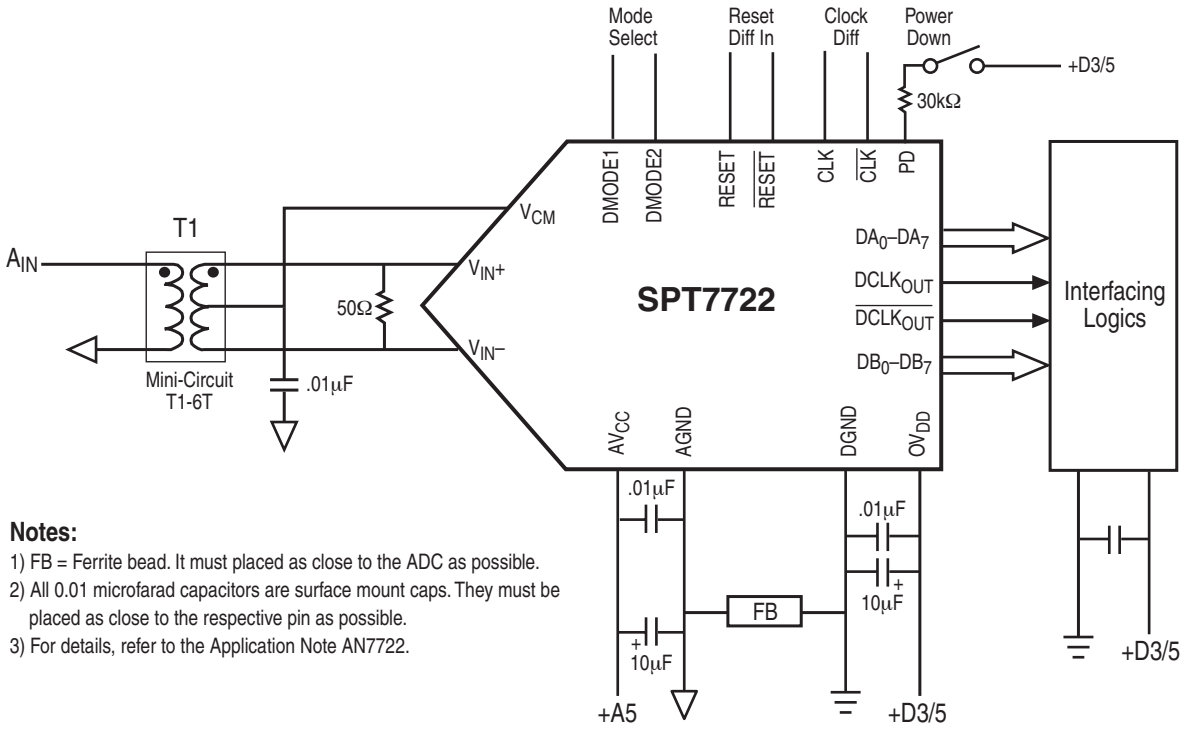


Figure 2. Dual Mode Timing Diagram



Notes:
1) FB = Ferrite bead. It must placed as close to the ADC as possible.
2) All 0.01 microfarad capacitors are surface mount caps. They must be placed as close to the respective pin as possible.
3) For details, refer to the Application Note AN7722.

Figure 3. Typical Interface Circuit

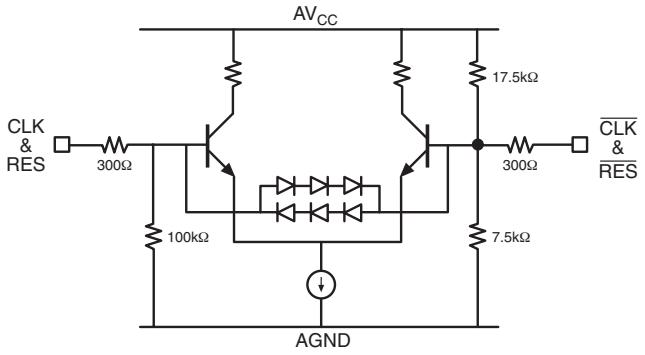


Figure 4. CLK and Reset Equivalent Circuit (without ESD Diodes)

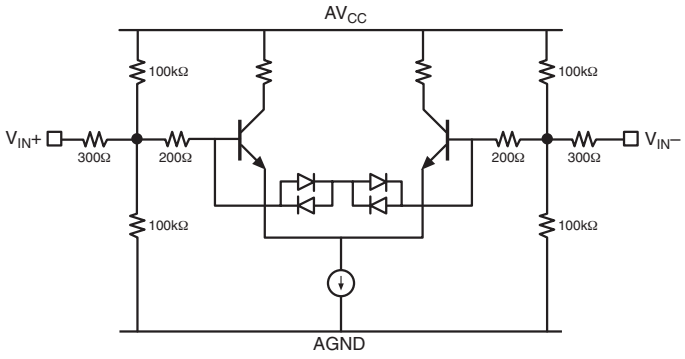


Figure 5. Analog Input Equivalent Circuit

Typical Interface Circuit

Very few external components are required to achieve the stated device performance. Figure 3 shows the typical interface requirements when using the SPT7722 in normal circuit operation. The following sections provide descriptions of the major functions and outline performance criteria to consider for achieving the optimal device performance.

Analog Input

The input of the SPT7722 can be configured in various ways depending on whether a single-ended or differential input is desired.

The AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the V_{CM} pin as shown in Figure 3. To obtain low distortion, it is important that the selected transformer does not exhibit core saturation at the full-scale voltage. Proper termination of the input is important for input signal purity. A small capacitor across the input attenuates kickback noise from the internal track-and-hold.

Figure 6 illustrates a solution (based on operational amplifiers) that can be used if a DC-coupled single-ended input is desired.

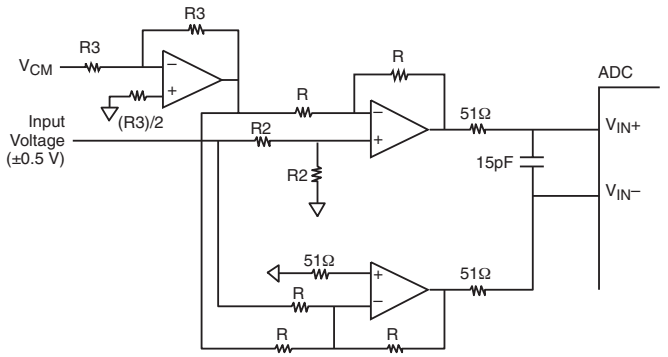


Figure 6. DC-Coupled Single-Ended to Differential Conversion (power supplies and bypassing are not shown)

Input Protection

All I/O pads are protected with an on-chip protection circuit. This circuit provides ESD robustness and prevents latchup under severe discharge conditions without degrading analog transmission times.

Power Supplies and Grounding

The SPT7722 is operated from a single power supply in the range of 4.75V to 5.25V. Normal operation is suggested to be 5.0V. All power supply pins should be bypassed as close to the package as possible. The analog and digital grounds should be connected together with a ferrite bead as shown in the typical interface circuit and as close to the ADC as possible.

Power-Down Mode

To save on power, the SPT7722 incorporates a power-down function. This function is controlled by the signal on pin PD. When pin PD is set high, the SPT7722 enters the power-down mode. All outputs are set to high impedance. In the power-down mode the SPT7722 dissipates 24mW typically.

Common-Mode Voltage Reference Circuit

The SPT7722 has an on-board common-mode voltage reference circuit (V_{CM}). It is 2.5V and is capable of driving 50µA loads typically. The circuit is commonly used to drive the center tap of the RF transformer in fully differential applications. For single-ended applications, this output can be used to provide the level shifting required for the single-to-differential converter conversion circuit. Bypass V_{CM} to AGND by external 0.01µF capacitor, as shown in Figure 3.

Clock Input

The clock input on the SPT7722 can be driven by either a single-ended or double-ended clock circuit and can handle TTL, PECL, and CMOS signals. When operating at high sample rates it is important to keep the pulse width of the clock signal as close to 50% as possible. For TTL/CMOS single-ended clock inputs, the rise time of the signal also becomes an important consideration.

Digital Outputs

The output circuitry of the SPT7722 has been designed to be able to support three separate output modes. The demuxed (double-wide) mode supports either parallel aligned or interleaved data output. The single-channel mode is not demuxed and can support direct output at speeds up to 125 MSPS. The output format is straight binary (table 1).

Table 1. Output Data Format

Analog Input	Output Code D7–D0
+FS	1111 1111
+FS - 1 LSB	1111 111Ø
+1 FS	1000 000Ø
-FS + 1 LSB	0000 000Ø
-FS	0000 0000

Ø indicates the flickering bit between logic 0 and 1

The data output mode is set using the DMODE1 and $DMODE_2$ inputs (pins 32 & 31 respectively). Table 2 describes the mode switching options.

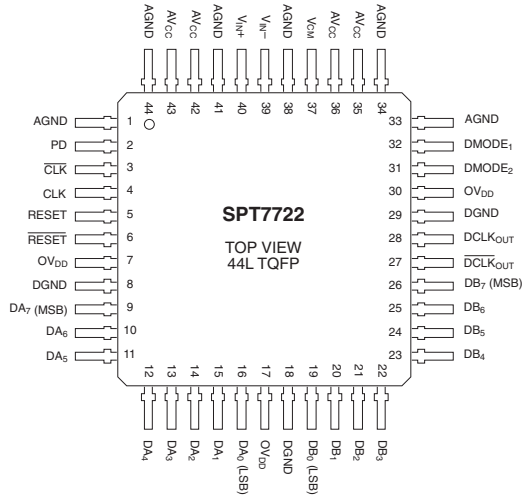
Table 2. Output Data Modes

Output Mode	$DMODE_1$	$DMODE_2$
Parallel Dual Channel Output	0	0
Interleaved Dual Channel Output	0	1
Single Channel Data Output (Bank A only 125 MSPS max)	1	X

Evaluation Board

The EB7721/22 evaluation board is available to aid designers in demonstrating the full performance of the SPT7722. This board includes a clock driver and reset circuit, adjustable references and common mode, a single-ended to differential input buffer and a single-ended to differential transformer (1:1). An application note (AN7722) describing the operation of this board, as well as information on the testing of the SPT7722, is also available. Contact the factory for price and availability of the EB7722.

Pin Assignments



Pin Definitions

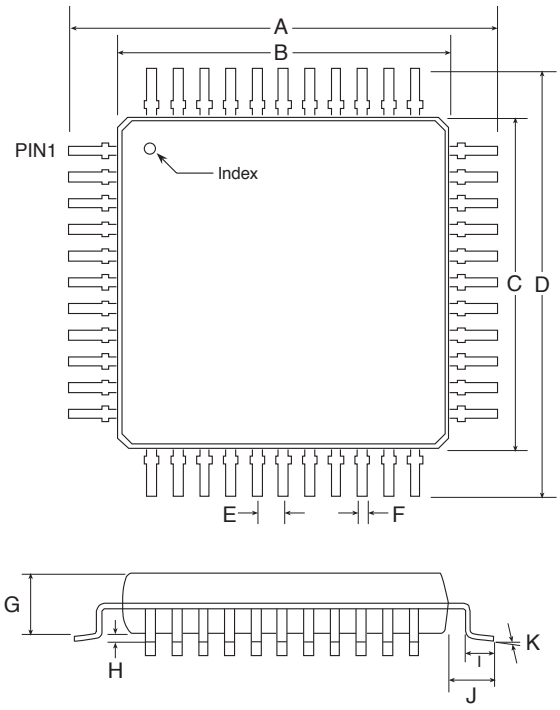
Pin Name	Pin Number	Pin Function Description
V_{IN}+	40	Non-Inverted Analog Input; nominally 1 V_{PP}; 100k pullup to V_{CC} and 100k pulldown to AGND, internally
V_{IN}-	39	Inverted Analog Input; nominally 1 V_{PP}; 100k pullup to V_{CC} and 100k pulldown to AGND, internally
DA_0–DA_7	16–9	Data Output Bank A; 3V/5V LVCMOS compatible
DB_0–DB_7	19–26	Data Output Bank B; 3 V/5V LVCMOS compatible
$DCLK_{OUT}$	28	Non-Inverted Data Output Clock; 3V/5V LVCMOS compatible
$\overline{DCLK_{OUT}}$	27	Inverted Data Output Clock; 3V/5V LVCMOS compatible
CLK	4	Non-Inverted Clock Input Pin; 100k pulldown to AGND, internally
$\overline{CLK}$	3	Inverted Clock Input Pin; 17.5k pullup to V_{CC} and 7.5k pulldown to AGND, internally
RESET	5	RESET synchronizes the data sampling and data output bank relationship when in Dual Channel Mode ($DMODE_1$ = 0); 100k pulldown to AGND, internally
$\overline{RESET}$	6	Inverted RESET Input Pin; 17.5k pullup to V_{CC} and 7.5 pulldown to AGND, internally
$DMODE_{1,2}$	32, 31	Internally:
		100k pulldown to AGND on $DMODE_1$ 50k pullup to V_{CC} on $DMODE_2$ Data Output Mode Pins: $DMODE_1$ = 0, $DMODE_2$ = 0: Parallel Dual Channel Output $DMODE_1$ = 0, $DMODE_2$ = 1: Interleaved Dual Channel Output $DMODE_1$ = 1, $DMODE_2$ = X: Single Channel Data Output on Bank A (125 MSPS max)
PD	2	Power Down Pin; PD = 1 for power-down mode. Outputs set to high impedance in power-down mode; 100k pulldown to AGND, internally
V_{CM}	37	2.5V Common Mode Voltage Reference Output
AV_{CC}	35, 36, 42, 43	+5V Analog Supply
OV_{DD}	7, 17, 30	+3V/+5V Digital Output Supply
AGND	1, 33, 34, 38, 41, 44	Analog Ground
DGND	8, 18, 29	Digital Ground

Ordering Information

Model	Part Number	Package
SPT7722	SPT7722SIT	TQFP-44

Temperature range for all parts: -40°C to +85°C.

Package Dimensions



TQFP-44						
	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A		0.472			12.00	
B		0.394			10.00	
C		0.394			10.00	
D		0.472			12.00	
E		0.031			0.80	
F	0.012		0.018	0.300		0.45
G	0.053		0.057	1.35		1.45
H	0.002		0.006	0.05		0.15
I	0.018		0.030	0.45		0.75
J		0.039			1.00	
K		0-7°			0-7°	

For additional information regarding our products, please visit the CADEKA at: cadeka.com

CADEKA Headquarters Loveland, Colorado
T: 970.663.5452
T: 877.663.5415 (toll free)

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