SPT5240

10-bit, 400 MWPS Current Output Digital-to-Analog Converter

Features

- 400 MWPS update rate
- Complementary current outputs
- +3.3 V power supply
- Low power dissipation:
  149mW (typ) @f_{CLK} = 400MHz and 12mA output
- Excellent AC performance:
  SFDR = 58dBc for f_{CLK} = 400MHz and f_{OUT} = 1.27 MHz
- Internal reference

Applications

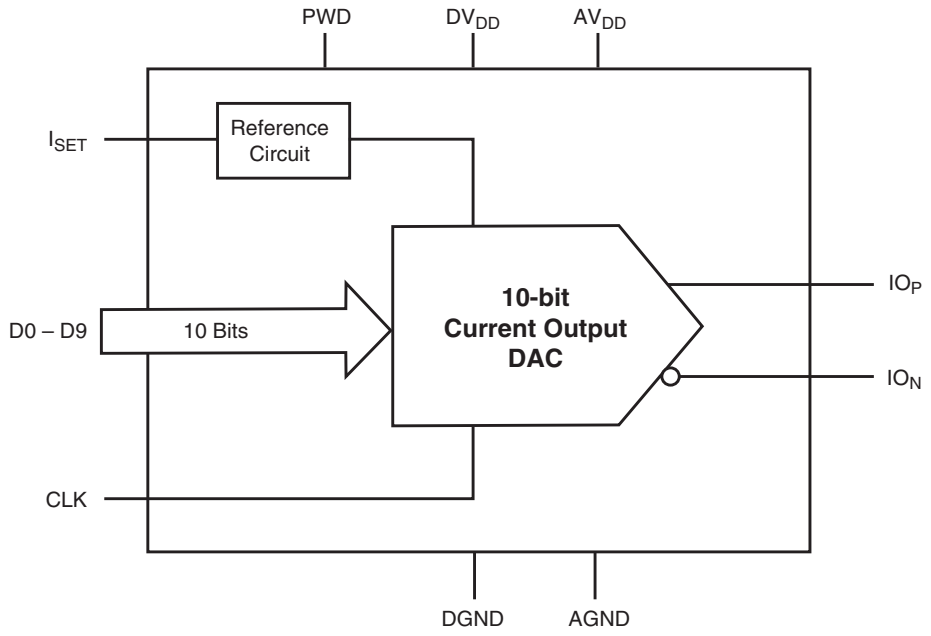
- Battery-operated devices
- Portable RF devices
- Set top boxes
- Video displays
- Broadband RF
- High-speed test equipment

Description

The SPT5240 is a 10-bit digital-to-analog converter that performs at an update rate of 400M words per second. The architecture achieves excellent high-frequency performance with very low power dissipation. This makes it ideal for all types of battery-operated equipment requiring high-speed digital-to-analog conversion.

The SPT5240 operates over an extended industrial temperature range from -40°C to +85°C and is available in a 32-lead LQFP package.

Functional Block Diagram



Electrical Specifications

(T_A = 25°C, AV_{DD} = 3.3V, DV_{DD} = 3.3V, f_{OUT} = 1.27MHz, f_{CLK} = 400MHz, Clock Duty Cycle = 50%, I_{OUT} = 20mA, R_L = 50Ω; unless otherwise noted)

Parameter	Conditions	Test Level	Min	Typ	Max	Units
DC Performance						
Resolution				10		Bits
Differential Linearity Error (DLE)	DC at IO_N	I	-1		2	LSB
Integral Linearity Error (ILE)	DC at IO_N	I	-4	±1.34	4	LSB
Offset Error	DC at both outputs	I	-.005		+.005	%FS
Full Scale Error	DC at both outputs	I	-15		+15	%FS
Gain Error	DC at both outputs	I	-15		+15	%FS
Maximum Full Scale Output Current		V		30		mA
Output Compliance Voltage		V		1.5		V
Output Impedance	Full-scale output	V		250		kΩ
Gain Error Tempco		V		±300		ppm FS/°C
AC Performance						
Maximum Clock Rate		IV	400			MHz
Glitch Energy	Major code transition	V		7		pV-s
Settling Time ($t_{settling}$)	See Figure 1, major code trans.	V		7.5		ns
Output Rise Time		V		1.3		ns
Output Fall Time		V		1.5		ns
Output Delay Time (t_D)	See Figure 1	V		1.8		ns
Spurious Free Dynamic Range (SFDR)		V		58		dBc
Total Harmonic Distortion (THD)		V		-55		dBc
Digital and Clock Data Input						
V_{IH} Minimum		V		2		V
V_{IL} Maximum		V		1		V
Logic “1” Current		I	-10		+10	µA
Logic “0” Current		I	-10		+10	µA
Input Setup Time (t_S)	See Figure 1	V		1		ns
Input Hold Time (t_H)	See Figure 1	V		1		ns
Clock Feedthrough		V		-29		dBFS

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection.

LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
IV	Parameter is guaranteed by design or characterization data.
V	Parameter is a typical value for information purposes only.

Electrical Specifications (Continued)

(T_A = 25°C, AV_{DD} = 3.3V, DV_{DD} = 3.3V, f_{OUT} = 1.27MHz, f_{CLK} = 400MHz, Clock Duty Cycle = 50%, I_{OUT} = 20mA, R_L = 50Ω; unless otherwise noted)

Parameter	Conditions	Test Level	Min	Typ	Max	Units
Power Supply Requirements						
Supply Voltage	$AV_{DD} = DV_{DD}$	IV	3.0	+3.3	3.6	V
Supply Current Sleep Mode						
AV_{DD}	25MHz Clock	V		9.5		mA
DV_{DD}	25MHz Clock	V		200		µA
Power Dissipation	20mA I_{OUT}	IV	170	195	215	mW
	12mA I_{OUT}	V		149		mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection.

LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
IV	Parameter is guaranteed by design or characterization data.
V	Parameter is a typical value for information purposes only.

Absolute Maximum Ratings (beyond which the device may be damaged)

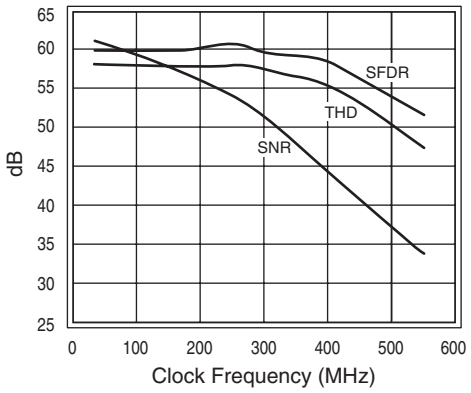
Parameter	Min	Max	Units
Supply Voltage			
AV_{DD}		3.7	V
DV_{DD}		3.7	V
Voltage Difference between AGND and DGND	-0.5	0.5	V
Voltage Difference between AV_{DD} and DV_{DD}	-0.5	0.5	V
Input Voltages			
D0 – D9	-0.5	DV_{DD} +0.5	V
CLK	-0.5	DV_{DD} +0.5	V
Junction Temperature		150	°C
Lead, soldering (10 seconds)		260	°C
Storage Temperature	-65	+150	°C
Thermal Resistance (Θ_{JA}) for 32 lead LQFP	64		°C/W

Note:
Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

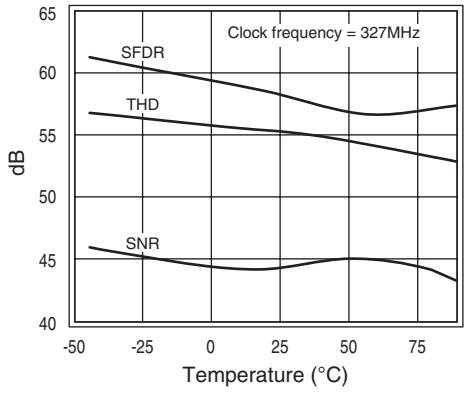
Typical Performance Characteristics

(T_A = 25°C, AV_{DD} = 3.3V, DV_{DD} = 3.3V, f_{OUT} = 1.27MHz, f_{CLK} = 400MHz, Clock Duty Cycle = 50%, I_{OUT} = 20mA, R_L = 50Ω; unless otherwise noted)

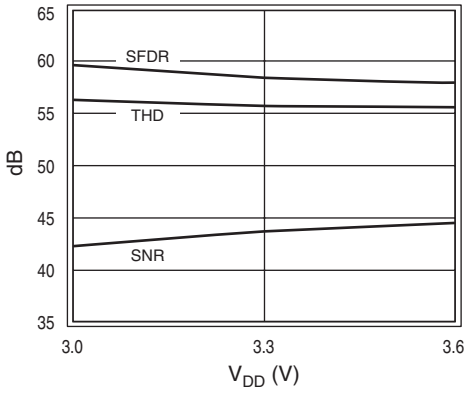
AC Performance vs. Clock Frequency



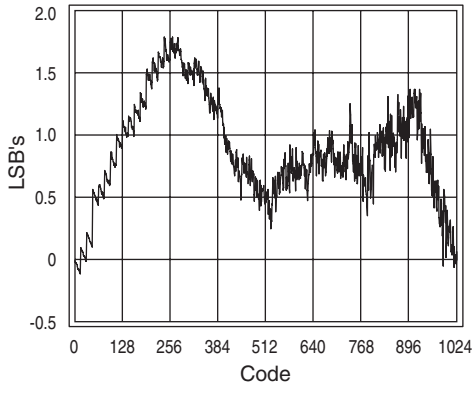
AC Performance vs. Temperature



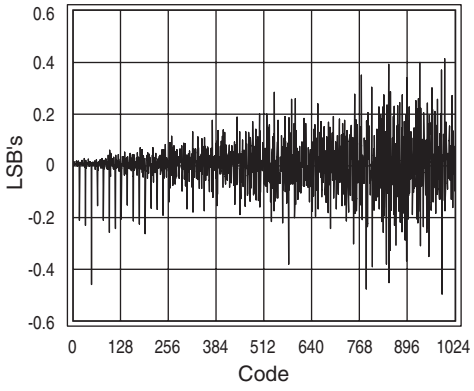
AC Performance vs. V_{DD}



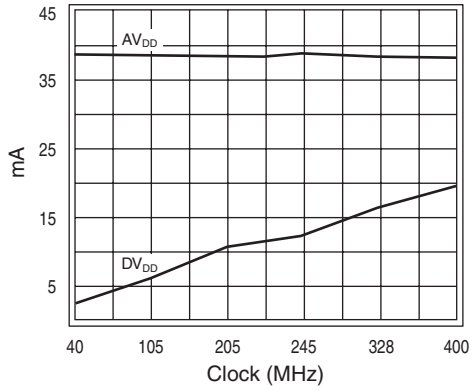
Intergral Nonlinearity vs. Code



Differential Nonlinearity vs. Code



AV_{DD}, DV_{DD} vs. Clock Frequency



Specification Definitions

Differential Linearity Error (DLE) or Differential Nonlinearity (DNL)

In an ideal DAC, output transitions between two adjacent codes are 1 LSB apart. Differential Linearity Error is the deviation, expressed in LSBs, from this ideal value.

Integral Linearity Error (ILE) or Integral Nonlinearity (INL)

The ideal transfer for a DAC is a straight line drawn between "zero-scale" output and "full-scale" output. ILE is the deviation of the output from the straight line. The deviation of the output at each code is measured and compared to the ideal output at that code. ILE may also be expressed as a sum of DLE starting from code 0…0 to the code that ILE measurement is desired.

Monotonic

A digital-to-analog converter is considered monotonic if the analog output never decreases as the code value at the input increases. A DLE less than -1 LSB would indicate a non-monotonic DAC.

Offset Error

The deviation, from ideal, at the DAC output when set to zero-scale. In the current output DAC there should be no current flow at zero-scale. Therefore, Offset Error is the amount of current measured with the DAC set to zero-scale.

Full-Scale Error

The ideal maximum full-scale current output of the DAC is determined by the value of R_{SET}. Full-scale error is the deviation of the output from ideal with the offset error included.

Gain Error

The ideal maximum full-scale current output of the DAC is determined by the value of R_{SET}. Gain error is the deviation of the output from ideal with the offset error removed.

Full-Scale Output

The maximum current output available for a given value of R_{SET}. In the SPT5240 IOP is full-scale at code 1111111111 and IO_N is full-scale at code 0000000000.

Zero-Scale Output

The minimum current output, ideally zero amps. In the SPT5240 IO_P is zero-scale at code 0000000000 and IO_N is zero-scale at code 1111111111.

Compliance Voltage

The maximum terminal output voltage for which the device will provide the specified current output characteristics.

Harmonic

1. Of a sinusoidal wave, an integer multiple of the frequency of the wave. ***Note:*** The frequency of the sine wave is called the fundamental frequency or the first harmonic, the second harmonic is twice the fundamental frequency, the third harmonic is three times the fundamental frequency, etc.

2. Of a periodic signal or other periodic phenomenon, such as an electromagnetic wave or a sound wave, a component frequency of the signal that is an integer multiple of the fundamental frequency. ***Note:*** The fundamental frequency is the reciprocal of the period of the periodic phenomenon.

Total Harmonic Distortion (THD)

The ratio of the sum of the power of first 9 harmonics above the fundamental frequency to the power of the fundamental frequency. Usually expressed in dBc.

Spurious Free Dynamic Range (SFDR)

The ratio of the fundamental sinusoidal power to the power of the single largest harmonic or spurious signal within the range of the 9th harmonic.

Clock Feedthrough

The ratio of the full-scale output to the peak-to-peak noise generated at the DAC output by input clock transitions. Expressed in dBFS.

Major Code Transition

The DAC code transition between 011…1 and 100…0 is referred to as major code transition. This transition often involves maximum number of internal circuit elements to switch states, resulting in worst DLE, ILE, glitch, etc.

Glitch Energy

A glitch is a switching transient that appears in the output of a DAC during a code transition. Glitch energy is measured as a product of the output voltage and time duration for major code transition, expressed in pV-s.

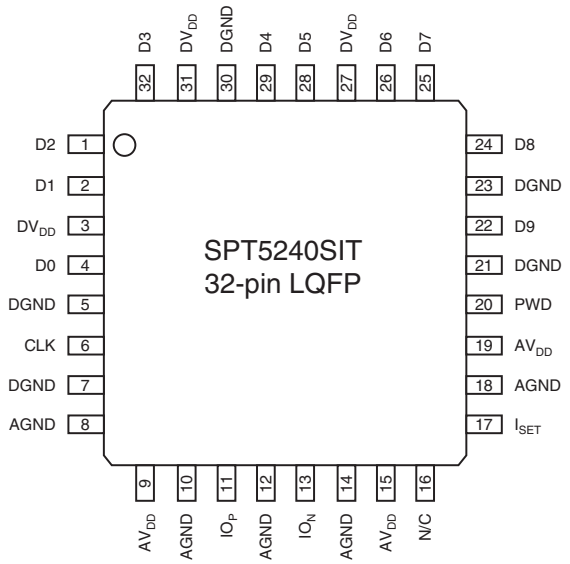
Output Rise Time

The amount of time for the output to change from 10% to 90% of the full-scale voltage, for a positive full scale transition from zero-scale to full-scale.

Output Fall Time

The amount of time for the output to change from 90% to 10% of the full-scale voltage, for a negative full scale transition from full-scale to zero-scale.

Pin Configuration



Pin Assignments

Analog Outputs

IO_P	DAC current output. Full-scale output at 11…11 input code.
IO_N	Complementary current output. Full-scale output at 00…00 input code.

Digital Inputs

D0 – D9	Digital inputs (D0 = LSB).
PWD	Power down mode pin. Active high. Internally pulled down.
CLK	Clock input pin. Data is latched on the rising edge.

Reference

I_{SET}	Full-scale adjust control. Connection for reference-current setting resistor.

Power

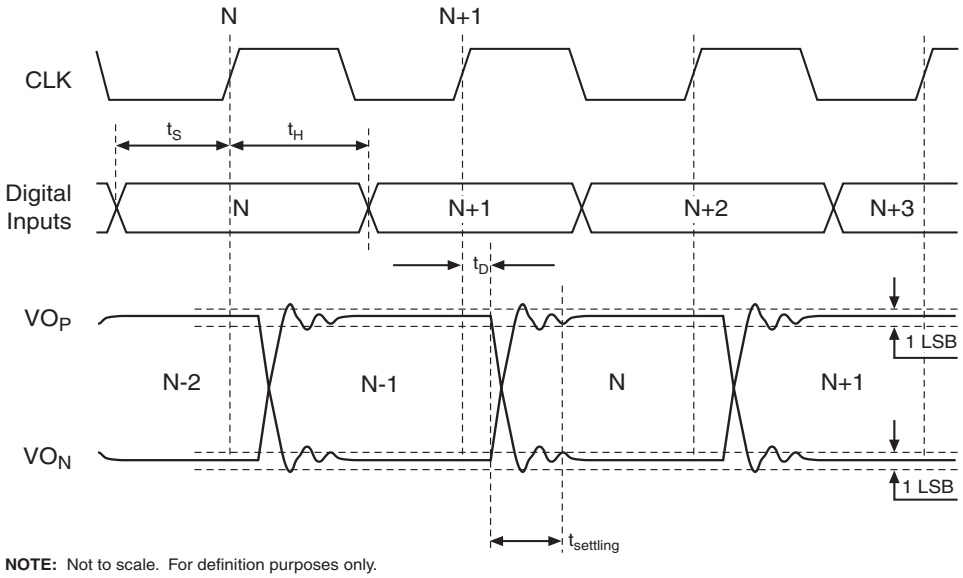
AGND	Analog Supply Ground.
DGND	Digital Supply Ground.
AV_{DD}	Analog +3.3V supply.
DV_{DD}	Digital +3.3V supply.
N/C	No Connect

Theory of Operation

The SPT5240 is a 10-bit 400 MWPS digital-to-analog converter. It integrates a DAC core with a bandgap reference and operates from a +3.3V power supply.

The DAC architecture is a compound differential current output DAC consisting of a 6-bit fully segmented DAC for the MSBs and a 4-bit fully segmented DAC for the LSBs. The input cell, followed by a master-slave latch, buffers the digital inputs. A 6:64 decoder decodes the digital data for the MSBs, and a 4:16 decoder does so for the LSBs. The outputs of the decoders are latched using a second bank of master-slave latches whose outputs then drive differential current switches, which steer the appropriate current to the IO_P or IO_N outputs.

The analog (AV_{DD}) and digital (DV_{DD}) power supplies are separated on chip to allow flexibility in the interface board. The analog (AGND) and digital (DGND) are separated on chip. Circuit board ground planes should be separated and tied together with a ferrite bead.



NOTE: Not to scale. For definition purposes only.

Figure 1: Timing Diagram

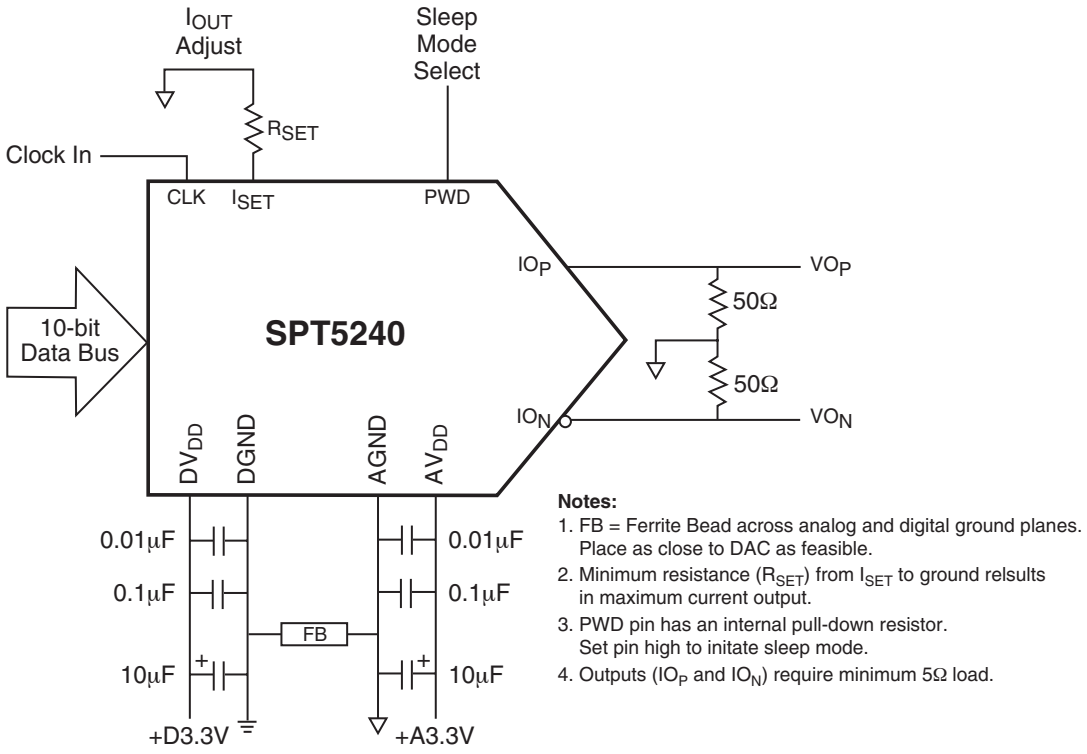


Figure 2: Typical Interface Circuit Diagram

Typical Interface Circuit

The SPT5240 requires few external components to achieve the stated performance. Figure 2 shows the typical interface requirements when used in normal circuit operation. The following sections provide descriptions of the major functions and outline performance criteria to consider for achieving optimal performance.

Digital Inputs

The SPT5240 has a 10-bit-wide parallel data input designed to work at +3.3V CMOS levels. Fast edges and low transients provide for improved performance.

Clock Input

The SPT5240 is driven by a single-ended clock circuit. In order to achieve best performance at the highest throughput, a clock generation circuit should provide fast edges and low jitter.

Input Protection

All I/O pads are protected with an on-chip protection circuit. This circuit provides robust ESD protection in excess of 3,000 volts, in human body model, without sacrificing speed.

Power Supplies and Grounding

The SPT5240 may be operated in the range of 3.0 to 3.6 volts. Normal operation is recommended to be separate analog and digital supplies operating at +3.3 volts. All power supply pins should be bypassed as close to the package as possible with the smallest capacitor closest to the device. Analog and digital ground planes should be connected together with a ferrite bead as shown in Figure 2 and as close to the DAC as possible.

Sleep Mode

To conserve power, the SPT5240 incorporates a power down function. This function is controlled by the signal on pin PWD. When PWD is set high, the SPT5240 enters the sleep mode. The analog outputs are both set to zero current output, resulting in less than 10mA current draw from the analog supply. For minimum power dissipation, data and clock inputs should be set to logic low or logic high.

Reference

The SPT5240 utilizes an on-chip bandgap reference to set full-scale output current level. The current reference to the DAC circuitry is set by the external resistance value between the I_{SET} pin and analog ground.

Analog Outputs

The SPT5240 provides differential current outputs which provide an output level based on the value of R_{SET} at maximum output code (see Figure 3). The required value of R_{SET} may be calculated using the formulas:

$$LSB = I_{FS}/1023$$

Then:

$$R_{SET} = \frac{1.111 - (1000 \bullet LSB)}{4 \bullet LSB}$$

Where I_{FS} is the desired full-scale current output.

Each output requires a minimum 5Ω load to analog ground. The typical circuit utilizes 50Ω loads to develop voltage for the output transformer (refer to EB5240 data sheet).

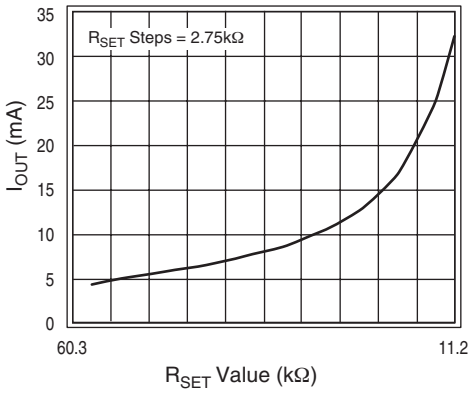


Figure 3: R_{SET} vs. I_{OUT}

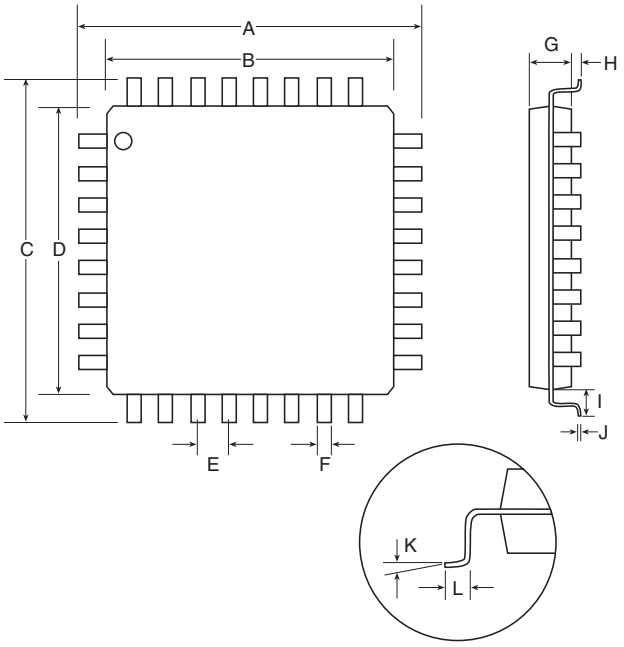
Table 1: Input Data Format

Input Code D9 – D0	Analog Output	
	IO_N	IO_P
0000000000	F_S	0
1111111111	0	F_S
Sleep XXXXXXXXXX	0	0

X indicates either data state.

Package Dimensions

LQFP-32



	INCHES		MILLIMETERS	
Symbol	Min	Max	Min	Max
A	0.346	0.362	8.80	9.20
B	0.272	0.280	6.90	7.10
C	0.346	0.362	8.80	9.20
D	0.272	0.280	6.90	7.10
E	0.031 Typ		0.80 BSC	
F	0.012	0.016	0.30	0.40
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.037	0.041	0.95	1.05
J		0.007		0.17
K	0°	7°	0°	7°
L	0.020	0.030	0.50	0.75

Ordering Information

Model	Part Number	Package	Container	Pack Qty
SPT5240	SPT5240SIT	32-pin LQFP	Tray	–

Temperature range for all parts: -40°C to +85°C.

For additional information regarding our products, please visit CADEKA at: cadeka.com

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