Data Sheet

CADEKA
Amplify the Human Experience

CDK1301

8-bit, 250 MSPS A/D Converter with Demuxed Outputs

FEATURES

- TTL/CMOS/PECL input logic compatible
- High conversion rate: 250 MSPS
- Single +5V power supply
- Very low power dissipation: 425mW
- 350MHz full power bandwidth
- Power-down mode: 24mW
- +3.0V/+5.0V (LVCMOS) digital output logic compatibility
- Single/demuxed output ports selectable
- Improved replacement for AD9054

APPLICATIONS

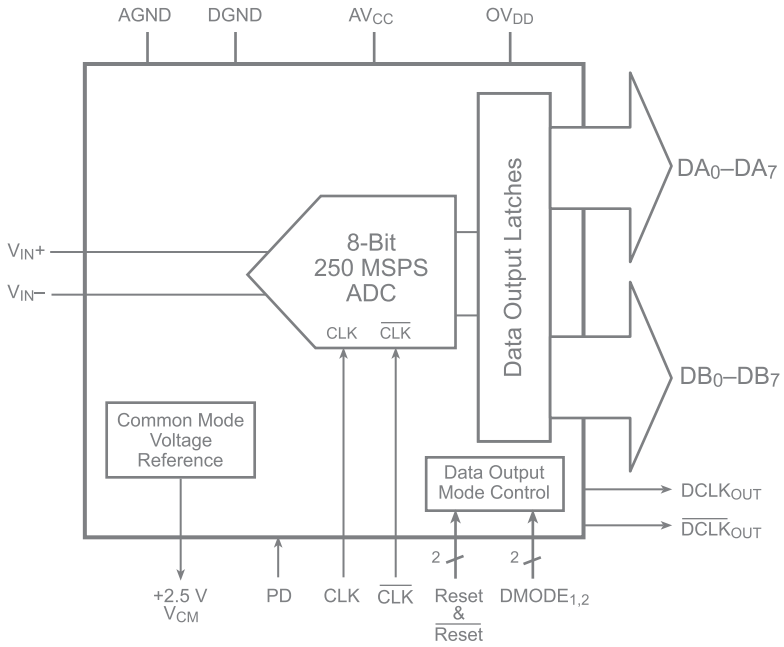
- RGB video processing
- Digital communications
- High-speed instrumentation
- Digital Sampling Oscilloscopes (DSO)
- Projection display systems

General Description

The CDK1301 is a high-speed, 8-bit analog-to-digital converter implemented in an advanced BiCMOS process. It is a performance-enhanced version of the CDK1300, offering better linearity and dynamic performance. An advanced folding and interpolating architecture provides both a high conversion rate and very low power dissipation of only 425mW. The analog inputs can be operated in either single-ended or differential input mode. A 2.5V common mode reference is provided on chip for the single-ended input mode to minimize external components.

The CDK1301 digital outputs are demuxed (double-wide) with both dual-channel and single-channel selectable output modes. Demuxed mode supports either parallel aligned or interleaved data output. The output logic is both +3.0V and +5.0V compatible. The CDK1301 is available in a 44-lead TQFP surface mount package over the industrial temperature range of -40°C to +85°C.

Block Diagram



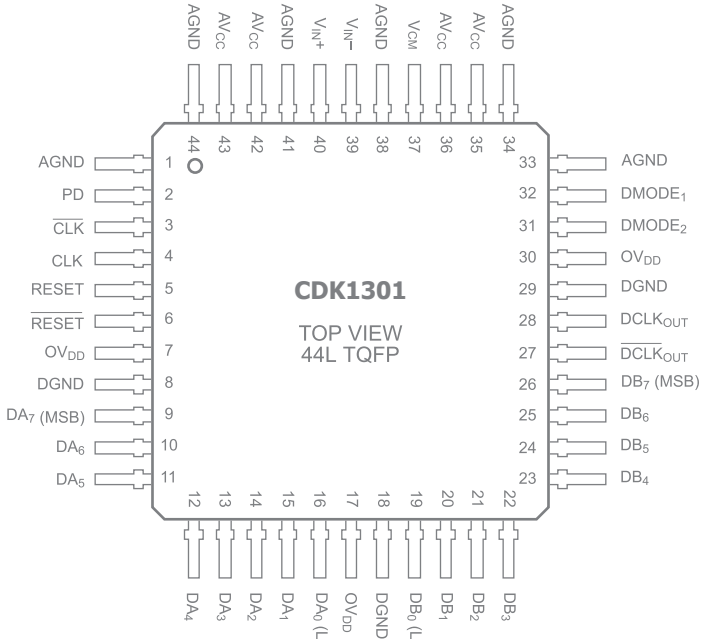
Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CDK1301ITQ44	TQFP-44	Yes	Yes	-40°C to +85°C	Rail
CDK1301ITQ44_Q	TQFP-44	No	No	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.

Pin Configuration

TQFP-44



Pin Assignments

Pin No.	Pin Name	Description
40	V_{IN+}	Non-inverted analog input; nominally $1V_{pp}$; 100k pullup to V_{cc} and 100k pulldown to AGND, internally
39	V_{IN-}	Inverted analog input; nominally $1V_{pp}$; 100k pullup to V_{cc} and 100k pulldown to AGND, internally
16-9	DA_0–DA_7	Data output bank A; 3V/5V LVCMOS compatible
19-26	DB_0–DB_7	Data output bank B; 3V/5V LVCMOS compatible
28	$DCLK_{OUT}$	Non-inverted data output clock; 3v/5v 3V/5V LVCMOS compatible
27	$\overline{DCLK_{OUT}}$	Inverted data output clock; 3V/5V LVCMOS compatible
4	CLK	Non-inverted clock input pin; 100k pulldown to AGND, internally
3	$\overline{CLK}$	Inverted clock input pin; 17.5k pullup to V_{CC} and 7.5k pulldown to AGND, internally
5	RESET	RESET synchronizes the data sampling and data output bank relationship when in dual channel mode ($DMODE_1$ = 0); 100k pulldown to AGND, internally
6	$\overline{RESET}$	Inverted RESET input pin; 17.5k pullup to V_{CC} and 7.5 pulldown to AGND, internally
32, 31	$DMODE_{1,2}$	Internally: 100k pulldown to AGND on $DMODE_1$ 50k pullup to V_{CC} on $DMODE_2$ Data output mode pins: $DMODE_1$ = 0, $DMODE_2$ = 0: parallel dual channel output $DMODE_1$ = 0, $DMODE_2$ = 1: interleaved dual channel output $DMODE_1$ = 1, $DMODE_2$ = x: single channel data output on bank a (125 MSPS max)
2	PD	Power-Down pin; PD = 1 for Power-Down mode. Outputs set to high impedance in Power-Down mode; 100k pulldown to AGND, internally
37	V_{CM}	2.5V common mode voltage reference output
35, 36, 42, 43	AV_{CC}	+5V analog supply
7, 17, 30	OV_{DD}	+3V/+5V digital output supply
1, 33, 34, 38, 41, 44	AGND	Analog ground
8, 18, 29	DGND	Digital ground

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage			
AV_{CC}		+6	V
OV_{DD}		+6	V
Input Voltages			
Analog inputs	-0.5V	V_{CC} +0.5V	V
Digital inputs	-0.5V	V_{CC} +0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Storage Temperature Range	-65		+125	°C

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C

Electrical Characteristics

(T_A = T_{Min} to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution			8		bits
DC Performance						
DLE	Differential Linearity Error	+25°C, f_{IN} = 1KHz(1)	-0.68	±0.4	0.68	LSB
		-40°C to +85°C, f_{IN} = 1KHz(2)	-0.95	±0.7	0.95	LSB
ILE	Integral Linearity Error	+25°C, f_{IN} = 1KHz(1)		±1.2	±1.90	LSB
		-40°C to +85°C, f_{IN} = 1KHz(2)		±1.4	±2.15	LSB
	No Missing Codes	@250 MSPS, f_{IN} = 1KHz(1)		Guaranteed		
Analog Input						
	Input Voltage Range	with respect to V_{IN-}		±512		mV_{pp}
V_{CM}	Input Common Mod(2)		2.0	2.5	3.0	V
	Input Bias Current	+25°C		13		µA
	Input Resistance	+25°C		50		kΩ
	Input Capacitance	+25°C		5		pF
	Input Bandwidth	+25°C (-3dB of FS)		350		MHz
	Gain Error(1)	+25°C	-7.5		+3.5	%FS
	Offset Error(1)	+25°C	-5		+5	LSB
PSRR	Offset Power Supply Rejection Ratio	AV_{cc} = 5V ±0.25V		<1		LSB
Timing Characteristics						
	Conversion Rate(2)		25	250		MSPS
t_{pd1}	Output Delay (Clock-to-Data)(2)	-40°C to +85°C	7	8	9.4	ns
	Output Delay Tempco			16		ps/°C
t_{ap}	Aperture Delay Time			0.3		ns
	Aperture Jitter Time			2.0		ps-RMS
	Pipeline Delay (Latency)					
	Single Channel Mode			2.5		Cycle
	Demuxed Interleaved Mode			2.5		Cycle
	Demuxed Parallel Mode					
	Channel B			2.5		Cycle
	Channel A			3.5		Cycle
	CLK to $DCLK_{OUT}$ Delay Time					
t_{pd2}	Single Channel Mode(2)		5.0	5.18	5.3	ns
t_{pd3}	Dual Channel Mode(2)		5.6	5.73	5.9	ns
	Output Delay (Clock to DClock)			18.1		ps/°C
Dynamic Performance						
ENOB	Effective Number of Bits	f_{IN} = 70MHz, +25°C(1)	6.4	7.0		Bits
		f_{IN} = 70MHz, -40°C to +85°C(2)	6.25	6.8		Bits
SNR	Signal-to-Noise Ratio	f_{IN} = 70MHz,+25°C(1)	44.3	46.1		dB
		f_{IN} = 70MHz, -40°C to +85°C(2)	42.6	45.4		dB
THD	Total Harmonic Distortion	f_{IN} = 70MHz, +25°C(1)		-47	-41.5	dB
		f_{IN} = 70MHz, -40°C to +85°C(2)		-45.5	-40.3	dB
SINAD	Signal-to-Noise and Distortion	f_{IN} = 70MHz, +25°C(1)	40.2	43.7		dB
		f_{IN} = 70MHz, -40°C to +85°C(2)	39.3	42.8		dB

Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

Electrical Characteristics

(T_A = T_{Min} to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Supply Requirements						
AV_{cc}	Analog Voltage Supply(2)		4.75	5.0	5.25	V
OV_{DD}	Digital Voltage Supply(2)		2.75		5.25	V
AI_{cc}	Current(1)			85	110	mA
	Current Power-down(1)	+25°C		4.8	5.5	mA
OI_{DD}	Current	OV_{DD} = 3.0V, 10pF load				
	Single Mode			35		mA
	Parallel Mode			55		mA
	Interleave Mode			55		mA
	Power Dissipation(1)			425	550	mW
Common Mode Reference Output						
	Voltage(1)		2.44	2.5	2.56	V
	Voltage Tempcp			84		ppm/°C
	Open Impedance	I_{OUT} = ±50µA		1.07		kΩ
PSRR	Power Supply Rejection Ratio			47.5		mV/V
Clock and Reset Inputs (Differential and Single-Ended)						
V_{DIFF}	Differential Signal Amplitude(2)		400			mV_{pp}
V_{IHD}	Differential High Input Voltage(2)		1.4		AV_{cc}	V
V_{ILD}	Differential Low Input Voltage(2)		0		3.9	V
V_{CMD}	Differential Common Mode Input(2)		1.2		4.1	V
V_{IH}	Single-Ended High Input Voltage(1)		1.8			V
V_{IL}	Single-Ended Low Input Voltage(2)		0		1.2	V
I_{IH}	High Input Current(1)	V_{ID} = 1.5V	-100	43	+100	µA
I_{IL}	Low Input Current(1)	V_{ID} = 1.5V	-100	43	+100	µA
Power Down and Mode Control Inputs (Single-Ended)						
	High Input Voltage(2)		2.0		AV_{cc}	V
	Low Input Voltage(2)		0		1.0	V
	Max Input Current Low(1)		-100	0.5	+100	µA
	Max Input Current High <4.0V(1)		-100	50	+100	µA
Digital Outputs						
	Logic "1" Voltage(1)	I_{OH} = -0.5mA	$OV_{DD-2.0}$			V
	Logic "0" Voltage(1)	I_{OL} = +1.6mA			0.2	V
	T_R/T_F Data	OV_{DD} = 3V, 10pF load		3.3/3.0		ns
		OV_{DD} = 5V, 10pF load		2.3/1.9		ns
	T_R/T_F DCLK	OV_{DD} = 3V, 10pF load		1.2/1.0		ns
		OV_{DD} = 5V, 10pF load		0.7/0.6		ns

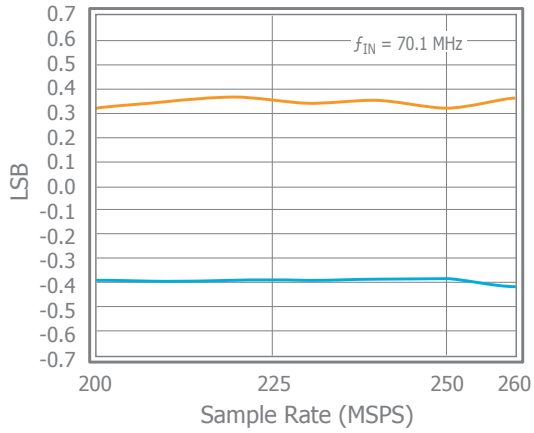
Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

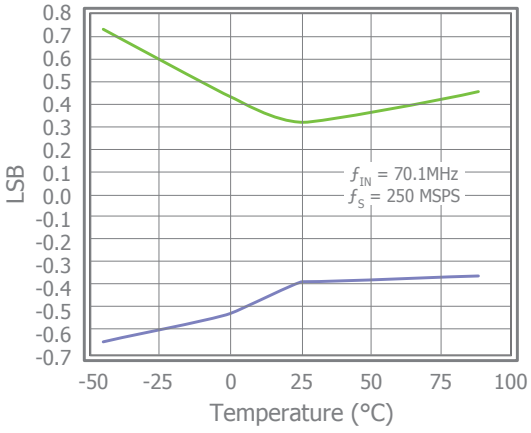
Typical Performance Characteristics

(T_A = T_{Min} to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

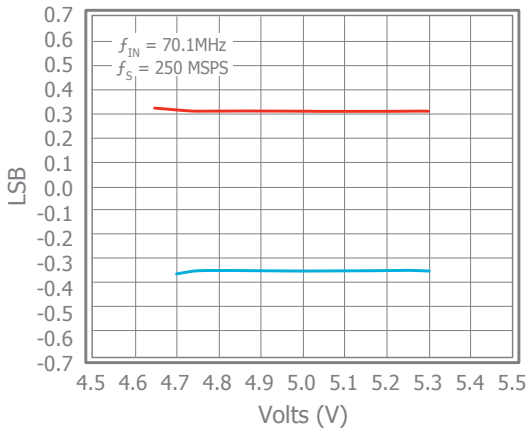
DLE vs. Sample Rate



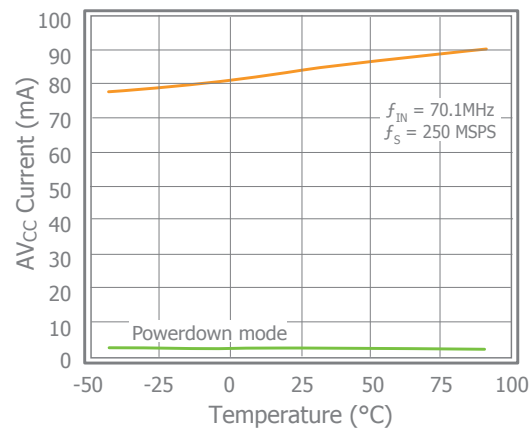
DLE vs. Temperature



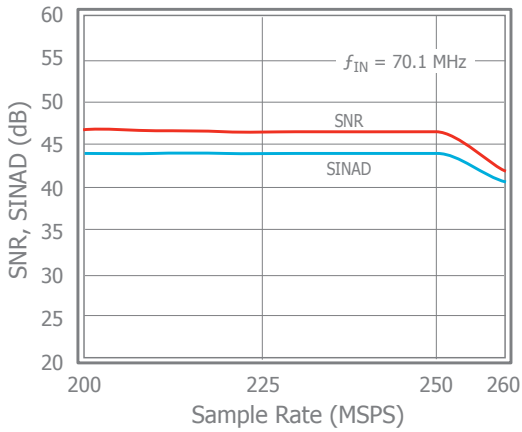
DLE vs. AV_{CC}



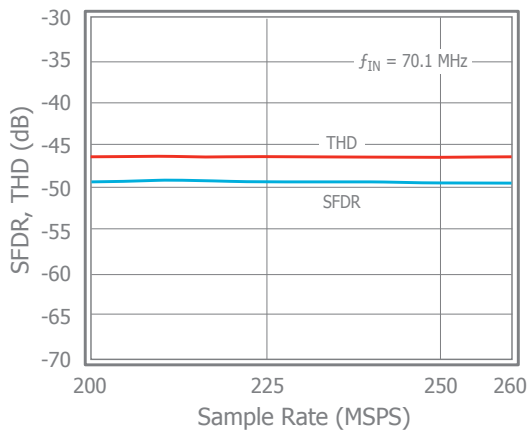
AV_{CC} Current vs. Temperature



SNR, SINAD vs. Sample Rate



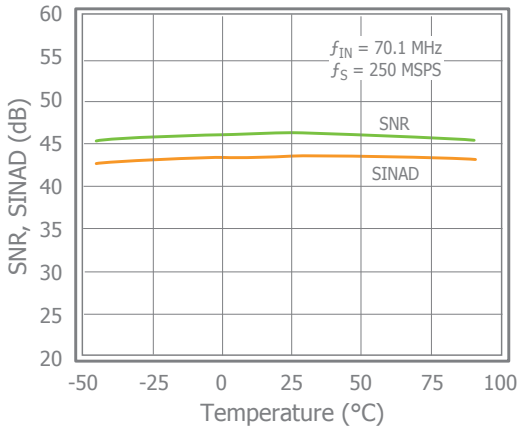
SFDR, THD vs. Sample Rate



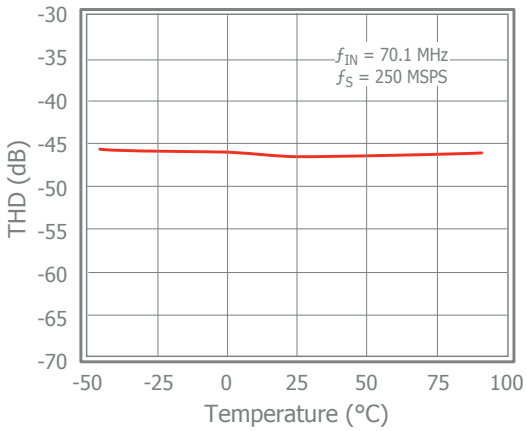
Typical Performance Characteristics

(T_A = T_{Min} to T_{Max}, AV_{CC}= +5V, OV_{DD} = +5V, f_{clk} = 250MHz, 50% duty cycle, f_{IN} = 70MHz, dual channel mode; unless otherwise noted)

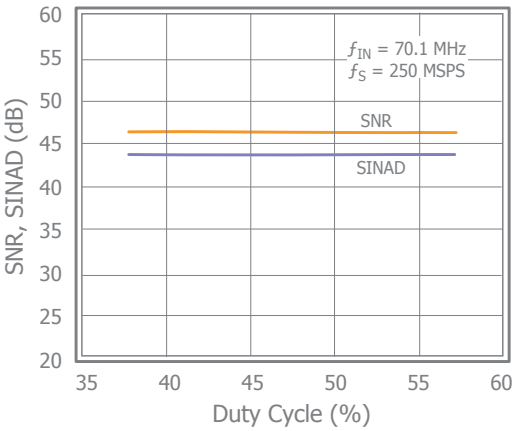
SNR, SINAD vs. Temperature



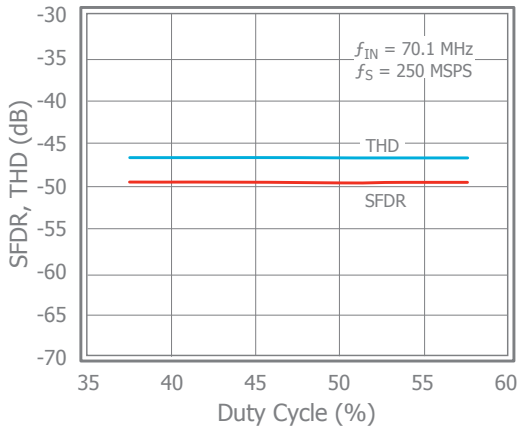
THD vs. Temperature



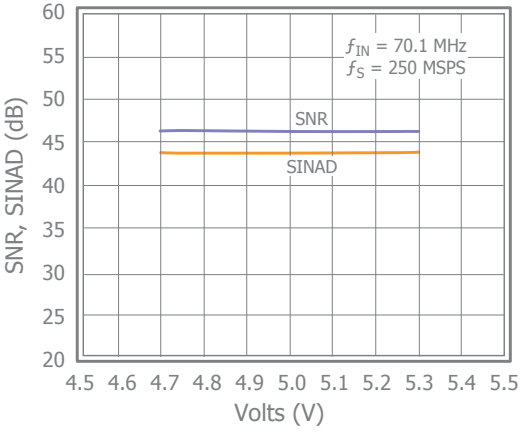
SNR, SINAD vs. Duty Cycle



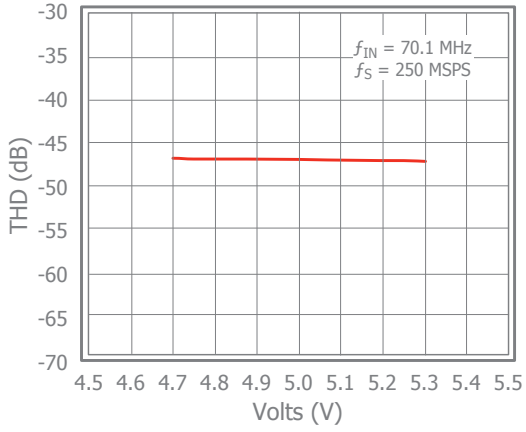
SFDR, THD vs. Duty Cycle



SNR, SINAD vs. AV_{CC}



THD vs. AV_{CC}



Theory of Operation

The CDK1301 is a three-step subranger. It consists of two THAs in series at the input, followed by three ADC blocks. The first block is a three-bit folder with over/under range detection. The second block consists of two single-bit folding interpolator stages. There are pipelining THAs between each ADC block.

The analog decode functions are the input buffer, input THAs, three-bit folder, folding interpolators, and pipelining THAs. The input buffer enables the part to withstand rail-to-rail input signals without latchup or excessive currents and also performs single-ended to differential conversion. All of the THAs have the same basic architecture. Each has a differential pair buffer followed by switched emitter followers driving the hold capacitors. The input THA also has hold mode feedthrough cancellation devices.

The three MSBs of the ADC are generated in the first threebit folder block, the output of which drives a differential reference ladder which also sets the full-scale input range. Differential pairs at the ladder taps generate midscale, quarter and three-quarter scale, overrange, and underrange. Every other differential pair collector is cross-coupled to generate the eighth scale zero crossings. The middle ADC block generates two bits from the folded signals of the previous stages after pipeline THAs. Its outputs drive more pipeline THAs to push the decoding of the three LSBs to the next half clock cycle. The three LSBs are generated in interpolators that are latched one full clock cycle after the MSBs.

The digital decode consists of comparators, exclusive of cells for gray to binary decoding, and/or cells used for mostly over/under range logic. There is a total of 2.5 clock cycles latency before the output bank selection. In order to reduce sparkle codes and maintain sample rate, no more than three bits at a time are decoded in any half clock cycle.

The output data mode is controlled by the state of the demux mode inputs. There are three output modes:

- All data on bank A with clock rate limited to one-half maximum
- Interleaved mode with data alternately on banks A and B on alternate clock cycles
- Parallel mode with bank A delayed one cycle to be synchronous with bank B every other clock cycle

If necessary, the input clock is divided by two. The divided clock selects the correct output bank. The user can synchronize with the divided clock to select the desired output bank via the differential RESET input.

The output logic family is CMOS with output OVDD supply adjustable from 2.7V to 5.25V. There are also differential clock output pins that can be used to latch the output data in single bank mode or to indicate the current output bank in demux mode.

Finally, a power-down mode is available, which causes the outputs to become tri-state, and overall power is reduced to about 24mW. There is a 2V reference to supply common mode for single-ended inputs that is not shut down in powerdown mode.

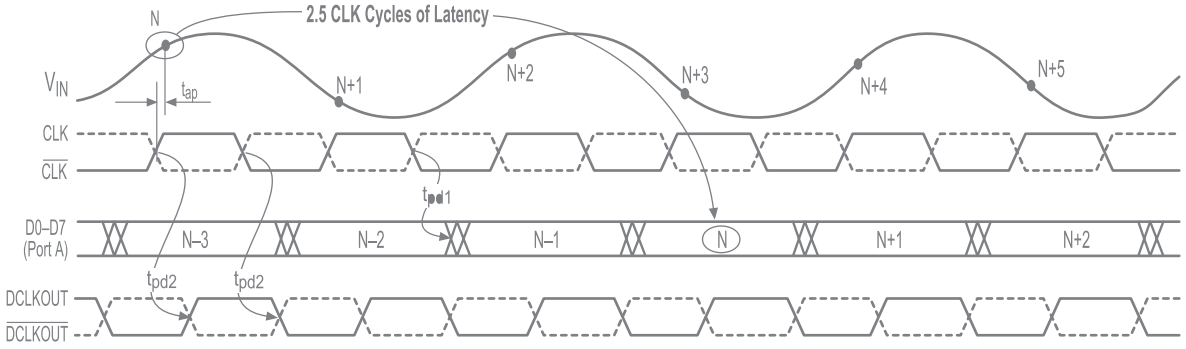


Figure 1. Single Mode Timing Diagram

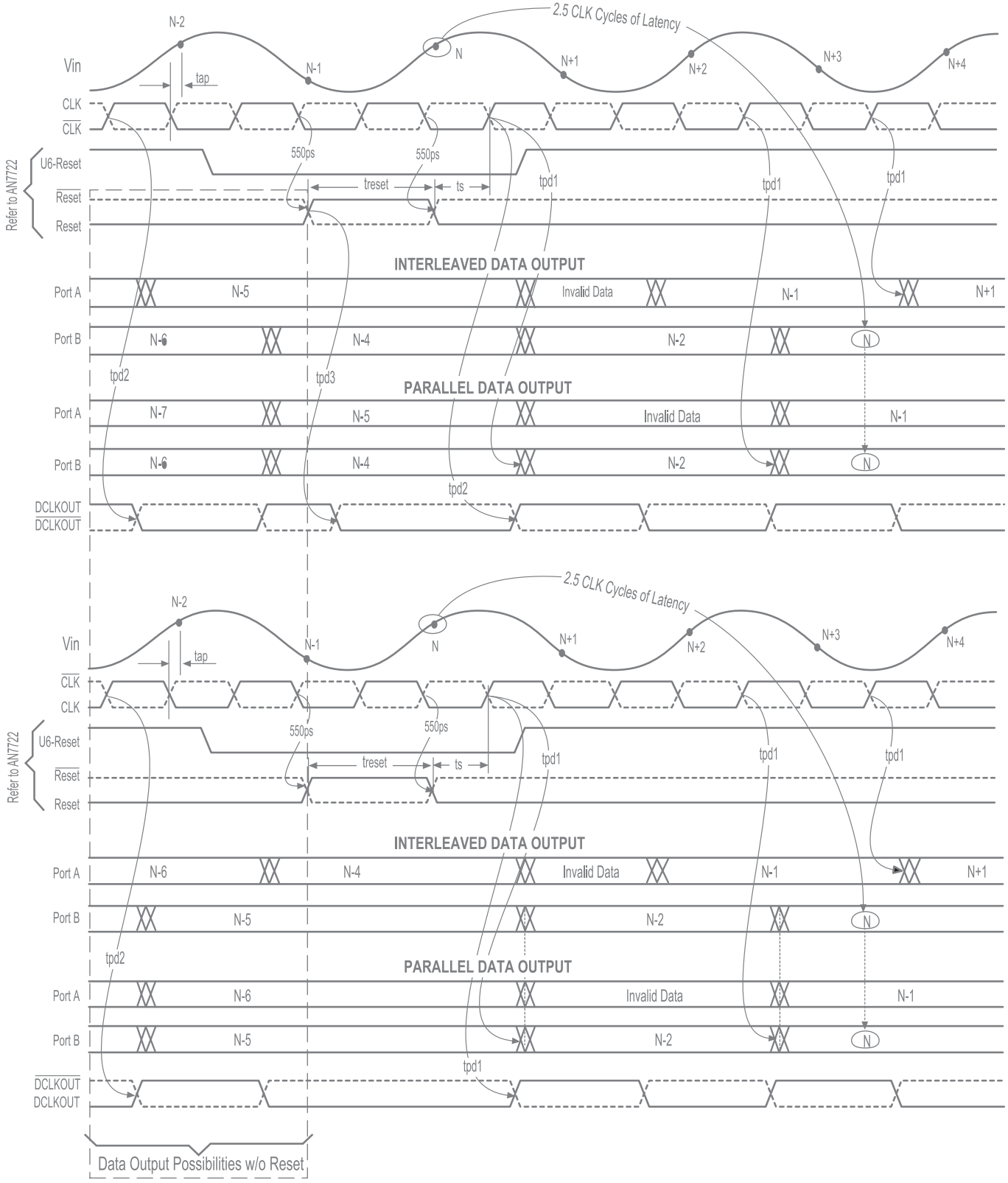
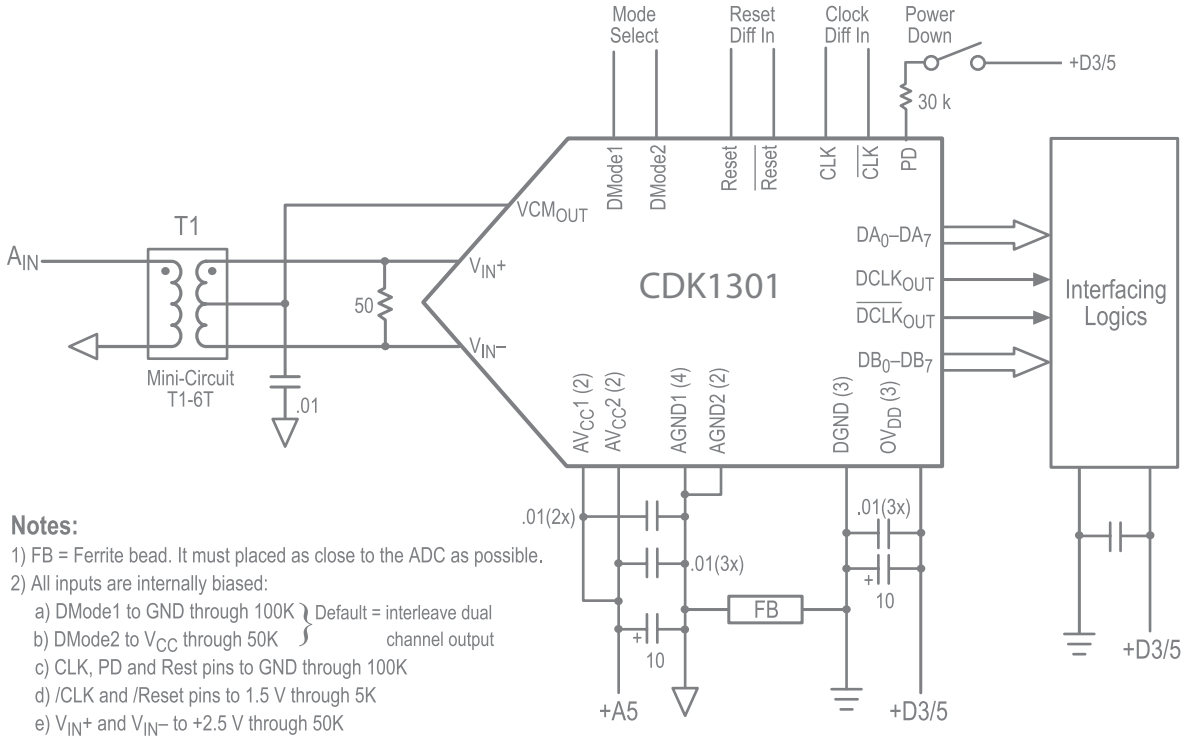


Figure 2. Dual Mode Timing Diagram



Notes:

1) FB = Ferrite bead. It must placed as close to the ADC as possible.
2) All inputs are internally biased:
   a) DMode1 to GND through 100K } Default = interleave dual
   b) DMode2 to V_{CC} through 50K } channel output
   c) CLK, PD and Rest pins to GND through 100K
   d) /CLK and /Reset pins to 1.5 V through 5K
   e) V_{IN}+ and V_{IN}– to +2.5 V through 50K
3) All 0.01microfarad capacitors are surface mount caps. They must be placed as close to the respective pin as possible

Figure 3. Typical Interface Circuit

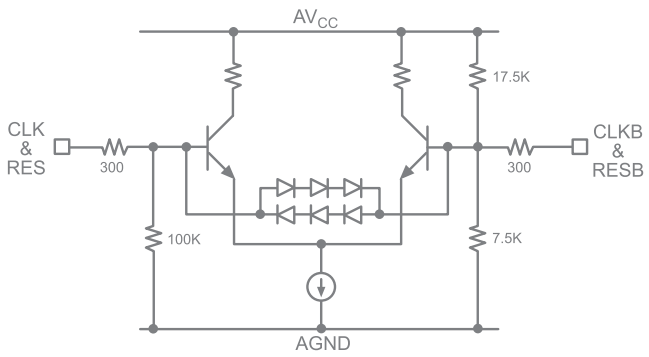


Figure 4. CLK and Reset Equivalent Circuit (without ESD Diodes)

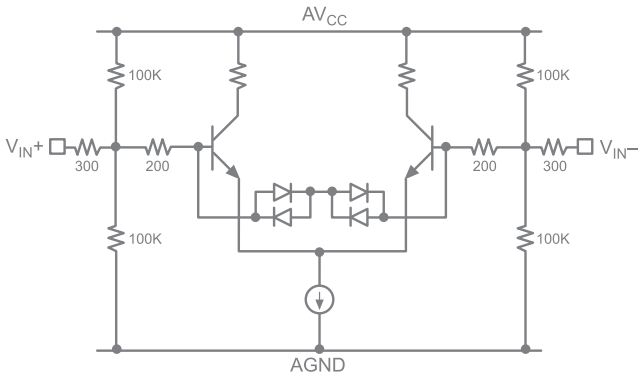


Figure 5. Analog Input Equivalent Circuit

Typical Interface Circuit

Very few external components are required to achieve the stated device performance. Figure 3 shows the typical interface requirements when using the CDK1301 in normal circuit operation. The following sections provide descriptions of the major functions and outline performance criteria to consider for achieving the optimal device performance.

Analog Input

The input of the CDK1301 can be configured in various ways depending on whether a single-ended or differential input is desired.

The AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the V_{CM} pin as shown in Figure 3. To obtain low distortion, it is important that the

selected transformer does not exhibit core saturation at the full-scale voltage. Proper termination of the input is important for input signal purity. A small capacitor across the input attenuates kickback noise from the internal track-and-hold.

Figure 6 illustrates a solution (based on operational amplifiers) that can be used if a DC-coupled single-ended input is desired.

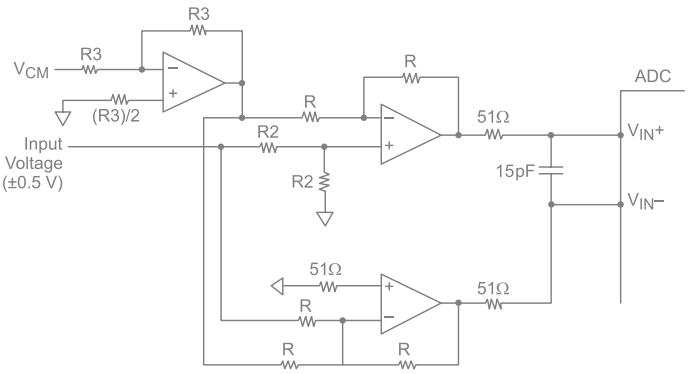


Figure 6. DC-Coupled Single-Ended to Differential Conversion (power supplies and bypassing are not shown)

Input Protection

All I/O pads are protected with an on-chip protection circuit. This circuit provides ESD robustness and prevents latchup under severe discharge conditions without degrading analog transmission times.

Power Supplies and Grounding

The CDK1301 is operated from a single power supply in the range of 4.75V to 5.25V. Normal operation is suggested to be 5.0V. All power supply pins should be bypassed as close to the package as possible. The analog and digital grounds should be connected together with a ferrite bead as shown in the typical interface circuit and as close to the ADC as possible.

Power-Down Mode

To save on power, the CDK1301 incorporates a power-down function. This function is controlled by the signal on pin PD. When pin PD is set high, the CDK1301 enters the power-down mode. All outputs are set to high impedance. In the powerdown mode the CDK1301 dissipates 24mW typically.

Common-Mode Voltage Reference Circuit

The CDK1301 has an on-board common-mode voltage reference circuit (V_{CM}). It is 2.5V and is capable of driving 50µA loads typically. The circuit is commonly used to drive the center tap of the RF transformer in fully differential applications. For single-ended applications, this output can be used to provide the level shifting required for the single-to-differential converter conversion circuit. Bypass V_{CM} to AGND by external 0.01µF capacitor, as shown in Figure 3 on the previous page.

Clock Input

The clock input on the CDK1301 can be driven by either a single-ended or double-ended clock circuit and can handle TTL, PECL, and CMOS signals. When operating at high sample rates it is important to keep the pulse width of the clock signal as close to 50% as possible. For TTL/CMOS single- ended clock inputs, the rise time of the signal also becomes an important consideration.

Digital Outputs

The output circuitry of the CDK1301 has been designed to be able to support three separate output modes. The demuxed (double-wide) mode supports either parallel aligned or interleaved data output. The single-channel mode is not demuxed and can support direct output at speeds up to 125 MSPS. The output format is straight binary (Table 1).

Table 1. Output Data Format

Analog Input	Output Code D7–D0
+FS	1111 1111
+FS - 1 LSB	1111 111Ø
+1 FS	1000 000Ø
-FS + 1 LSB	0000 000Ø
-FS	0000 0000

Ø indicates the flickering bit between logic 0 and 1

The data output mode is set using the $DMODE_1$ and $DMODE_2$ inputs (pins 32 & 31 respectively). Table 2 describes the mode switching options.

Table 2. Output Data Modes

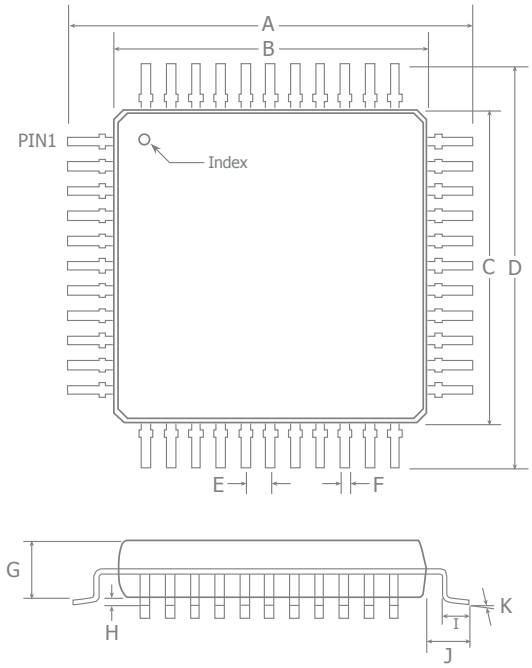
Output Mode	$DMODE_1$	$DMODE_2$
Parallel Dual Channel Output	0	0
Interleaved Dual Channel Output	0	1
Single Channel Data Output (Bank A only 125 MSPS max)	1	X

Evaluation Board

The TBD evaluation board is available to aid designers in demonstrating the full performance of the CDK1301. This board includes a clock driver and reset circuit, adjustable references and common mode, a single-ended to differential input buffer and a single-ended to differential transformer (1:1). An application note (TBD) describing the operation of this board, as well as information on the testing of the CDK1301, is also available. Contact the factory for price and availability of the TBD.

Mechanical Dimensions

TQFP-44 Package



TQFP-44						
	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A		0.472			12.00	
B		0.394			10.00	
C		0.394			10.00	
D		0.472			12.00	
E		0.031			0.80	
F	0.012		0.018	0.300		0.45
G	0.053		0.057	1.35		1.45
H	0.002		0.006	0.05		0.15
I	0.018		0.030	0.45		0.75
J		0.039			1.00	
K		0-7°			0-7°	

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