

# KH600

## 1GHz, Differential Input/Output Amplifier

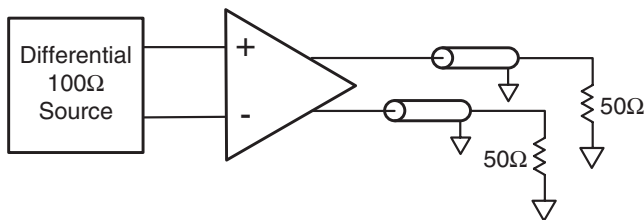
### Features

- DC - 1GHz bandwidth
- Fixed 14dB (5V/V) gain
- 100Ω (differential) inputs and outputs
- -74/-64dBc 2nd/3rd HD at 50MHz
- 45mA output current
- 9V<sub>pp</sub> into 100Ω differential load
- 13,000V/μs slew rate
- Optional supply current and offset voltage adjustment

### Applications

- ATE systems
- High-end instrumentation
- High bandwidth output amplifier
- Differential buffer
- Line driver

### Typical Application



The KH600 includes 50Ω resistors from each input to ground (resulting in a differential input impedance of 100Ω).

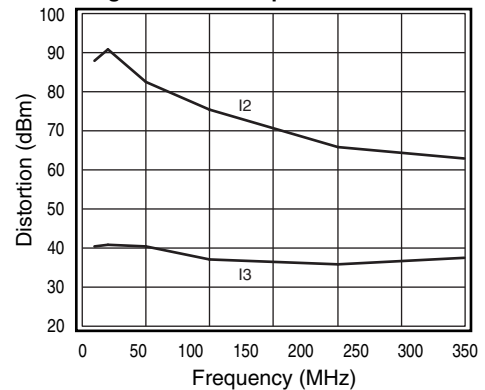
### Description

The KH600 is the first amplifier to combine differential input and output with a bandwidth of DC-1GHz at 2V<sub>pp</sub>. The inputs and outputs are 100Ω differential (50Ω single ended). The KH600 operates from ±5V supplies and offers a fixed gain of 14dB (5V/V).

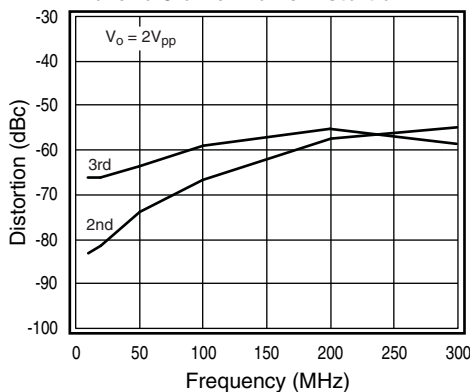
The KH600 also offers optional supply current, differential output offset voltage, and common mode offset voltage adjustments.

The KH600 is constructed using Cadeka's in-house thin film resistor/bipolar transistor technology. The KH600 is available in a 12-pin TO-8 package.

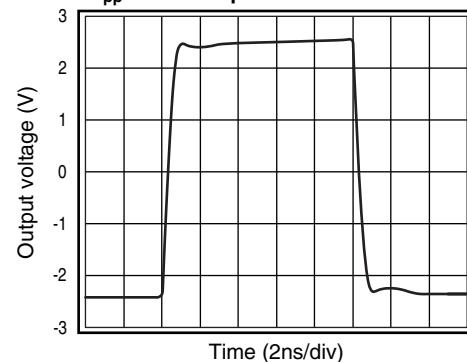
Single Tone Intercept Point



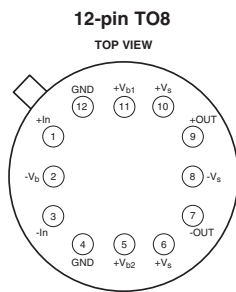
2nd and 3rd Harmonic Distortion



5V<sub>pp</sub> Pulse Response



## Pin Assignments



NOTE: Case is grounded.

## Pin Definitions

Pin Number	Pin Name	Pin Function Description
6, 10	+V <sub>S</sub>	Positive supply voltage
8	-V <sub>S</sub>	Negative supply voltage
11	+V <sub>b1</sub>	Positive bias voltage for OUT1
5	+V <sub>b2</sub>	Positive bias voltage for OUT2
2	-V <sub>b</sub>	Negative bias voltage for OUT1 and OUT2
1	IN1	Input 1, +IN
3	IN2	Input 2, -IN
9	OUT1	Output 1, +OUT
7	OUT2	Output 2, -OUT
4, 12	GND	Input termination ground and case

## Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Total Supply Voltage	–	15	V
Maximum Junction Temperature	–	+150	°C
Storage Temperature Range	-65	+150	°C
Lead Temperature, 10 seconds	–	+300	°C

## Electrical Specifications

( $G = +5V/V$  (14dB),  $R_L = 100\Omega$  (differential),  $T_a = +25^\circ C$ ,  $+V_{b1} = +V_{b2} = +V_S = +5V$ ,  $-V_b = -V_S = -5V$ ; unless noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Frequency Domain Response</b>					
-3dB Bandwidth	$V_O = 2V_{pp}$		1000		MHz
Peaking	DC to 250MHz		0.2		dB
	DC to 500MHz		0.5		dB
Full Power Bandwidth	$V_O = 8V_{pp}$		350		MHz
Linear Phase Deviation	DC to 500MHz		3		deg
Gain	1MHz		14		dB
	DC <sup>1</sup>	14.2	14.3	14.4	dB
Input Return Loss (SE $50\Omega$ ) <sup>2</sup>	DC = 250MHz		22		dB
	DC = 500MHz		14		dB
Output Return Loss (SE $50\Omega$ ) <sup>2</sup>	DC = 500MHz		27		dB
<b>Time Domain Response</b>					
Rise and Fall Time	2V step		350		ps
	8V step		1		ns
Overload Recovery	$V_{in} = 4V_{pp}$		900		ps
Slew Rate	8V step		13,000		V/ $\mu s$
<b>Distortion and Noise Response</b>					
2nd Harmonic Distortion	$5V_{pp}$ , 50MHz		61		dBc
	$2V_{pp}$ , 50MHz <sup>1</sup>	61	74		dBc
	$1V_{pp}$ , 200MHz		65		dBc
3rd Harmonic Distortion	$5V_{pp}$ , 50MHz		46		dBc
	$2V_{pp}$ , 50MHz <sup>1</sup>	57	64		dBc
	$1V_{pp}$ , 200MHz		70		dBc
Input Referred Noise	>1MHz		1.35		nV/ $\sqrt{Hz}$
Noise Figure			6.5		dB
<b>DC Performance</b>					
Output Offset Voltage	I/Os terminated $50\Omega$ to GND <sup>1</sup>	-60	-18	+60	mV
Average Drift			200		$\mu V/^\circ C$
Power Supply Rejection Ratio ( $\pm V_S$ )	DC		55		dB
Supply Current	$\pm V_S$ pins <sup>1</sup>		67	70	mA
	$\pm V_b$ pins ( $+V_{b1}$ shorted to $+V_{b2}$ ) <sup>1</sup>		22	24	mA
<b>Output Characteristics</b>					
Output Voltage Swing	differential		9		$V_{pp}$
Output Current			$\pm 45$		mA
<b>Recommended Operating Conditions</b>					
Total Supply Voltage	( $+V_S$ to $-V_S$ )		4 to 12		V
$-V_b$			0 to -12		V
$+V_{b1}$ , $+V_{b2}$			0 to -12		V
Input Voltage (Relative to Gain)			$\pm 2$		V

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

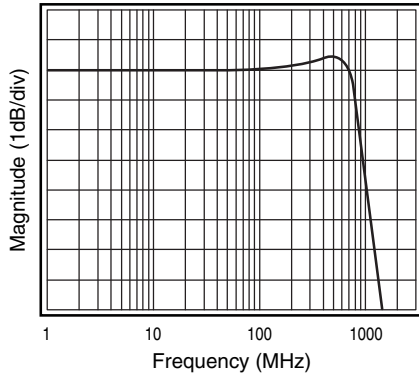
### Notes:

- 100% tested at  $25^\circ C$ .
- SE = Single-Ended.

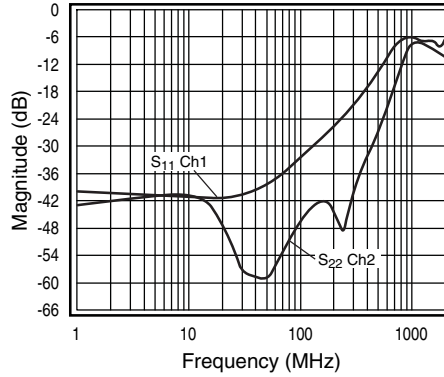
# Typical Operating Characteristics

( $G = +5V/V$  (14dB),  $R_L = 100\Omega$  (differential),  $T_a = +25^\circ C$ ,  $+V_{b1} = +V_{b2} = +V_s = +5V$ ,  $-V_b = -V_s = -5V$ ; unless noted)

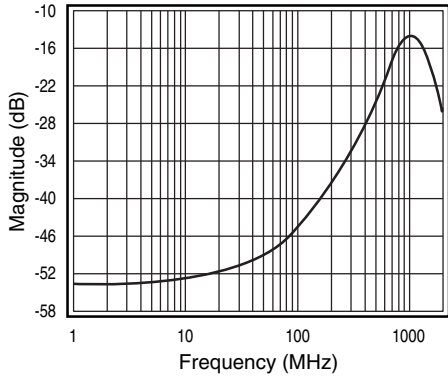
**Small Signal AC Response ( $S_{21}$ )**



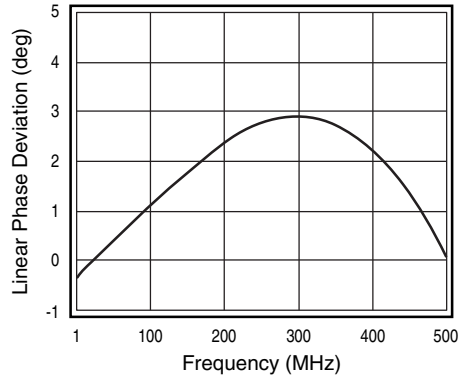
**Input and Output Return Loss ( $S_{11}/S_{22}$ )**



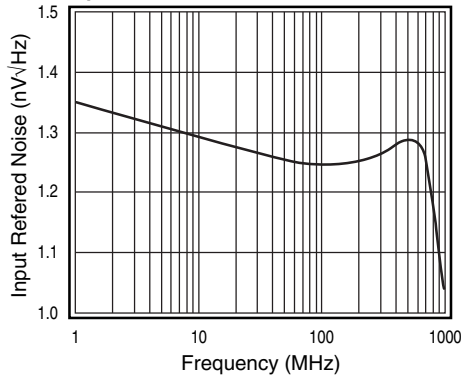
**Reverse Isolation ( $S_{12}$ )**



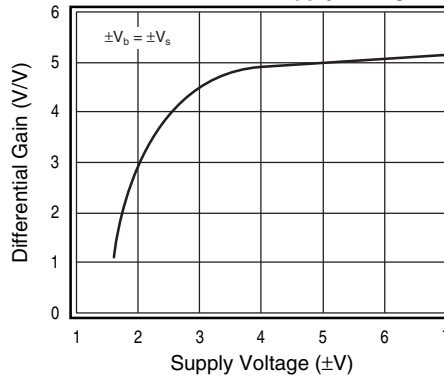
**Linear Phase Deviation**



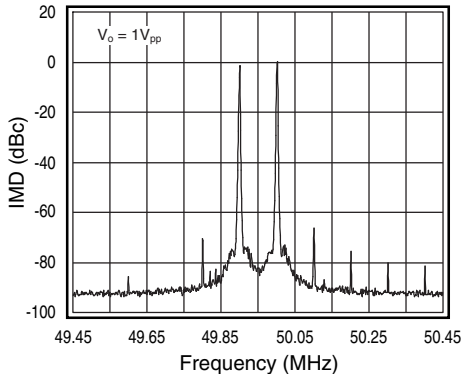
**Input Noise**



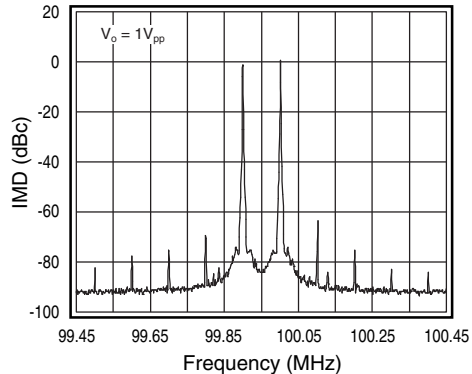
**Differential Gain vs. Supply Voltage**



**2 Tone 3rd Order Intermod. Distortion**

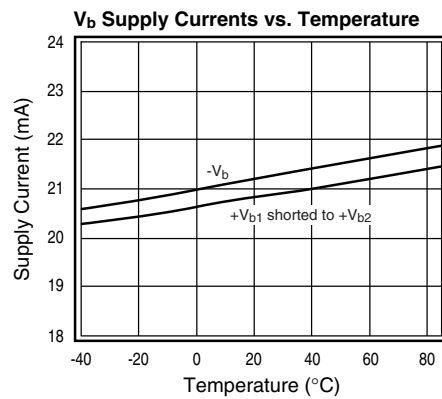
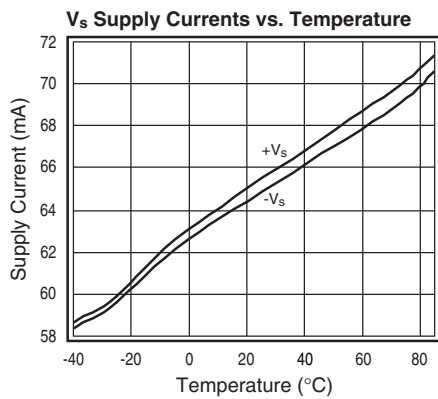
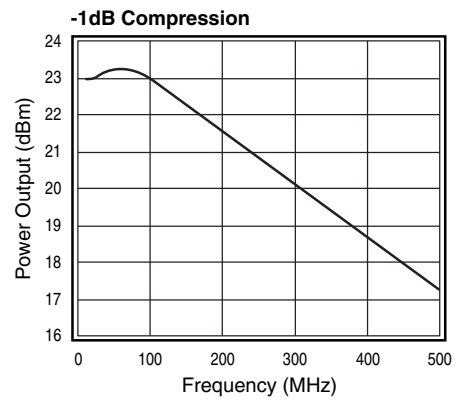
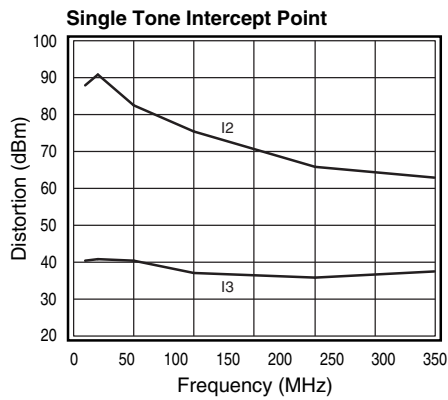
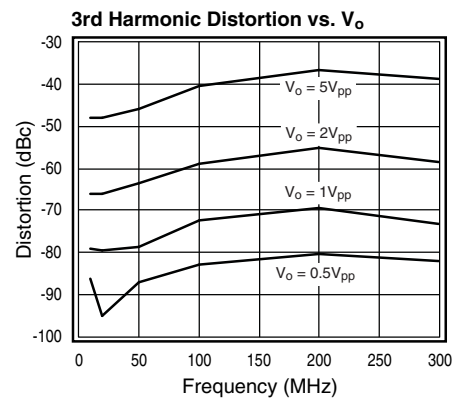
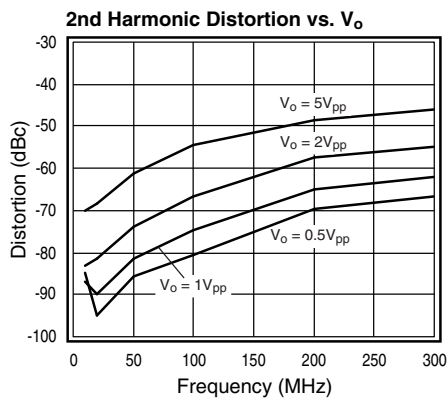
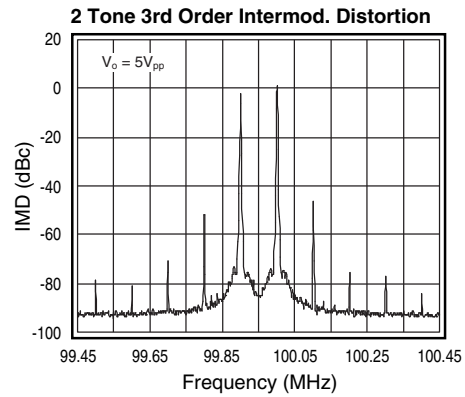
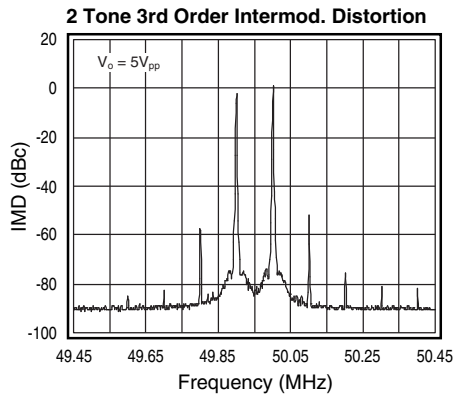


**2 Tone 3rd Order Intermod. Distortion**



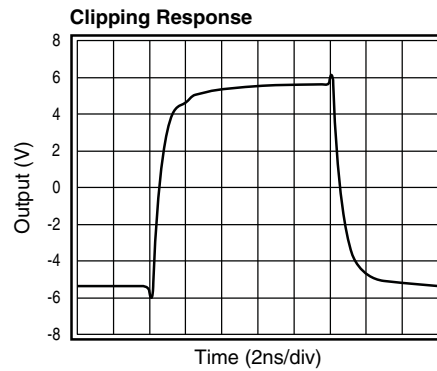
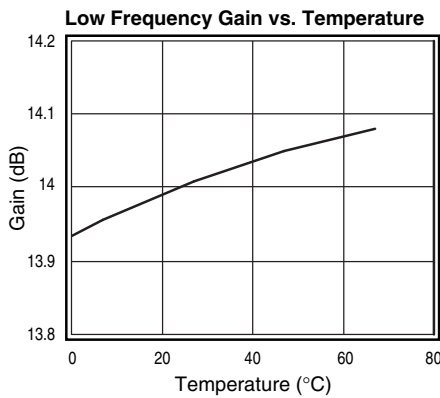
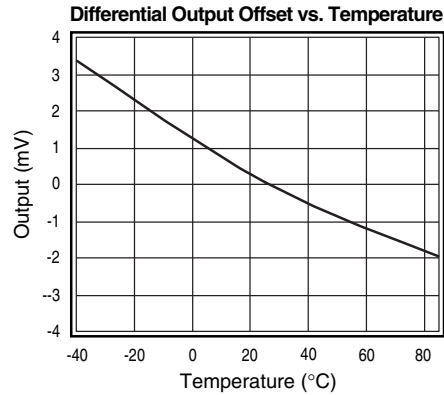
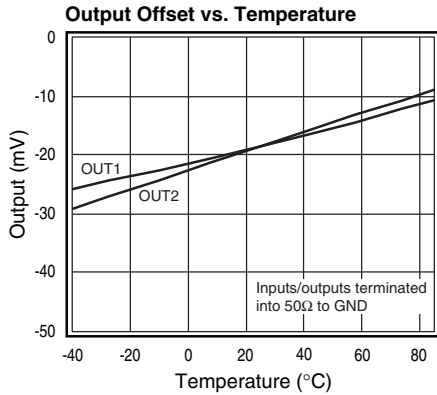
# Typical Operating Characteristics

( $G = +5V/V$  (14dB),  $R_L = 100\Omega$  (differential),  $T_a = +25^\circ C$ ,  $+V_{b1} = +V_{b2} = +V_s = +5V$ ,  $-V_b = -V_s = -5V$ ; unless noted)



## Typical Operating Characteristics

(G = +5V/V (14dB),  $R_L = 100\Omega$  (differential),  $T_a = +25^\circ\text{C}$ ,  $+V_{b1} = +V_{b2} = +V_s = +5\text{V}$ ,  $-V_b = -V_s = -5\text{V}$ ; unless noted)



## Functional Description

The circuit is a differential amplifier with current output and feedback. The simplified schematic is shown in Figure 1. The output impedance is set by the value of the feedback resistors (R3-R6) and the gain of the current mirrors. Amplifier gain is set by R1 and R2. All of these resistors are internal due to the high bandwidth of the amplifier.

The common mode output voltage (both outputs together) can be varied by changing the voltages on  $+V_{b1}$ ,  $+V_{b2}$  and  $-V_b$ . Making all three voltages more negative (for instance,  $+V_b$ 's change from +5 to +3, and  $-V_b$  changes from -5 to -7) will cause the output common mode level to become more positive. The opposite conditions will cause the output common mode level to become more negative. This can be very useful in driving differential circuits which have an elevated DC common mode input level. See *Adjusting Common Mode Output Offset Voltage* section for more details.

By varying  $+V_{b1}$  and  $+V_{b2}$  differentially, the differential output offset can be adjusted. See *Trimming Differential Output Offset Voltage* for more details.

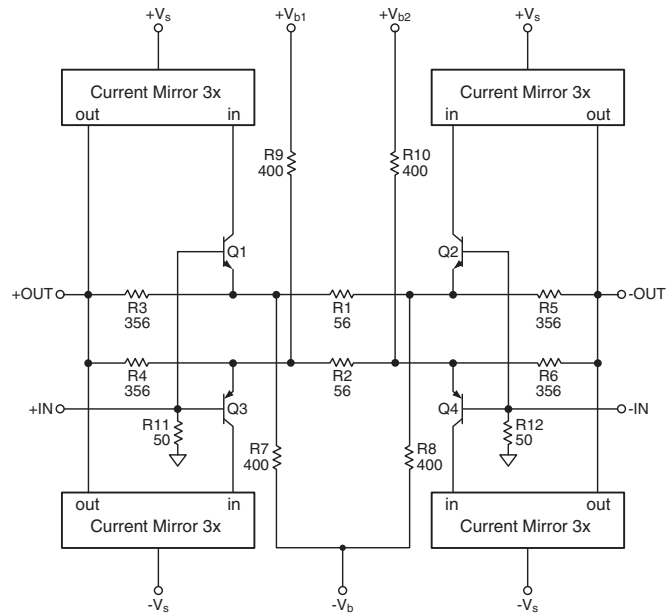


Figure 1: KH600 Simplified Schematic

# Application Information

## General Description

Standard Operation:

$$+V_{b1} = +V_{b2} = +V_s = +5V;$$

$$-V_b = -V_s = -5V$$

The KH600 is a 1GHz differential input/output amplifier constructed using Cadeka's in-house thin film resistor/bipolar transistor technology. A differential signal on the inputs of the KH600 will generate a differential signal at the outputs. If a single ended input signal is applied to IN1 and a fixed voltage to IN2, the KH600 will produce both a differential and common-mode output signal. To achieve the maximum dynamic range, center the inputs halfway between +V<sub>S</sub> and -V<sub>S</sub>.

The KH600 includes 50Ω resistors from each input to ground, resulting in a differential input impedance of 100Ω. Each KH600 output has a 50Ω resistance, synthesized by feedback, providing a 100Ω differential output impedance.

The KH600 has 3 bias voltage pins that can be used to:

- Adjust the supply current
- Trim the differential output offset voltage
- Adjust the common mode output offset voltage over a ±3V range

If these adjustments are not required, short +V<sub>b1</sub> and +V<sub>b2</sub> to +V<sub>S</sub> and -V<sub>b</sub> to -V<sub>S</sub> as shown in Figure 2. Throughout this data sheet, this configuration (+V<sub>b1</sub> = +V<sub>b2</sub> = +V<sub>S</sub> = +5V and -V<sub>b</sub> = -V<sub>S</sub> = -5V) is referred to as the Standard Operating Condition. All of the plots in the Typical Performance section and the specifications in the Electrical Characteristics table utilize the basic circuit configuration shown in Figure 2, unless otherwise indicated. Figure 3 illustrates the optional circuit configuration, utilizing the bias voltage pins. Further discussions regarding these optional adjustments are provided later in this document.

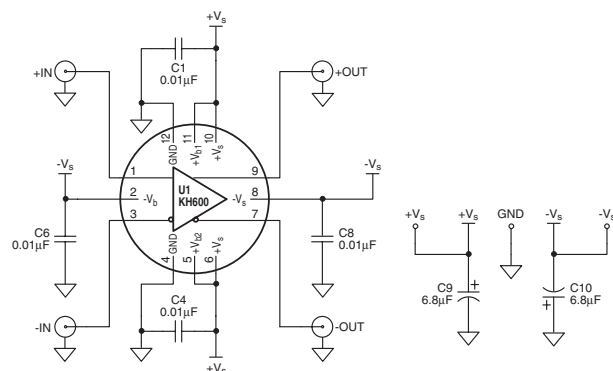


Figure 2: Basic Circuit Configuration

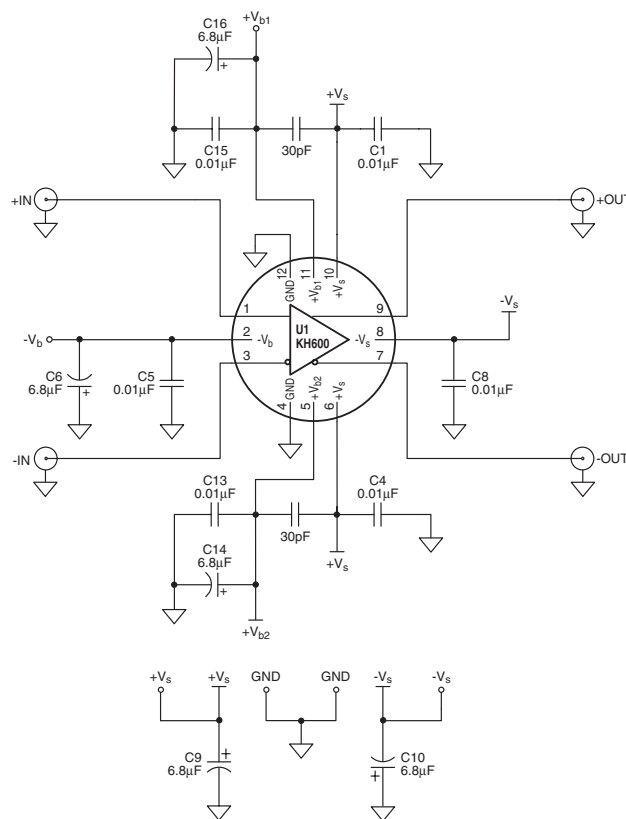


Figure 3: Optional Circuit Configuration (including optional supply current and offset adjust)

## Gain

Differential Gain for the KH600 is defined as (OUT1– OUT2)/(IN1–IN2). Applying identical (same phase) signals to both inputs and measuring one output will provide the Common Mode Gain. Figure 4 shows the differential and common mode gains of the KH600. Figure 5 illustrates the response of the KH600 outputs when one input is driven and the other is terminated into 50Ω.

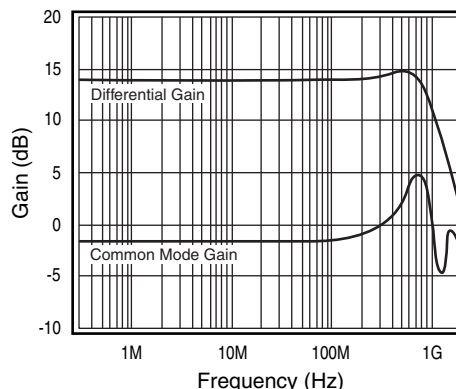


Figure 4: Differential and Common Mode Gain

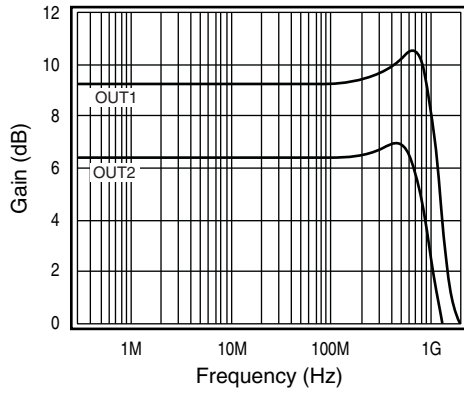


Figure 5: Gain with Single-Ended Input Applied to IN1

Supply Current

The KH600 draws supply current from the 2  $V_s$  pins as well as the 3  $V_b$  pins. Under Standard Conditions, the total supply current is typically 89mA. Changing the voltages on the bias voltage pins will change their respective supply currents as shown in Figures 6 and 7

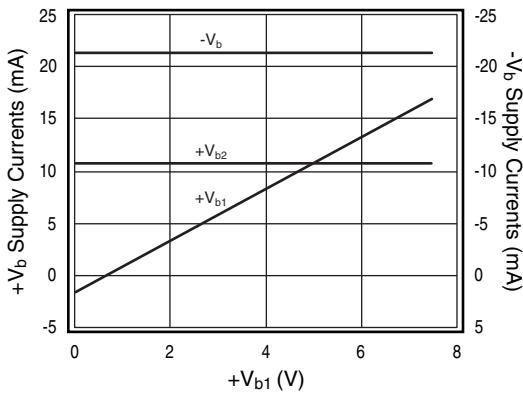


Figure 6:  $V_b$  Supply Currents vs.  $+V_{b1}$

Changing the voltage on the  $+V_{b1}$  pin will alter the supply current for  $+V_{b1}$  only,  $+V_{b2}$  and  $-V_b$  stay constant at typically 11mA and 22mA respectively. See Figure 6. The same principle applies for  $+V_{b2}$ . And Figure 7 illustrates the effect of changing  $-V_b$ .

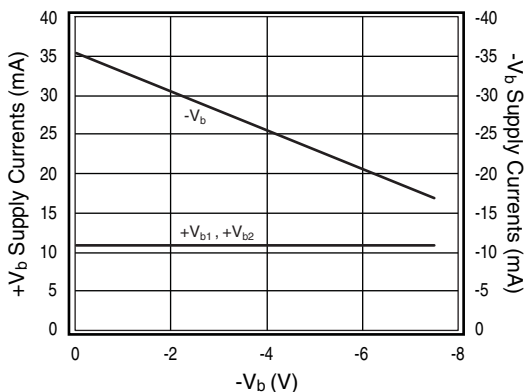


Figure 7:  $V_b$  Supply Currents vs  $-V_b$

Power Dissipation

The KH600 runs at “constant” power, which may be calculated by  $(Total I_s)(V_s - (-V_s))$ . Under standard operating conditions, the power is 890mW. The power dissipated in the package is completely constant, independent of signal level. In other words, the KH600 runs class A.

Power Supply Rejection Ratio (PSRR)

The KH600 has 5 supply pins,  $+V_s$ ,  $-V_s$ ,  $+V_{b1}$ ,  $+V_{b2}$ , and  $-V_b$ . All of these sources must be considered when measuring the PSRR. Figure 8 shows the response of  $+V_s$  and  $-V_s$ , looking at OUT2.  $+V_s$  and  $-V_s$  have the same effect on OUT1.

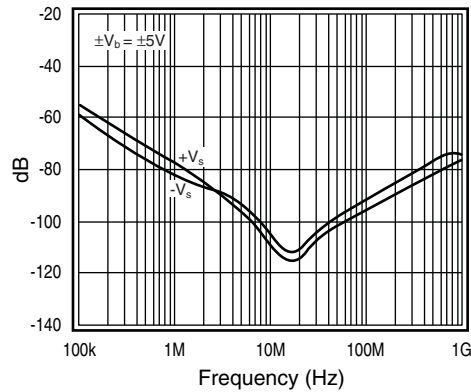


Figure 8:  $\pm V_s$  PSRR

Figure 9 shows the response of OUT1 and OUT2 when  $+V_{b1}$  changes. The PSRR of the  $V_b$  pins is “bad”, which means that they have a large effect on the response of the KH600 when their voltages are changed. This is the desired effect of the bias voltage pins. As Figure 9 indicates, changing  $+V_{b1}$  has a greater effect on OUT1 than it does on OUT2. Changing  $+V_{b1}$  has a direct effect on OUT1. Changing  $+V_{b2}$  has a direct effect on OUT2. See the Trimming Differential Output Offset Voltage section for more details.

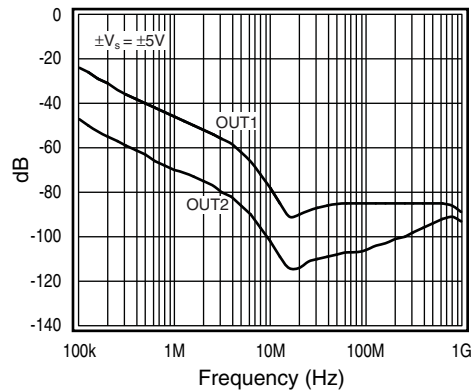


Figure 9:  $+V_b$  PSRR

## Single-to-Differential Operation

The KH600 is specifically designed for differential-to-differential operation. However, the KH600 can be used in a single-to-differential configuration with some performance degradation. The unused input should be terminated into  $50\Omega$ . When driven single-ended, there will be a slight imbalance in the differential output voltages, see Figure 5. This imbalance is approximately 2.88dB. To compensate for this imbalance, attenuate the higher gain output. (If the signal is applied to IN1, attenuate OUT1.)

## Unused Inputs and/or Outputs

For optimal performance, terminate any unused inputs and/or outputs with  $50\Omega$ .

## Adjusting Supply Current

The KH600 operates class A, so maximum output current is directly proportional to supply current. Adjusting the voltages on  $+V_{b1}$  and  $+V_{b2}$  in opposition to  $-V_b$  controls supply current. The default supply current of the KH600 has been optimized for best bandwidth and distortion performance. The main reason for adjusting supply current is to either reduce power or increase maximum output current. Adjusting the supply current will not significantly improve bandwidth or distortion and may actually degrade them.

To adjust the supply current, apply voltages of equal magnitude, but opposite polarity, to the bias voltage pins. For example, setting  $+V_{b1}$ ,  $+V_{b2}$  to +5VDC and  $-V_b$  to -5VDC (as shown in Figure 3) results in the standard supply current condition. Setting  $+V_{b1}$ ,  $+V_{b2}$  to +5.5V and  $-V_b$  to -5.5V results in an approximate 10% increase in supply current. Figure 10 shows the how the total supply current of the KH600 is effected by changes in the bias voltages ( $V_b = +V_{b1} = +V_{b2} = |-V_b|$ ).

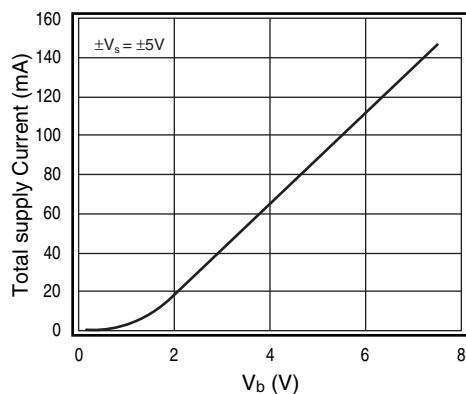


Figure 10: Total Supply Current vs.  $V_b$

Supply current is relatively independent of the voltages on  $+V_s$  and  $-V_s$  as shown in Figure 11.

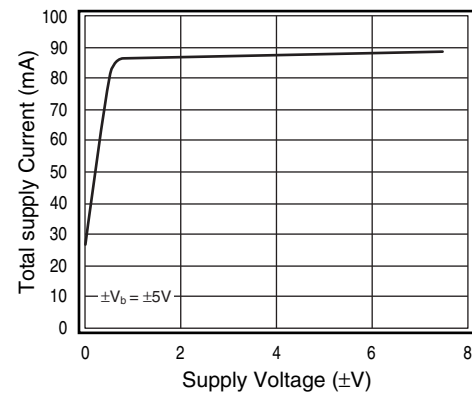


Figure 11: Total Supply Current vs.  $V_s$

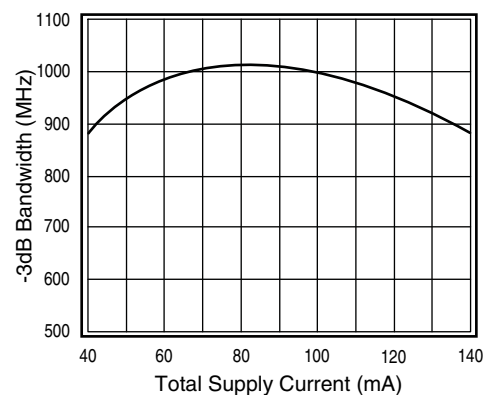


Figure 12: -3dB Bandwidth vs.  $I_s$

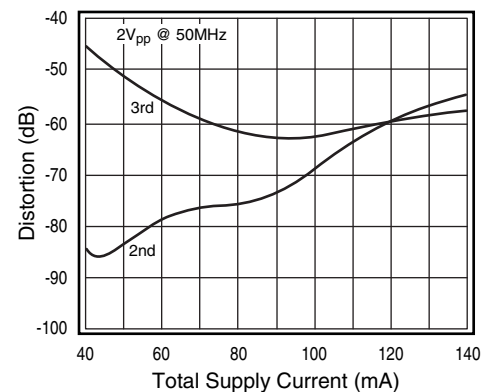


Figure 13: Harmonic Distortion vs. Total  $I_s$

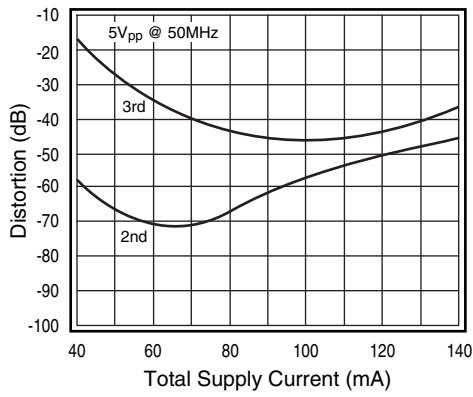


Figure 14: Harmonic Distortion vs. Total  $I_s$

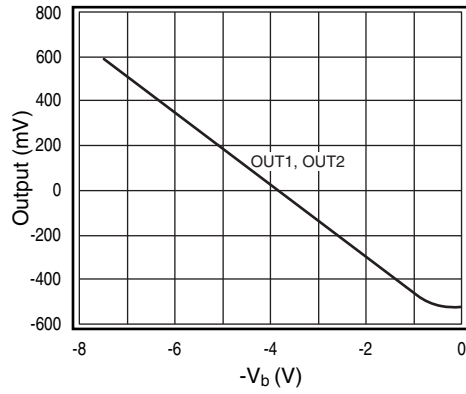


Figure 17: Output vs.  $-V_b$

**Trimming Differential Output Offset Voltage**

Vary  $+V_{b1}$  and  $+V_{b2}$  to adjust differential offset voltage.  $+V_{b1}$  controls OUT1 and  $+V_{b2}$  controls OUT2. The output voltage moves in a direction opposite to the direction of the bias voltage. Figure 15 shows the resulting voltage change at OUT1 and OUT2 when the voltage on  $+V_{b1}$  is changed. Figure 16 shows the resulting voltage change at OUT1 and OUT2 when the voltage on  $+V_{b2}$  is changed. OUT1 and OUT2 change at the same rate when  $-V_b$  is changed, as shown in Figure 17. Therefore, changing the voltage on  $-V_b$  has no effect on differential output offset voltage.

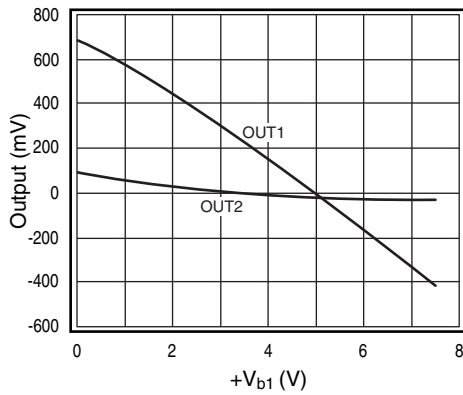


Figure 15: Output vs.  $+V_{b1}$

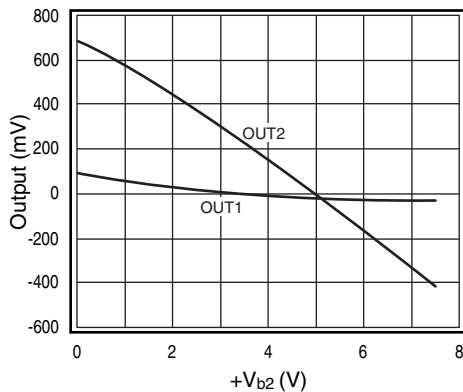


Figure 16: Output vs.  $+V_{b2}$

**Adjusting Common Mode Output Offset Voltage**

Short  $+V_{b1}$  to  $+V_{b2}$  and vary  $+V_b$  and  $-V_b$  to adjust common mode output offset voltage. The recommended values for achieving a given output offset are shown in Figure 18. These values were chosen to give the best distortion performance. The exact values are not crucial.

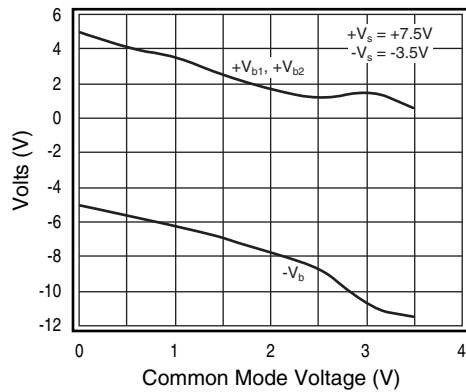


Figure 18:  $V_b$  vs. Common Mode Voltage

For common mode voltages of 0 to  $-3.5V$  swap the  $V_b$ 's and change the polarity. See the example below.

Desired Common Mode Voltage	$+V_{b1}$ and $+V_{b2}$ (V)	$-V_b$ (V)
2 Volts	2	-8
-2 Volts	8	-2

Figures 19 and 20 illustrate how the common mode voltage effects harmonic distortion. Figure 21 shows the resulting  $I_s$  and  $-I_s$  supply currents.

Pay close attention to your peak-to-peak output voltage requirement. As you change the common mode voltage, you may need to increase or shift  $\pm V_s$  in order to achieve your output requirements. A 2V margin is recommended. For example, if your output requirement is  $5V_{pp}$  and you will be

changing the common mode from 1V to 3V set  $V_s = +7.5$  and  $-V_s = -3.5V$ . This example calls for a supply voltage of greater than 10V. This will not effect supply current because as Figure 11 indicates, changing  $\pm V_s$  has no effect on supply current.

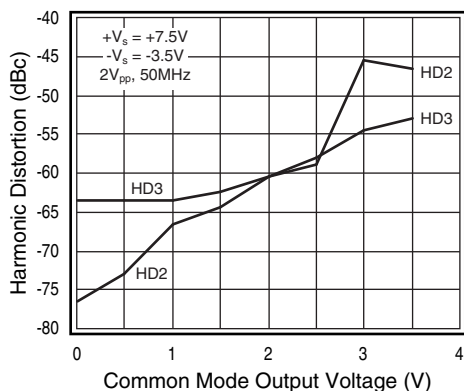


Figure 19: 2Vpp HD vs. Common Mode Voltage

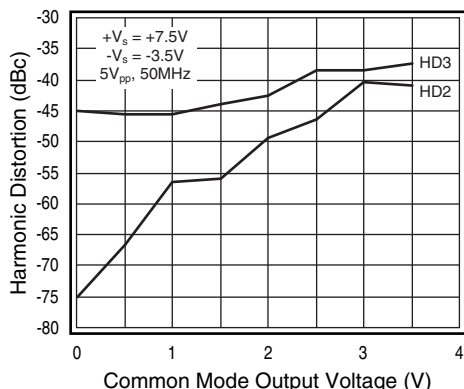


Figure 20: 5Vpp HD vs. Common Mode Voltage

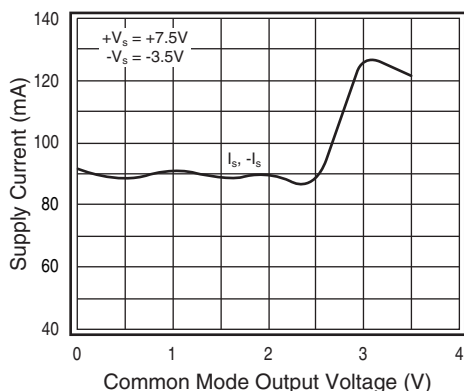


Figure 21: Resulting  $I_s$  and  $-I_s$

## Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Cadeka has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include all recommended 6.8 $\mu$ F and 0.01 $\mu$ F bypass capacitors
- Place the 6.8 $\mu$ F capacitors within 0.75 inches of the power pin
- Place the 0.01 $\mu$ F capacitors within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances
- A 10pF to 50pF bypass capacitor can be used between pins 5 and 6 and between pins 10 and 11 to reduce crosstalk from the positive supply

Refer to the evaluation board layouts shown in Figure 22 for more information.

## Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

Evaluation Board	Description	Products
KEB007	Basic KH600 Eval Bd	KH600
KEB009	KH600 Eval Bd with offset and $I_{cc}$ Adjust Option	KH600

Do not include capacitors C2, C3, C7, C11, and C12 that are shown on the KEB007 evaluation board. Evaluation board schematics and layouts are shown in Figure 22. Refer to the schematic shown in Figure 1 for the KEB007 board and Figure 3 for the KEB009 board.

# KH600 Evaluation Board Layout

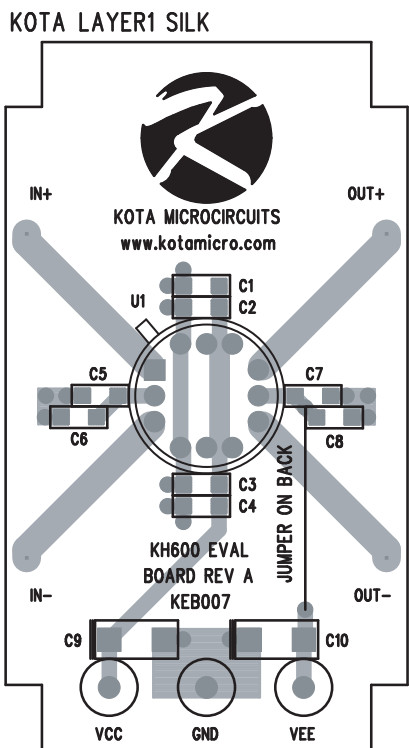


Figure 22a: KEB007 (top side)

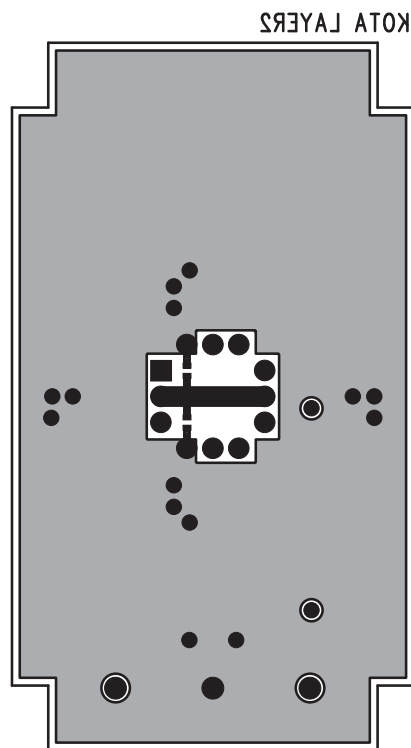


Figure 22b: KEB007 (bottom side)

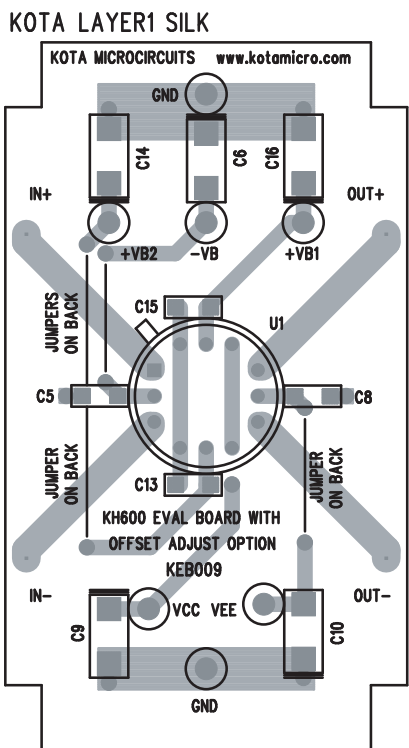


Figure 22c: KEB009 (top side)

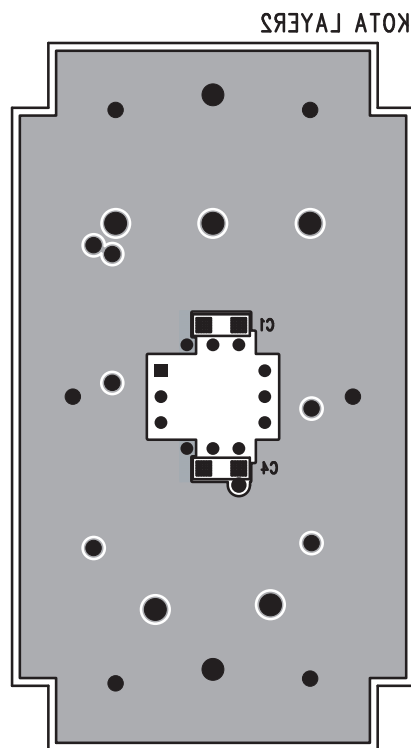


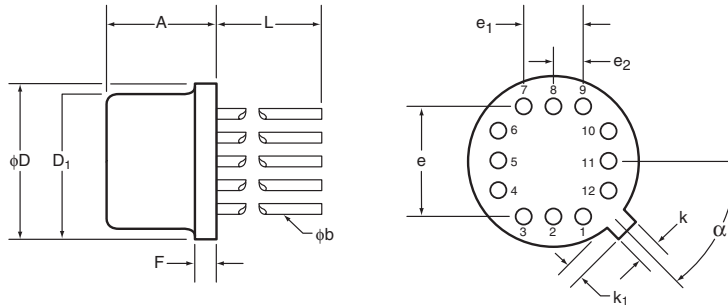
Figure 22d: KEB009 (bottom side)

## Ordering Information

Model	Part Number	Package	Evaluation Board
KH600	KH600AI	12-pin TO8	KEB007, KEB009

Temperature range: -40°C to +85°C.

## KH600 Package Dimensions



TO-8				
SYMBOL	INCHES		MILIMETERS	
	Minimum	Maximum	Minimum	Maximum
A	0.142	0.181	3.61	4.60
$\phi b$	0.016	0.019	0.41	0.48
$\phi D$	0.595	0.605	15.11	15.37
$\phi D_1$	0.543	0.555	13.79	14.10
e	0.400 BSC		10.16 BSC	
e <sub>1</sub>	0.200 BSC		5.08 BSC	
e <sub>2</sub>	0.100 BSC		2.54 BSC	
F	0.016	0.030	0.41	0.76
k	0.026	0.036	0.66	0.91
k <sub>1</sub>	0.026	0.036	0.66	0.91
L	0.310	0.340	7.87	8.64
$\alpha$	45° BSC		45° BSC	

### NOTES:

Seal: cap weld  
 Lead finish: gold per MIL-M-38510  
 Package composition:  
 Package: metal  
 Lid: Type A per MIL-M-38510

### Life Support Policy

Cadeca's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Cadeca Microcircuits, Inc. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Cadeca does not assume any responsibility for use of any circuitry described, and Cadeca reserves the right at any time without notice to change said circuitry and specifications.