

# COMLINEAR<sup>®</sup> CLC1605, CLC3605

## Single and Triple, 1.5GHz Amplifiers

### FEATURES

- 0.1dB gain flatness to 120MHz
- 0.01%/0.01° differential gain/phase
- 1.2GHz -3dB bandwidth at G = 2
- 700MHz large signal bandwidth
- 2,500V/μs slew rate
- 3.7nV/√Hz input voltage noise
- 120mA output current
- Triple offers disable
- Fully specified at 5V and ±5V supplies
- CLC1605: Pb-free SOT23-5
- CLC3605: Pb-free SOIC-16

### APPLICATIONS

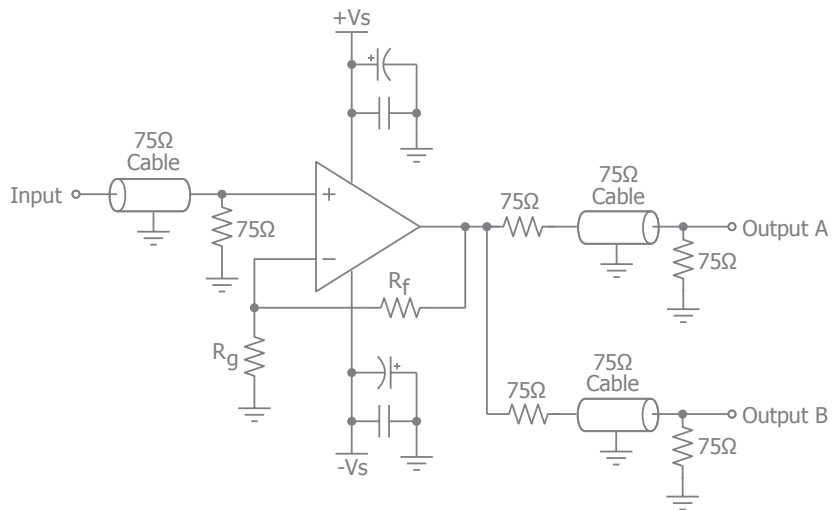
- RGB video line drivers
- High definition video driver
- Video switchers and routers
- ADC buffer
- Active filters
- High-speed instrumentation
- Wide dynamic range IF amp
- Radar/communication receivers

### General Description

The COMLINEAR CLC1605 (single) and CLC3605 (triple) are high-performance, current feedback amplifiers that provide 1.5GHz unity gain bandwidth, ±0.1dB gain flatness to 120MHz, and 2,500V/μs slew rate. This high performance exceeds the requirements of high-definition television (HDTV) and other multimedia applications. These COMLINEAR high-performance amplifiers also provide ample output current to drive multiple video loads.

The COMLINEAR CLC1605 and CLC3605 are designed to operate from ±5V or +5V supplies. The CLC3605 offers a fast enable/disable feature to save power. While disabled, the outputs are in a high-impedance state to allow for multiplexing applications. The combination of high-speed, low-power, and excellent video performance make these amplifiers well suited for use in many general purpose, high-speed applications including high-definition video, imaging applications, and radar/communications receivers.

### Typical Application - Driving Dual Video Loads



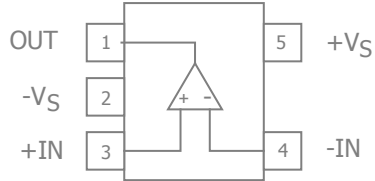
### Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1605IST5X	SOT23-5	Yes	Yes	-40°C to +85°C	Reel
CLC3605ISO16X	SOIC-16	Yes	Yes	-40°C to +85°C	Reel
CLC3605ISO16	SOIC-16	Yes	Yes	-40°C to +85°C	Rail

Moisture sensitivity level for all parts is MSL-1.



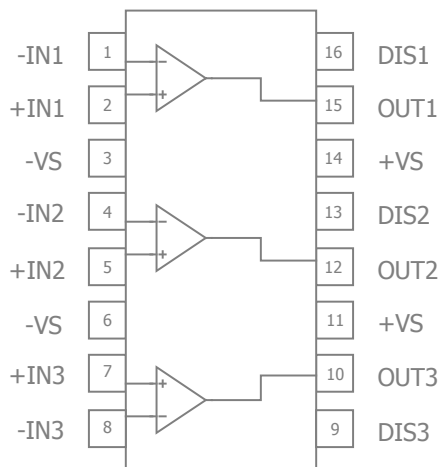
## CLC1605 Pin Configuration



## CLC1605 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	-VS	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	+VS	Positive supply

## CLC3605 Pin Configuration



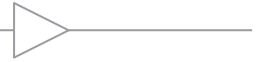
## CLC3605 Pin Configuration

Pin No.	Pin Name	Description
1	-IN1	Negative input, channel 1
2	+IN1	Positive input, channel 1
3	-VS	Negative supply
4	-IN2	Negative input, channel 2
5	+IN2	Positive input, channel 2
6	-VS	Negative supply
7	+IN3	Positive input, channel 3
8	-IN3	Negative input, channel 3
9	DIS3	Disable pin. Enabled if pin is grounded, left floating or pulled below $V_{ON}$ , disabled if pin is pulled above $V_{OFF}$ .
10	OUT3	Output, channel 3
11	+VS	Positive supply
12	OUT2	Output, channel 2
13	DIS2	Disable pin. Enabled if pin is grounded, left floating or pulled below $V_{ON}$ , disabled if pin is pulled above $V_{OFF}$ .
14	+VS	Positive supply
15	OUT1	Output, channel 1
16	DIS1	Disable pin. Enabled if pin is grounded, left floating or pulled below $V_{ON}$ , disabled if pin is pulled above $V_{OFF}$ .

## Disable Pin Truth Table

Pin	High	Low*
DIS	Disabled	Enabled

\*Default Open State



## Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	14	V
Input Voltage Range	$-V_S - 0.5V$	$+V_S + 0.5V$	V
Continuous Output Current		120	mA

## Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
16-Lead SOIC		68		°C/W

Notes:

Package thermal resistance ( $\theta_{JA}$ ), JEDEC standard, multi-layer test boards, still air.

## ESD Protection

Product	SOT23-5	SOIC-16
Human Body Model (HBM) <sup>(1)</sup>	2kV	2kV
Charged Device Model (CDM)	1kV	1kV

Notes:

1. 0.8kV between the input pairs +IN and -IN pins only. All other pins are 2kV.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	4.5		12	V



## Electrical Characteristics at +5V

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	Unity Gain Bandwidth	$G = +1$ , $V_{OUT} = 0.5V_{pp}$ , $R_f = 499\Omega$		1250		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.5V_{pp}$		1000		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 1V_{pp}$		825		MHz
BW <sub>0.1dBSS</sub>	0.1dB Gain Flatness	$G = +2$ , $V_{OUT} = 0.5V_{pp}$		100		MHz
BW <sub>0.1dBLS</sub>	0.1dB Gain Flatness	$G = +2$ , $V_{OUT} = 1V_{pp}$		100		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time	$V_{OUT} = 1\text{V}$ step; (10% to 90%)		0.6		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 1\text{V}$ step		10		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		1		%
SR	Slew Rate	2V step		1350		V/ $\mu\text{s}$
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 5MHz		-75		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 5MHz		-85		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 5MHz		74		dB
D <sub>G</sub>	Differential Gain	NTSC (3.58MHz), AC-coupled, $R_L = 150\Omega$		0.04		%
D <sub>P</sub>	Differential Phase	NTSC (3.58MHz), AC-coupled, $R_L = 150\Omega$		0.01		°
IP3	Third Order Intercept	$V_{OUT} = 1V_{pp}$ , 10MHz		37		dBm
SFDR	Spurious Free Dynamic Range	$V_{OUT} = 1V_{pp}$ , 5MHz		61		dBc
$e_n$	Input Voltage Noise	> 1MHz		3.7		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Current Noise	> 1MHz, Inverting		20		pA/ $\sqrt{\text{Hz}}$
		> 1MHz, Non-Inverting		30		pA/ $\sqrt{\text{Hz}}$
X <sub>TALK</sub>	Crosstalk	Channel-to-channel 5MHz, $V_{OUT} = 2V_{pp}$		60		dB
DC Performance						
V <sub>IO</sub>	Input Offset Voltage			0		mV
dV <sub>IO</sub>	Average Drift			1.6		$\mu\text{V}/^\circ\text{C}$
I <sub>bn</sub>	Input Bias Current - Non-Inverting			3		$\mu\text{A}$
dI <sub>bn</sub>	Average Drift			7		nA/ $^\circ\text{C}$
I <sub>bi</sub>	Input Bias Current - Inverting			6		$\mu\text{A}$
dI <sub>bi</sub>	Average Drift			20		nA/ $^\circ\text{C}$
PSRR	Power Supply Rejection Ratio	DC		58		dB
I <sub>S</sub>	Supply Current	per channel		11		mA
Disable Characteristics - CLC3605 only						
T <sub>ON</sub>	Turn On Time			23		ns
T <sub>OFF</sub>	Turn Off Time			350		ns
OFF <sub>IOS</sub>	Off Isolation	5MHz, $V_{OUT} = 2V_{pp}$		75		dB
V <sub>OFF</sub>	Power Down Input Voltage	DIS pin, disabled if pin is pulled above V <sub>OFF</sub>	Disabled if DIS > 1.5V			V
V <sub>ON</sub>	Enable Input Voltage	DIS pin, enabled if pin is grounded, left open or pulled below V <sub>ON</sub>	Enabled if DIS < 0.5V			V
I <sub>SD</sub>	Disable Supply Current	DIS pin is pulled to V <sub>S</sub>		0.09		mA
Input Characteristics						
R <sub>IN</sub>	Input Resistance	Non-inverting		150		k $\Omega$
		Inverting		70		$\Omega$
C <sub>IN</sub>	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			1.5 to 3.5		V
CMRR	Common Mode Rejection Ratio	DC		50		dB



## Electrical Characteristics at +5V continued

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to  $V_S/2$ ,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
$R_O$	Output Resistance	Closed Loop, DC		0.1		$\Omega$
$V_{OUT}$	Output Voltage Swing	$R_L = 150\Omega$		1.5 to 3.5		V
$I_{OUT}$	Output Current			$\pm 120$		mA

### Notes:

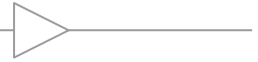
1. 100% tested at  $25^\circ\text{C}$



## Electrical Characteristics at $\pm 5V$

$T_A = 25^\circ C$ ,  $V_S = \pm 5V$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
UGBW	Unity Gain Bandwidth	$G = +1$ , $V_{OUT} = 0.5V_{pp}$ , $R_f = 499\Omega$		1500		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.5V_{pp}$		1200		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		700		MHz
BW <sub>0.1dBSS</sub>	0.1dB Gain Flatness	$G = +2$ , $V_{OUT} = 0.5V_{pp}$		120		MHz
BW <sub>0.1dBLS</sub>	0.1dB Gain Flatness	$G = +2$ , $V_{OUT} = 2V_{pp}$		120		MHz
Time Domain Response						
$t_R$ , $t_F$	Rise and Fall Time	$V_{OUT} = 2V$ step; (10% to 90%)		0.65		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 2V$ step		13		ns
OS	Overshoot	$V_{OUT} = 0.2V$ step		1		%
SR	Slew Rate	2V step		2500		V/ $\mu$ s
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		-73		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		-85		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		72		dB
D <sub>G</sub>	Differential Gain	NTSC (3.58MHz), AC-coupled, $R_L = 150\Omega$		0.01		%
D <sub>P</sub>	Differential Phase	NTSC (3.58MHz), AC-coupled, $R_L = 150\Omega$		0.01		°
IP3	Third Order Intercept	$V_{OUT} = 2V_{pp}$ , 10MHz		42		dBm
SFDR	Spurious Free Dynamic Range	$V_{OUT} = 1V_{pp}$ , 5MHz		73		dBc
$e_n$	Input Voltage Noise	> 1MHz		3.7		nV/ $\sqrt{Hz}$
$i_n$	Input Current Noise	> 1MHz, Inverting		20		pA/ $\sqrt{Hz}$
		> 1MHz, Non-Inverting		30		pA/ $\sqrt{Hz}$
X <sub>TALK</sub>	Crosstalk	Channel-to-channel 5MHz		60		dB
DC Performance						
V <sub>IO</sub>	Input Offset Voltage <sup>(1)</sup>		-10	0	10	mV
dV <sub>IO</sub>	Average Drift			1.6		$\mu$ V/ $^\circ C$
I <sub>bn</sub>	Input Bias Current - Non-Inverting <sup>(1)</sup>		-40	19	40	$\mu$ A
dI <sub>bn</sub>	Average Drift			7		nA/ $^\circ C$
I <sub>bi</sub>	Input Bias Current - Inverting <sup>(1)</sup>		-35	6	35	$\mu$ A
dI <sub>bi</sub>	Average Drift			20		nA/ $^\circ C$
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	DC	40	60		dB
I <sub>S</sub>	Supply Current <sup>(1)</sup>	per channel		12	18	mA
Disable Characteristics - CLC3605 only						
T <sub>ON</sub>	Turn On Time			35		ns
T <sub>OFF</sub>	Turn Off Time			410		ns
OFF <sub>IOS</sub>	Off Isolation	5MHz, $V_{OUT} = 2V_{pp}$		75		dB
V <sub>OFF</sub>	Power Down Input Voltage	DIS pin, disabled if pin is pulled above V <sub>OFF</sub>	Disabled if DIS > 3V			V
V <sub>ON</sub>	Enable Input Voltage	DIS pin, enabled if pin is grounded, left open or pulled below V <sub>ON</sub>	Enabled if DIS < 1V			V
I <sub>SD</sub>	Disable Supply Current <sup>(1)</sup>	per channel, DIS pin is pulled to V <sub>S</sub>		0.1	0.3	mA
Input Characteristics						
R <sub>IN</sub>	Input Resistance	Non-inverting		150		k $\Omega$
		Inverting		70		$\Omega$
C <sub>IN</sub>	Input Capacitance			1.0		pF
CMIR	Common Mode Input Range			$\pm 4.0$		V
CMRR	Common Mode Rejection Ratio <sup>(1)</sup>	DC	40	55		dB



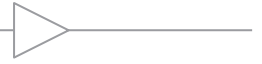
## Electrical Characteristics at $\pm 5V$ continued

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5V$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
$R_O$	Output Resistance	Closed Loop, DC		0.1		$\Omega$
$V_{OUT}$	Output Voltage Swing	$R_L = 150\Omega$ <sup>(1)</sup>	$\pm 3.0$	$\pm 3.8$		V
$I_{OUT}$	Output Current			$\pm 280$		mA

### Notes:

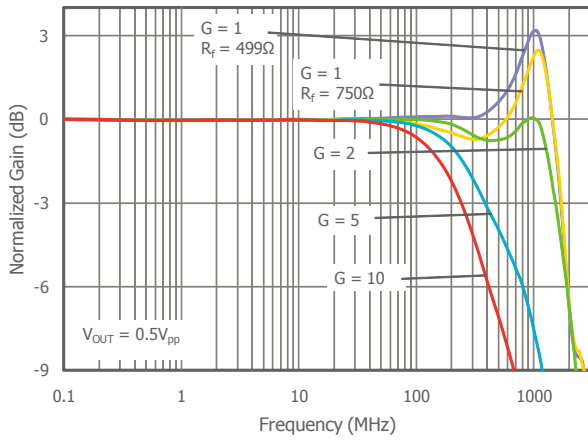
1. 100% tested at  $25^\circ\text{C}$



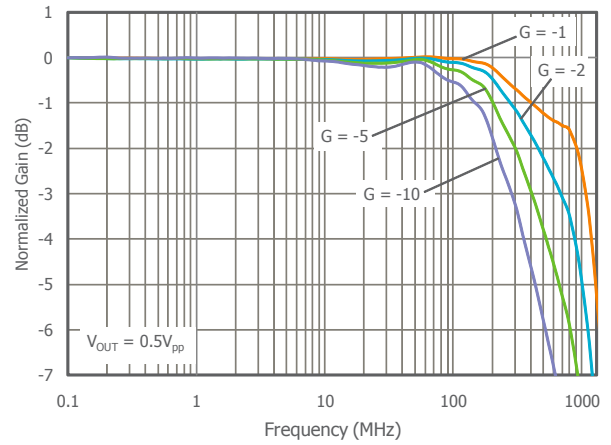
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

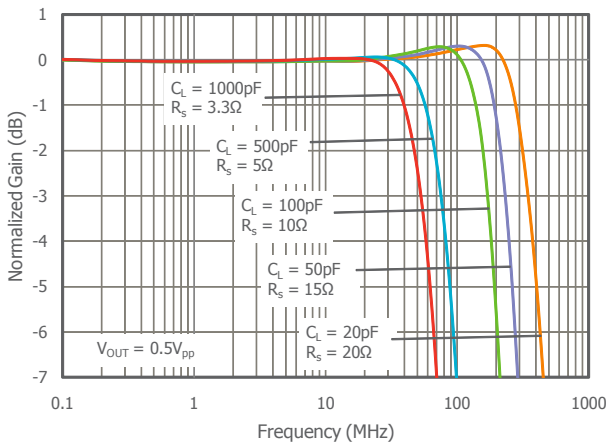
Non-Inverting Frequency Response



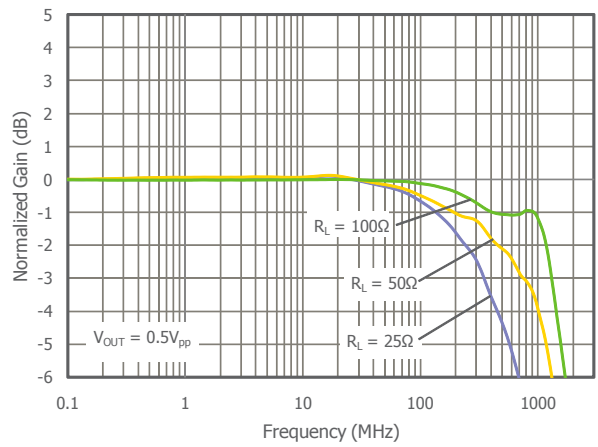
Inverting Frequency Response



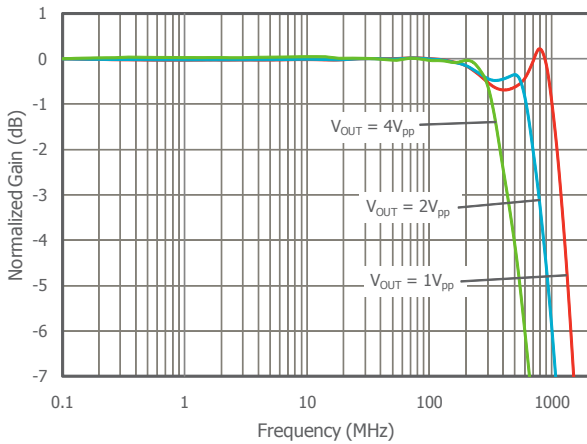
Frequency Response vs.  $C_L$



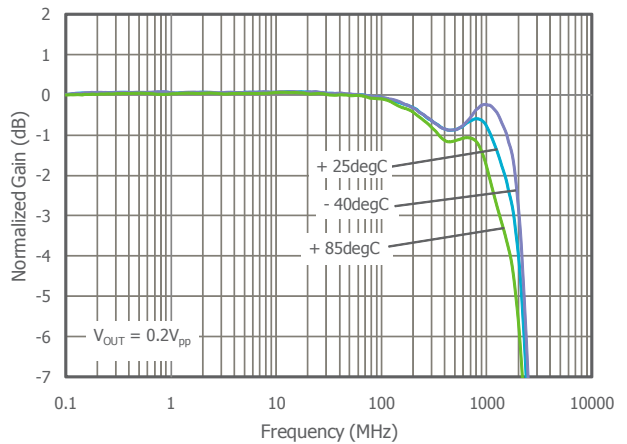
Frequency Response vs.  $R_L$

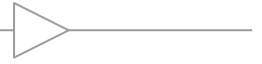


Frequency Response vs.  $V_{OUT}$



Frequency Response vs. Temperature

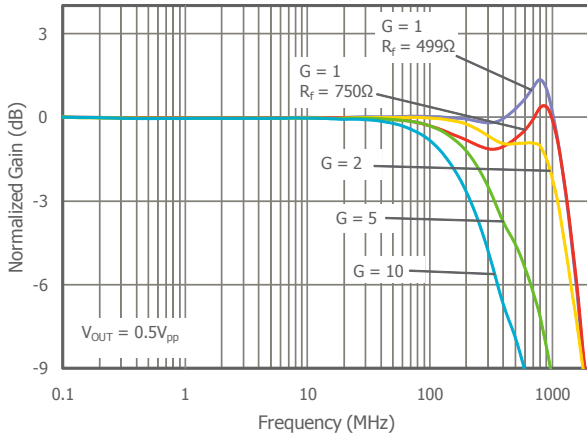




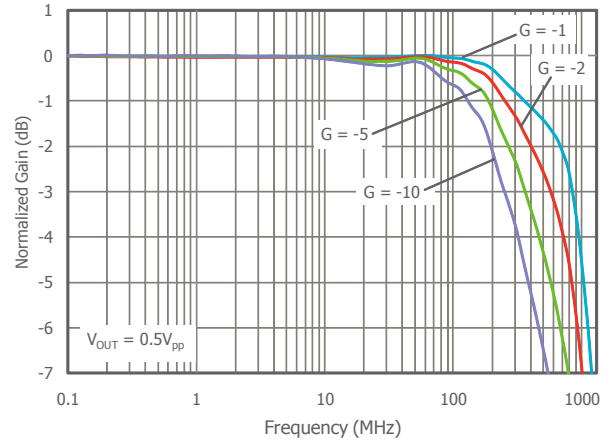
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

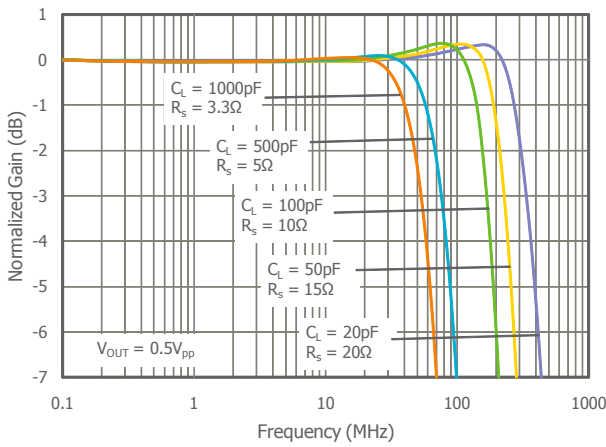
Non-Inverting Frequency Response at  $V_S = 5\text{V}$



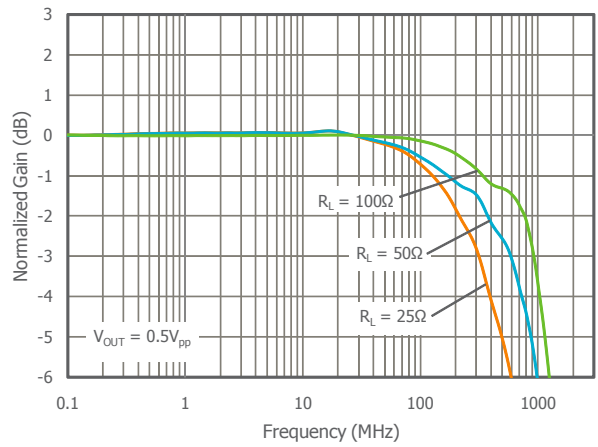
Inverting Frequency Response at  $V_S = 5\text{V}$



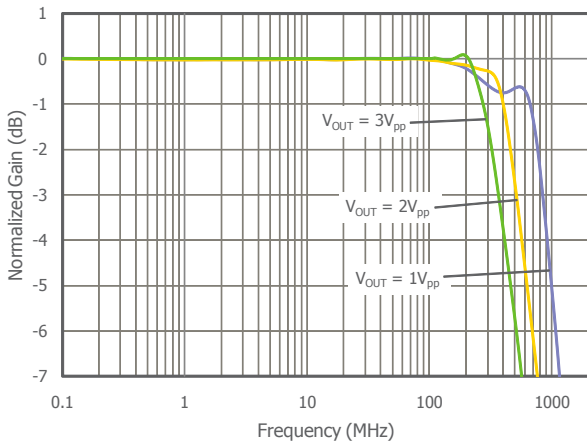
Frequency Response vs.  $C_L$  at  $V_S = 5\text{V}$



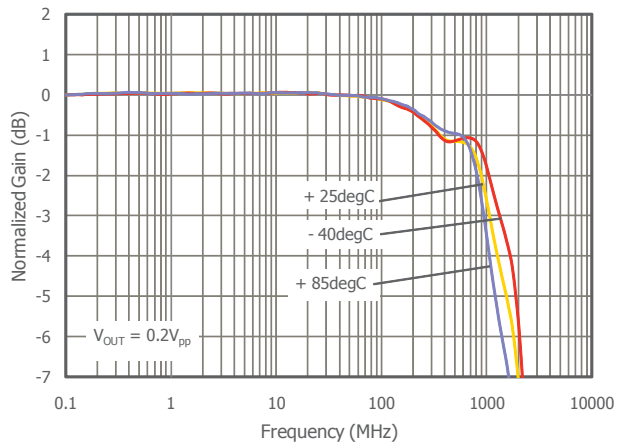
Frequency Response vs.  $R_L$  at  $V_S = 5\text{V}$



Frequency Response vs.  $V_{OUT}$  at  $V_S = 5\text{V}$



Frequency Response vs. Temperature at  $V_S = 5\text{V}$

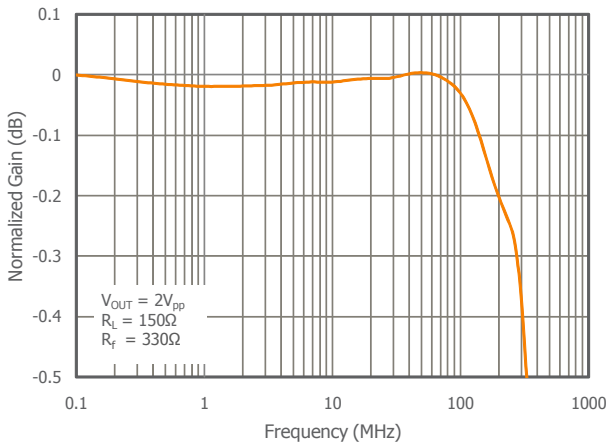




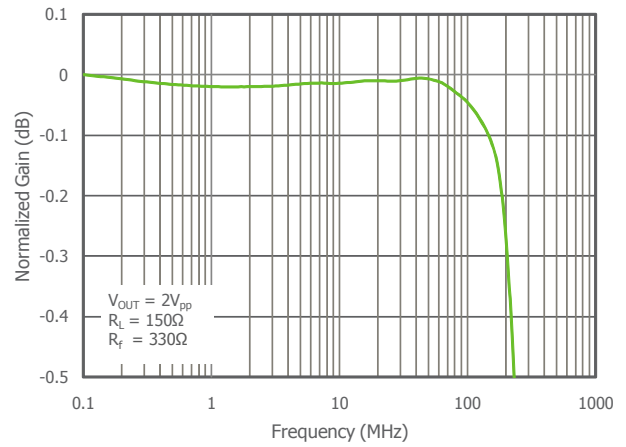
## Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

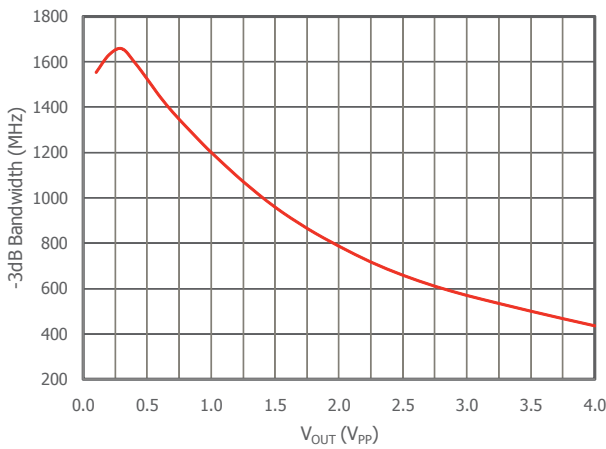
Gain Flatness



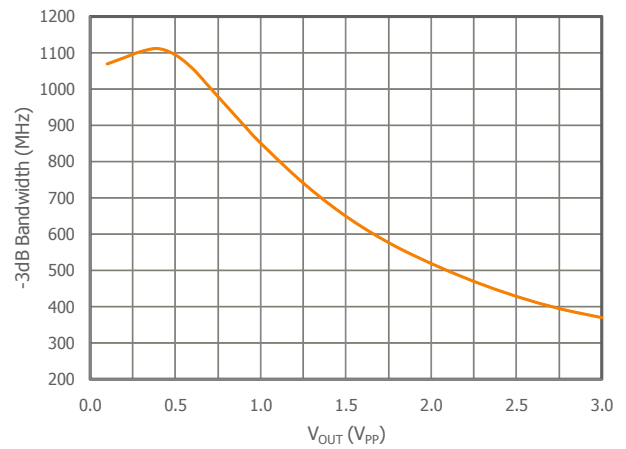
Gain Flatness at  $V_S = 5\text{V}$



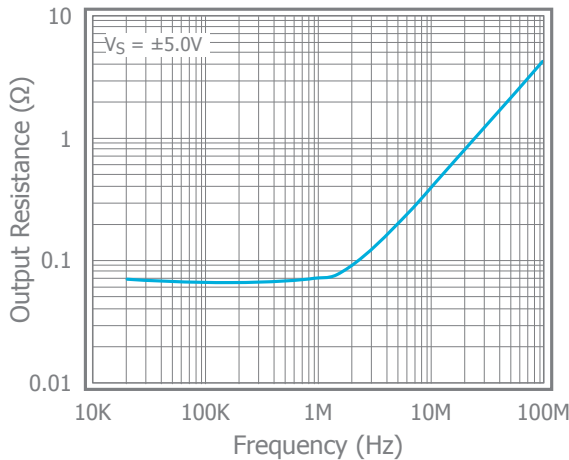
-3dB Bandwidth vs.  $V_{OUT}$



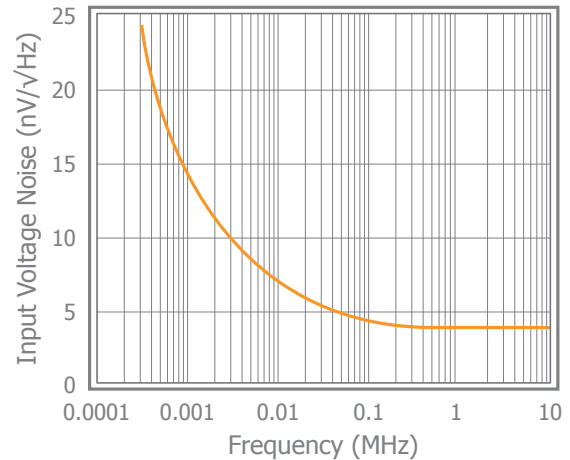
-3dB Bandwidth vs.  $V_{OUT}$  at  $V_S = 5\text{V}$



Closed Loop Output Impedance vs. Frequency



Input Voltage Noise

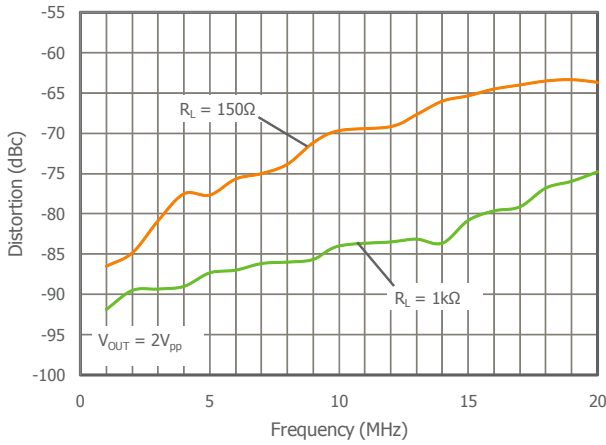




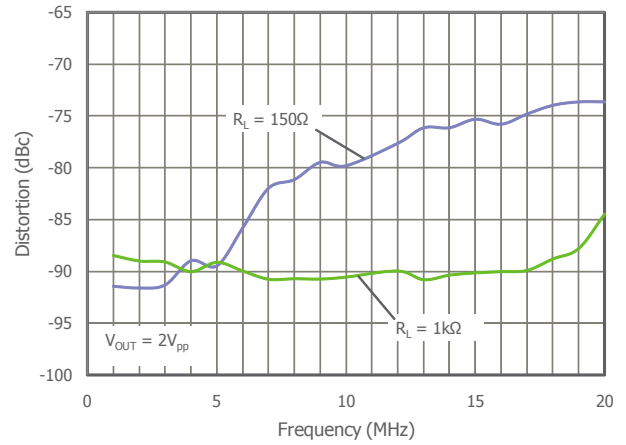
## Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

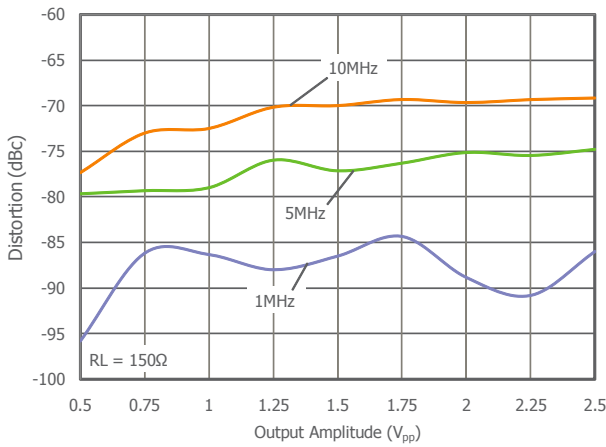
2nd Harmonic Distortion vs.  $R_L$



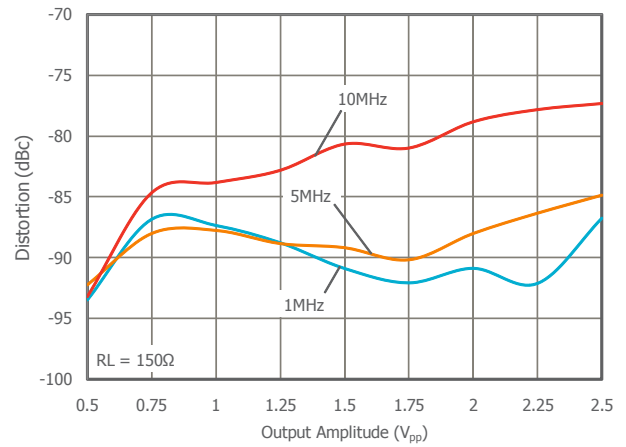
3rd Harmonic Distortion vs.  $R_L$



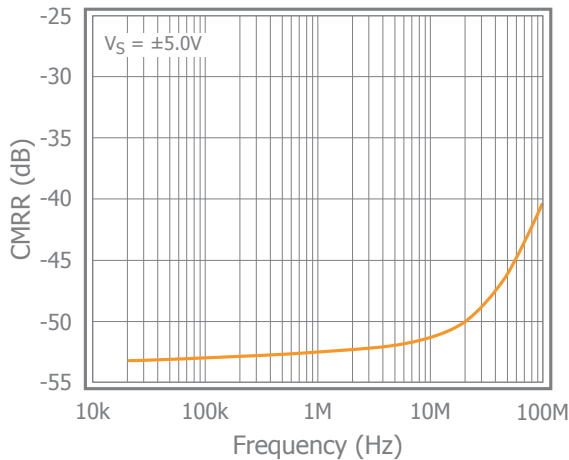
2nd Harmonic Distortion vs.  $V_{OUT}$



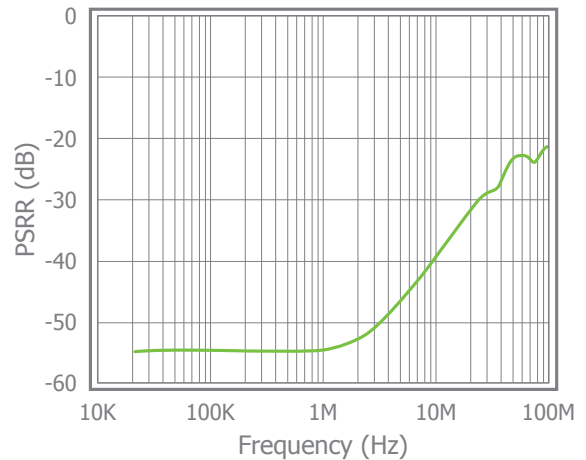
3rd Harmonic Distortion vs.  $V_{OUT}$

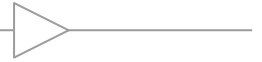


CMRR vs. Frequency



PSRR vs. Frequency

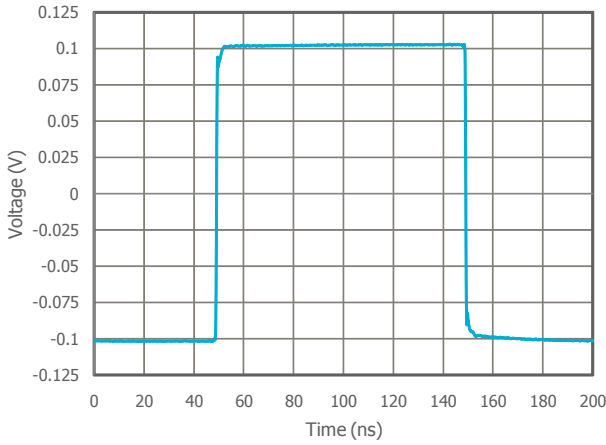




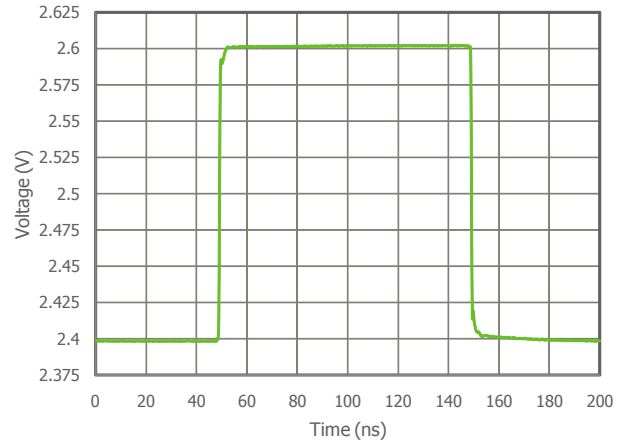
### Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

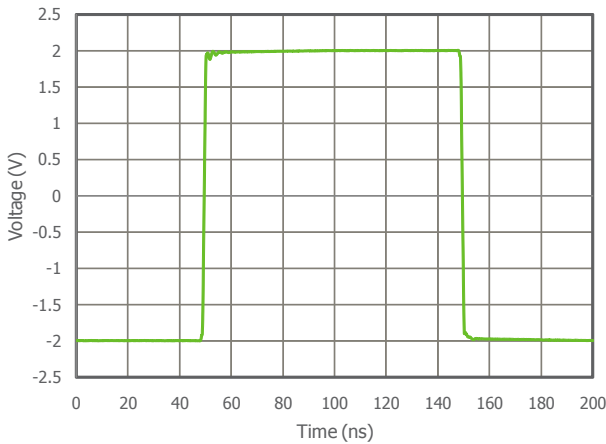
Small Signal Pulse Response



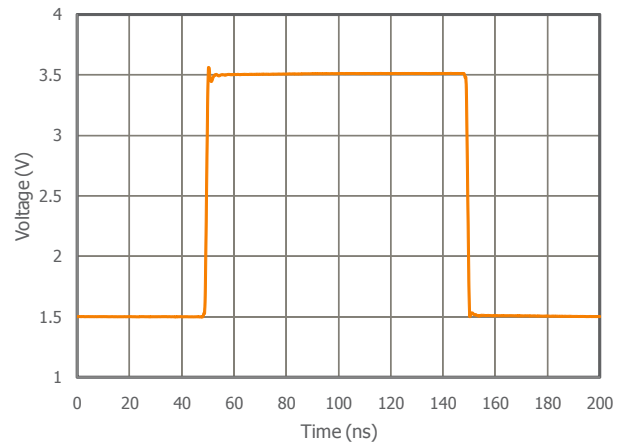
Small Signal Pulse Response at  $V_S = 5\text{V}$



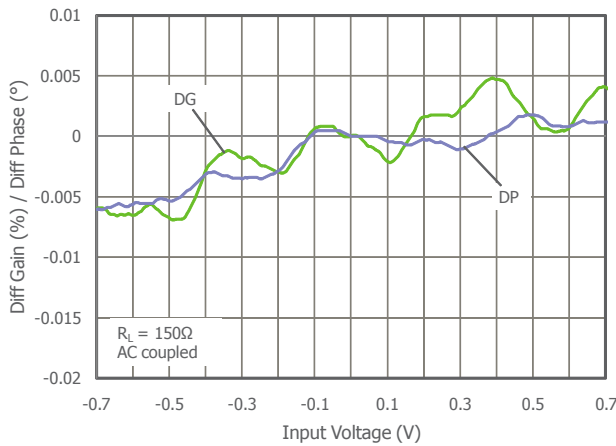
Large Signal Pulse Response



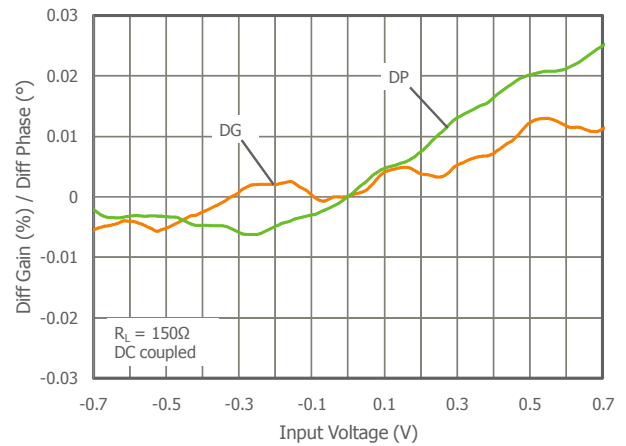
Large Signal Pulse Response at  $V_S = 5\text{V}$

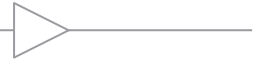


Differential Gain & Phase AC Coupled Output



Differential Gain & Phase DC Coupled Output

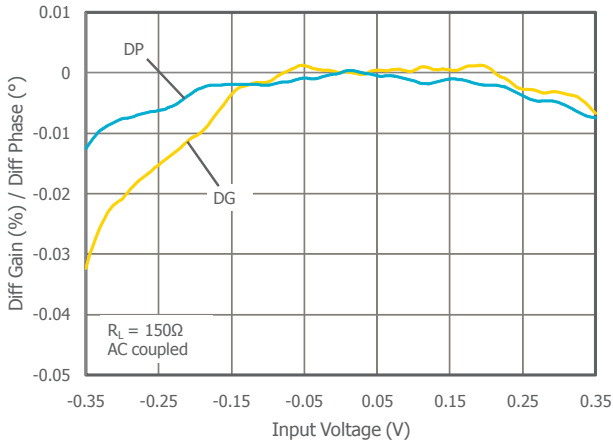




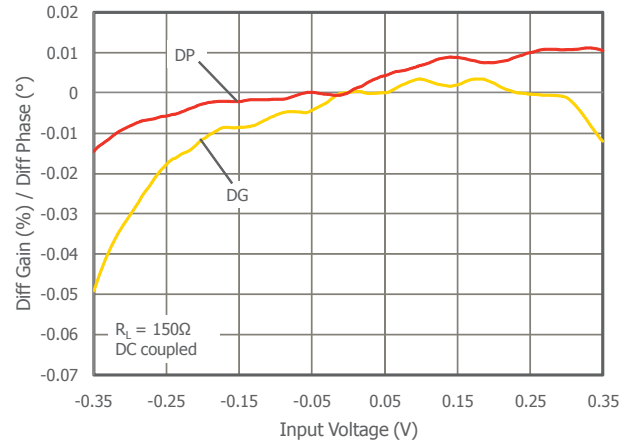
## Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5\text{V}$ ,  $R_f = R_g = 330\Omega$ ,  $R_L = 150\Omega$  to GND,  $G = 2$ ; unless otherwise noted.

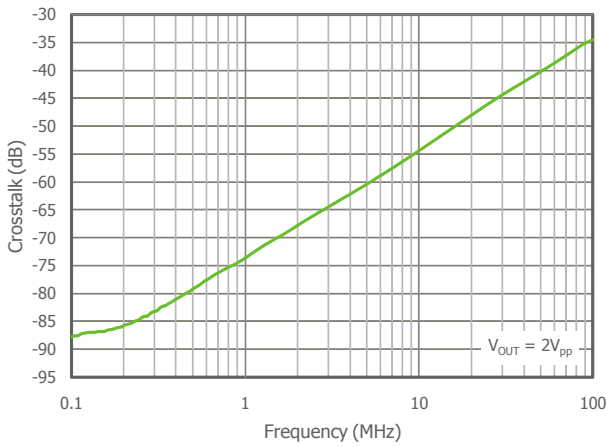
Differential Gain & Phase AC Coupled Output at  $V_S = \pm 2.5\text{V}$



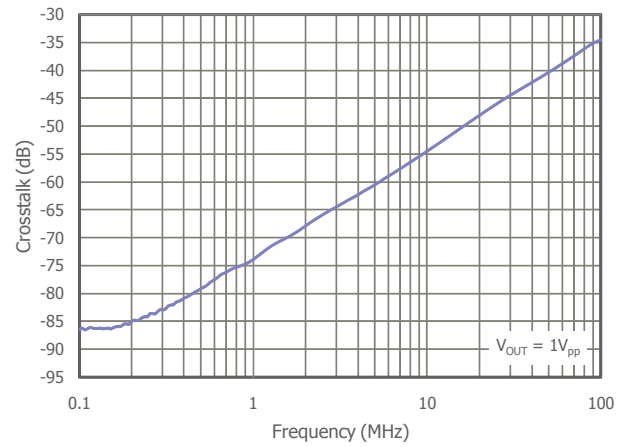
Differential Gain & Phase DC Coupled Output at  $V_S = \pm 2.5\text{V}$



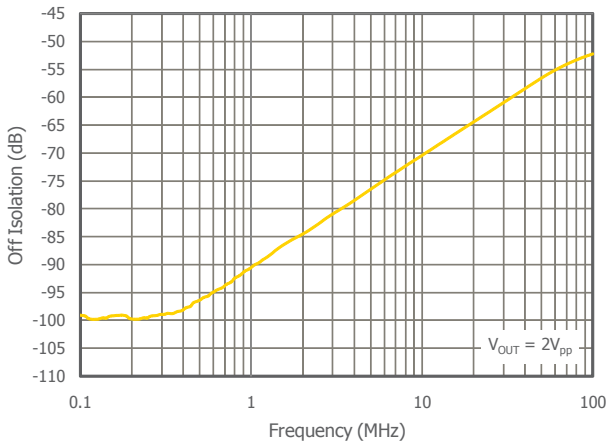
Crosstalk vs. Frequency (CLC3605)



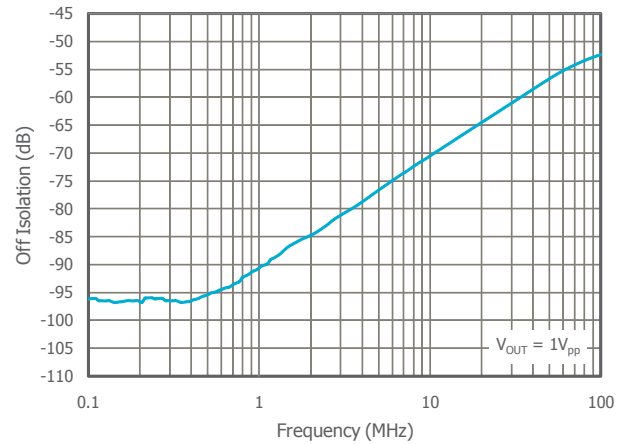
Crosstalk vs. Frequency at  $V_S=5\text{V}$  (CLC3605)



Off Isolation vs. Frequency



Off Isolation vs. Frequency at  $V_S=5\text{V}$





## General Information - Current Feedback Technology

### Advantages of CFB Technology

The CLC1605 Family of amplifiers utilize current feedback (CFB) technology to achieve superior performance. The primary advantage of CFB technology is higher slew rate performance when compared to voltage feedback (VFB) architecture. High slew rate contributes directly to better large signal pulse response, full power bandwidth, and distortion.

CFB also alleviates the traditional trade-off between closed loop gain and usable bandwidth that is seen with a VFB amplifier. With CFB, the bandwidth is primarily determined by the value of the feedback resistor,  $R_f$ . By using optimum feedback resistor values, the bandwidth of a CFB amplifier remains nearly constant with different gain configurations.

When designing with CFB amplifiers always abide by these basic rules:

- Use the recommended feedback resistor value
- Do not use reactive (capacitors, diodes, inductors, etc.) elements in the direct feedback path
- Avoid stray or parasitic capacitance across feedback resistors
- Follow general high-speed amplifier layout guidelines
- Ensure proper precautions have been made for driving capacitive loads

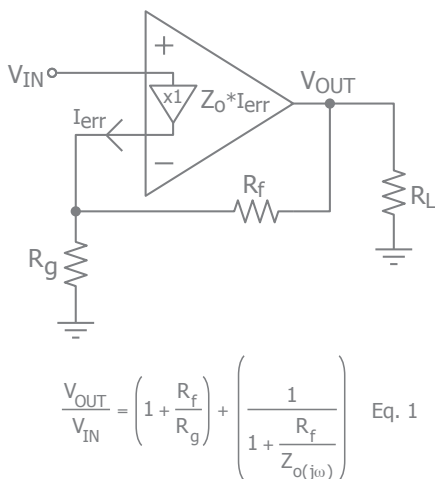


Figure 1. Non-Inverting Gain Configuration with First Order Transfer Function

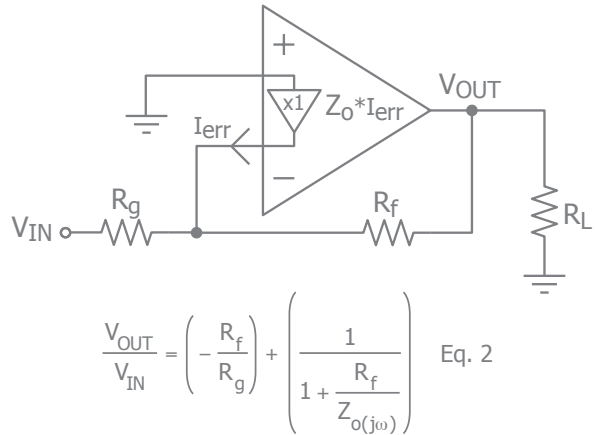


Figure 2. Inverting Gain Configuration with First Order Transfer Function

### CFB Technology - Theory of Operation

Figure 1 shows a simple representation of a current feedback amplifier that is configured in the traditional non-inverting gain configuration.

Instead of having two high-impedance inputs similar to a VFB amplifier, the inputs of a CFB amplifier are connected across a unity gain buffer. This buffer has a high impedance input and a low impedance output. It can source or sink current ( $I_{err}$ ) as needed to force the non-inverting input to track the value of  $V_{in}$ . The CFB architecture employs a high gain trans-impedance stage that senses  $I_{err}$  and drives the output to a value of  $(Z_o(j\omega) * I_{err})$  volts. With the application of negative feedback, the amplifier will drive the output to a voltage in a manner which tries to drive  $I_{err}$  to zero. In practice, primarily due to limitations on the value of  $Z_o(j\omega)$ ,  $I_{err}$  remains a small but finite value.

A closer look at the closed loop transfer function (Eq.1) shows the effect of the trans-impedance,  $Z_o(j\omega)$  on the gain of the circuit. At low frequencies where  $Z_o(j\omega)$  is very large with respect to  $R_f$ , the second term of the equation approaches unity, allowing  $R_f$  and  $R_g$  to set the gain. At higher frequencies, the value of  $Z_o(j\omega)$  will roll off, and the effect of the secondary term will begin to dominate. The -3dB small signal parameter specifies the frequency where the value  $Z_o(j\omega)$  equals the value of  $R_f$  causing the gain to drop by 0.707 of the value at DC.

For more information regarding current feedback amplifiers, visit [www.cadeca.com](http://www.cadeca.com) for detailed application notes, such as AN-3: *The Ins and Outs of Current Feedback Amplifiers*.



## Application Information

### Basic Operation

Figures 3, 4, and 5 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

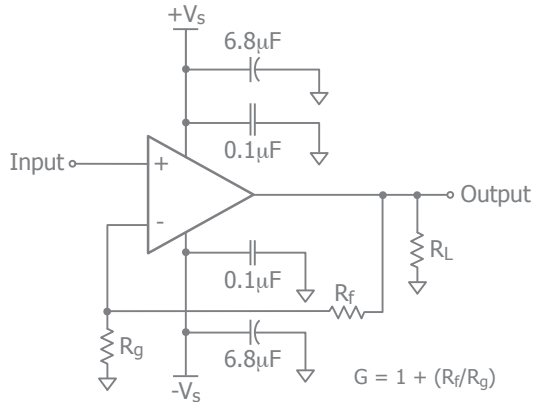


Figure 3. Typical Non-Inverting Gain Circuit

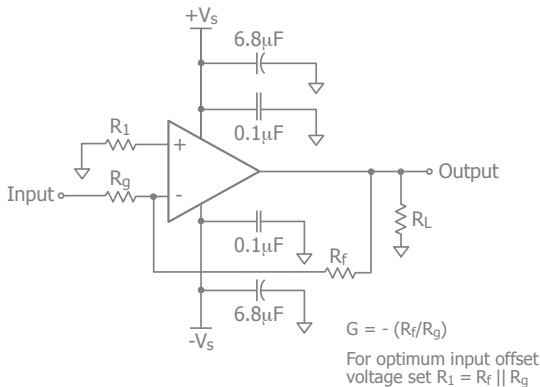


Figure 4. Typical Inverting Gain Circuit

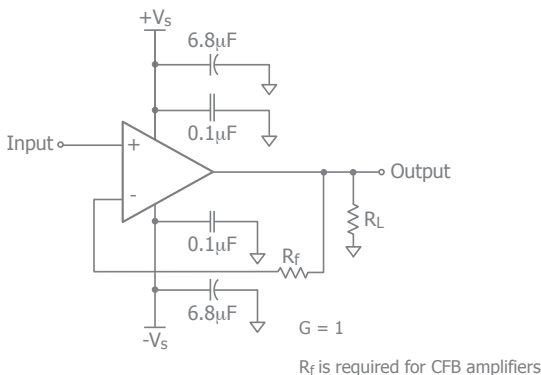


Figure 5. Typical Unity Gain (G=1) Circuit

CFB amplifiers can be used in unity gain configurations. Do not use the traditional voltage follower circuit, where the output is tied directly to the inverting input. With a CFB amplifier, a feedback resistor of appropriate value must be used to prevent unstable behavior. Refer to figure 5 and Table 1. Although this seems cumbersome, it does allow a degree of freedom to adjust the passband characteristics.

### Feedback Resistor Selection

One of the key design considerations when using a CFB amplifier is the selection of the feedback resistor,  $R_f$ .  $R_f$  is used in conjunction with  $R_g$  to set the gain in the traditional non-inverting and inverting circuit configurations. Refer to figures 3 and 4. As discussed in the Current Feedback Technology section, the value of the feedback resistor has a pronounced effect on the frequency response of the circuit.

Table 1, provides recommended  $R_f$  and associated  $R_g$  values for various gain settings. These values produce the optimum frequency response, maximum bandwidth with minimum peaking. Adjust these values to optimize performance for a specific application. The typical performance characteristics section includes plots that illustrate how the bandwidth is directly affected by the value of  $R_f$  at various gain settings.

Gain (V/V)	$R_f$ ( $\Omega$ )	$R_g$ ( $\Omega$ )	$\pm 0.1\text{dB BW}$ (MHz)	$-3\text{dB BW}$ (MHz)
1	499	-	167	1500
2	330	330	120	1200
5	330	82.5	66	385
10	330	33	38	245

Table 1: Recommended  $R_f$  vs. Gain

In general, lowering the value of  $R_f$  from the recommended value will extend the bandwidth at the expense of additional high frequency gain peaking. This will cause increased overshoot and ringing in the pulse response characteristics. Reducing  $R_f$  too much will eventually cause oscillatory behavior.

Increasing the value of  $R_f$  will lower the bandwidth. Lowering the bandwidth creates a flatter frequency response and improves 0.1dB bandwidth performance. This is important in applications such as video. Further increase in  $R_f$  will cause premature gain rolloff and adversely affect gain flatness.



### Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance,  $R_S$ , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

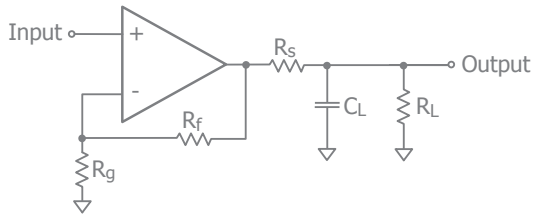


Figure 6. Addition of  $R_S$  for Driving Capacitive Loads

Table 2 provides the recommended  $R_S$  for various capacitive loads. The recommended  $R_S$  values result in  $\leq 0.5\text{dB}$  peaking in the frequency response. The Frequency Response vs.  $C_L$  plot, on page 5, illustrates the response of the CLC1605 Family.

$C_L$ (pF)	$R_S$ ( $\Omega$ )	-3dB BW (MHz)
20	20	350
50	15	235
100	10	170
500	5	75
1000	3.3	52

Table 1: Recommended  $R_S$  vs.  $C_L$

For a given load capacitance, adjust  $R_S$  to optimize the tradeoff between settling time and bandwidth. In general, reducing  $R_S$  will increase bandwidth at the expense of additional overshoot and ringing.

### Parasitic Capacitance on the Inverting Input

Physical connections between components create unintentional or parasitic resistive, capacitive, and inductive elements.

Parasitic capacitance at the inverting input can be especially troublesome with high frequency amplifiers. A parasitic capacitance on this node will be in parallel with the gain setting resistor  $R_f$ . At high frequencies, its impedance can begin to raise the system gain by making  $R_g$  appear smaller.

In general, avoid adding any additional parasitic capacitance at this node. In addition, stray capacitance across the  $R_f$  resistor can induce peaking and high frequency ringing. Refer to the **Layout Considerations** section for additional information regarding high speed layout techniques.

### Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC1605 Family will typically recover in less than 10ns from an overdrive condition. Figure 7 shows the CLC1605 in an overdriven condition.

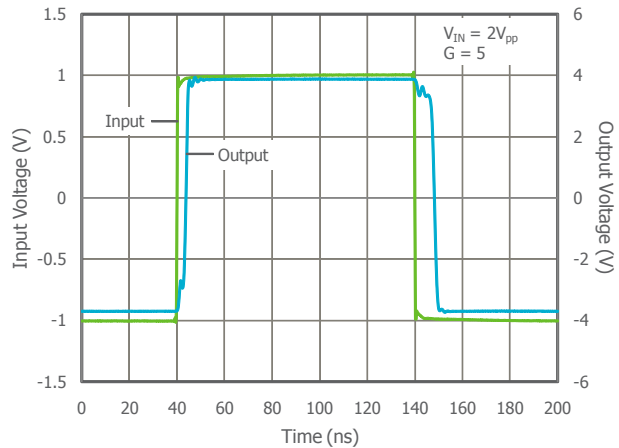


Figure 7. Overdrive Recovery

### Power Dissipation

Power dissipation should not be a factor when operating under the stated 1000 ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond its intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value  $\Theta_{JA}$  ( $\Theta_{JA}$ ) is used along with the total die power dissipation.



$$T_{\text{Junction}} = T_{\text{Ambient}} + (\Theta_{\text{JA}} \times P_{\text{D}})$$

Where  $T_{\text{Ambient}}$  is the temperature of the working environment.

In order to determine  $P_{\text{D}}$ , the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_{\text{D}} = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMS supply}}$$

$$V_{\text{supply}} = V_{\text{S+}} - V_{\text{S-}}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{LOAD}})_{\text{RMS}})^2 / R_{\text{load eff}}$$

The effective load resistor ( $R_{\text{load eff}}$ ) will need to include the effect of the feedback network. For instance,

$R_{\text{load eff}}$  in figure 3 would be calculated as:

$$R_{\text{L}} \parallel (R_{\text{f}} + R_{\text{g}})$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here,  $P_{\text{D}}$  can be found from

$$P_{\text{D}} = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{Load}}$$

Quiescent power can be derived from the specified  $I_{\text{S}}$  values along with known supply voltage,  $V_{\text{Supply}}$ . Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{LOAD}})_{\text{RMS}} = V_{\text{PEAK}} / \sqrt{2}$$

$$(I_{\text{LOAD}})_{\text{RMS}} = (V_{\text{LOAD}})_{\text{RMS}} / R_{\text{load eff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{DYNAMIC}} = (V_{\text{S+}} - V_{\text{LOAD}})_{\text{RMS}} \times (I_{\text{LOAD}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or  $V_{\text{supply}}/2$ .

Figure 8 shows the maximum safe power dissipation in the package vs. the ambient temperature for the available packages.

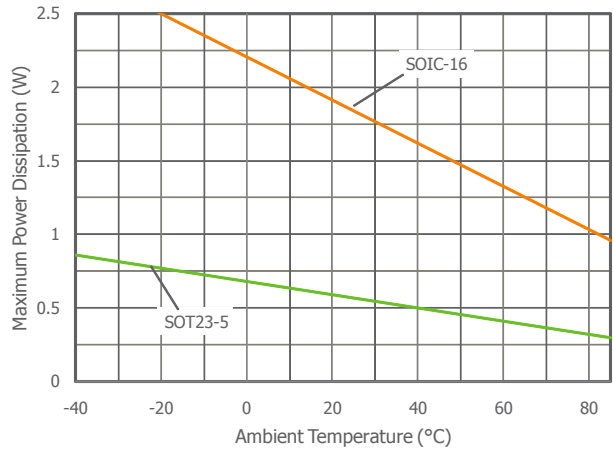


Figure 8. Maximum Power Derating

Better thermal ratings can be achieved by maximizing PC board metallization at the package pins. However, be careful of stray capacitance on the input pins.

In addition, increased airflow across the package can also help to reduce the effective  $\Theta_{\text{JA}}$  of the package.

In the event the outputs are momentarily shorted to a low impedance path, internal circuitry and output metallization are set to limit and handle up to 65mA of output current. However, extended duration under these conditions may not guarantee that the maximum junction temperature (+150°C) is not exceeded.

### Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.



### Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1605
CEB013	CLC3605

### Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-14. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the -Vs pin of the amplifier is not directly connected to the ground plane.

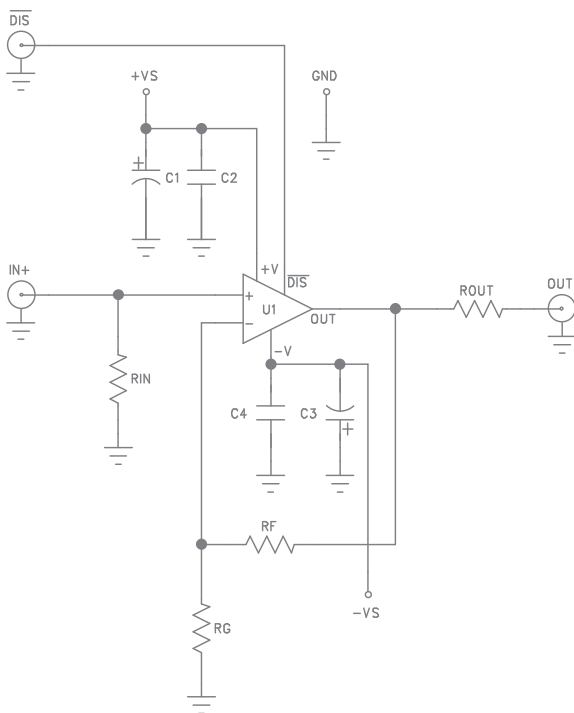


Figure 9. CEB002 Schematic

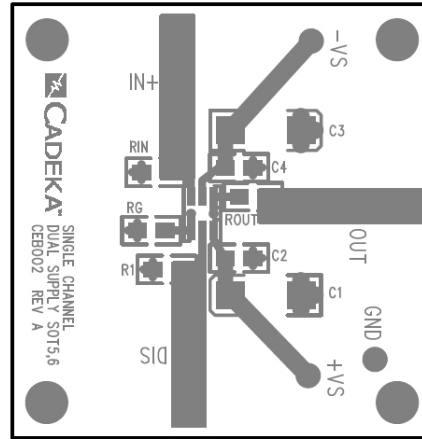


Figure 10. CEB002 Top View

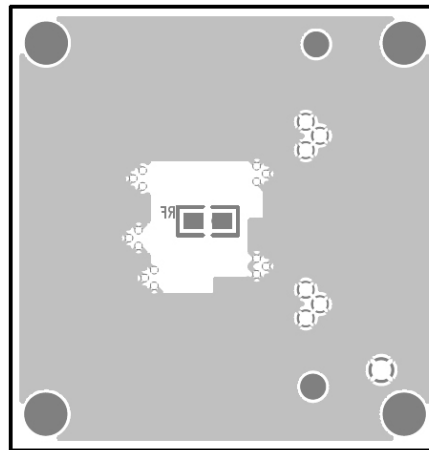


Figure 11. CEB002 Bottom View

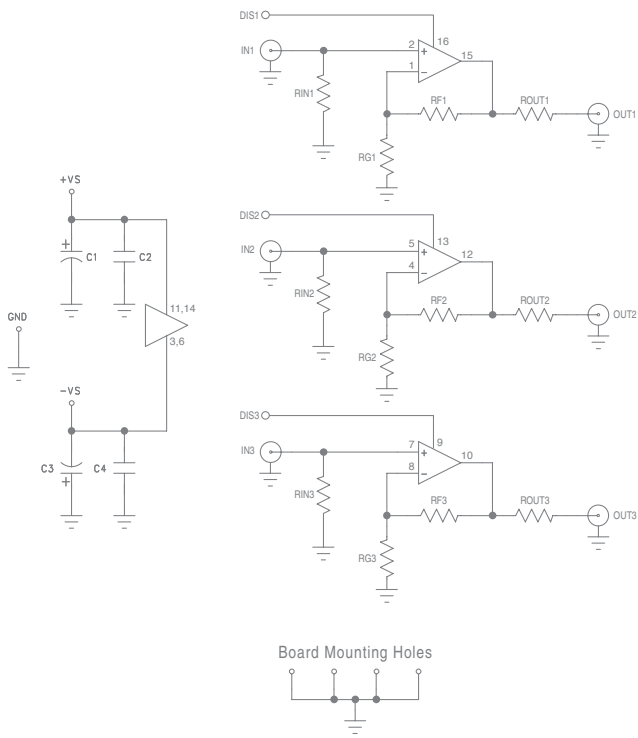
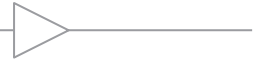


Figure 12. CEB013 Schematic

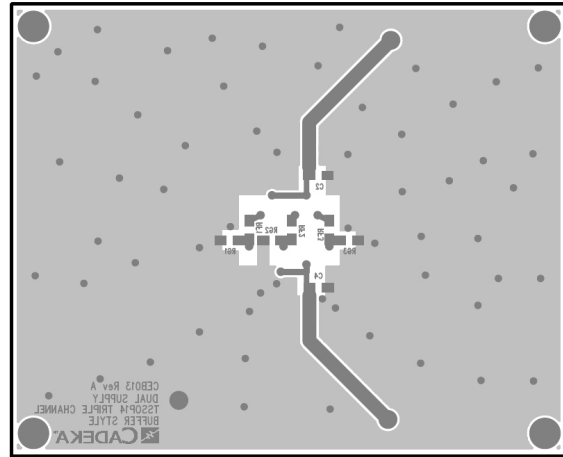


Figure 14. CEB013 Bottom View

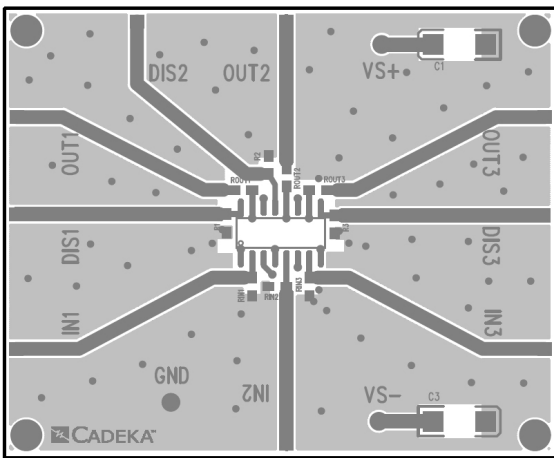
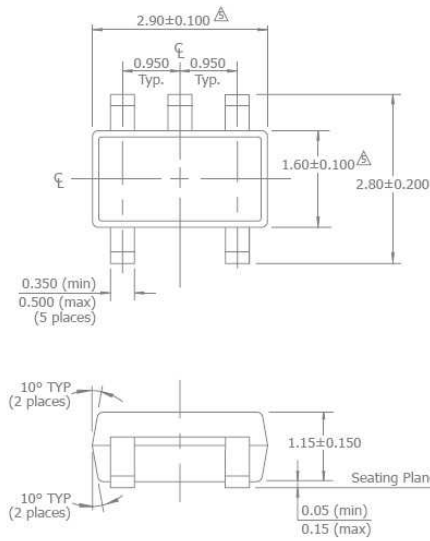


Figure 13. CEB013 Top View



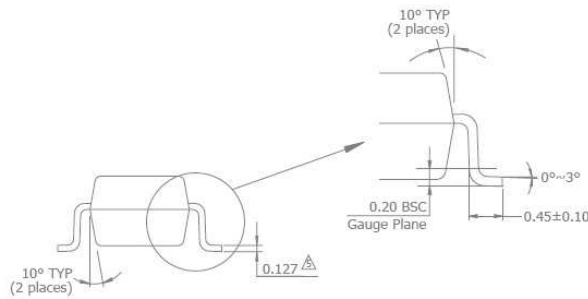
## Mechanical Dimensions

### SOT23-5 Package

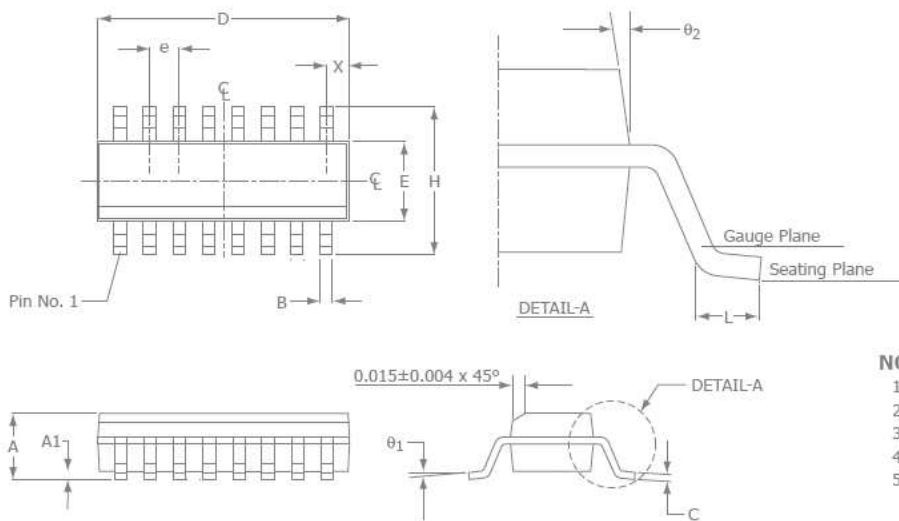


**NOTES:**

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
  2. Package surface to be matte finish VDI 11~13.
  3. Die is facing up for mold. Die is facing down for trim/form, i.e. reverse trim/form.
  4. The footlength measuring is based on the gauge plane method.
- △ Dimension are exclusive of mold flash and gate burr.  
 △ Dimension are exclusive of solder plating.



### SOIC-16 Package



SOIC-16		
SYMBOL	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.014	0.019
D	0.386	0.393
E	0.150	0.157
H	0.229	0.244
e	0.050 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.020 Ref	
θ <sub>1</sub>	0°	8°
θ <sub>2</sub>	7° BSC	

**NOTE:**

1. All dimensions are in inches.
2. Lead coplanarity should be 0" to 0.004" max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.0075" from the lead tip.

For additional information regarding our products, please visit CADEKA at: [cadeka.com](http://cadeka.com)

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 T: 970.663.5452  
 T: 877.663.5452 (toll free)

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